International Journal of Power Electronics and Drive Systems (IJPEDS)
Vol. 15, No. 2, June 2024, pp. 1052~1060
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v15.i2.pp1052-1060

Design of a high-speed MCML D-Latch at 0.6 V in 45 nm CMOS technology

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Article Info

Article history:

Received Jun 9, 2023
Revised Oct 25, 2023
Accepted Nov 7, 2023

Keywords:

D-Latch
Low voltage folded D–Latch
MOS current mode logic
Noise
Power
Propagation delay

ABSTRACT

Metal oxide semiconductor (MOS) current mode logic (MCML) is generally preferred for high-speed circuit design. In this paper, a novel low voltage folded (LVF) MCML D-Latch is designed. The existing topologies of the MCML D-Latch consume more power and operate at 1 V. The proposed D-Latch can operate at 0.6V with better delay and power management. MCML circuits minimize delay and perform fast operations, hence it can be used in high-frequency applications. The proposed LVF MCML D–Latch is analyzed with the parameters such as power, delay, power delay product and output noise using cadence virtuoso in 45 nm complementary metal oxide semiconductor (CMOS) technology at a voltage of 0.6 V and a temperature of 27 °C. The proposed technique achieves 62.11% of power reduction, transient response speed improved by 51.23% and noise cancellation becomes 26.13% improvement over the existing circuit. It also achieves 96% of output swing which is more efficient compared to others. Finally, the parametric analysis is performed with different temperatures to verify the stability of the proposed circuit. From the simulated results, it is clear that the proposed LVF MCML D-Latch provides better performance in high-speed phase locked loop (PLL) applications.

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1. INTRODUCTION

In high-speed circuit design, the power consumption and frequency are interrelated in complementary metal oxide semiconductor (CMOS) techniques. Specifically, higher frequencies typically result in increased power consumption. However, in the case of current mode logic (CML), regardless of the frequency used, it maintains a consistent power level [1]. CML uses metal oxide semiconductor (MOS) transistors called MCML circuits. MCML can be widely used in radio frequency and mixed-signal integrated circuit (IC) design. CML is widely utilized because of its high resistance to common-mode signals. This characteristic also makes MCML a favored option in mixed-signal environments [2], [3]. High-performance analog and digital circuits may now be integrated on the same silicon substrate because of developments in semiconductor technology. Due to the significant switching noise, the standard CMOS logic approach does not have analog friendly environment [4], [5]. MOS current mode logic (MCML) replaces CMOS with minimum switching noise and also achieves high speed with better power management in flip-flop design [6], [7]. Because of this feature, MCML is specially used in high-speed signaling of digital data (which includes chip-to-chip applications) and mixed-signal ICs [8]–[10].

In phase locked loop (PLL), MCML can be used for high-speed applications using hybrid current starved ring voltage-controlled oscillator (VCO) [11]. Design of high-speed phase frequency detector (HSPFD) achieves low power and wideband PLL [12]. All digital PLL (ADPLL) is also used for digital communication applications [13], [14]. The concept of CML uses pair of MOS differential transistors because differential signaling protects against switching noise and the current mode provides quick switching [15]–[17]. Maintaining voltage stability is essential for ensuring the safe functioning of power systems. Voltage instability can lead to the emergence of unacceptably low voltages across a significant portion of the network. To adjust that, voltage scaling is used. Voltage scaling refers to the technique of adjusting the supply voltage level in electronic circuits to achieve specific design objectives. It involves either increasing or decreasing the voltage supplied to the circuit components to optimize certain performance parameters through signal integrity. It is a measure of how well the signal retains its desired characteristics, such as voltage levels, timing, and shape, without distortion, degradation, or interference [18], [19]. A tri-state gate is capable of generating an output similar to a conventional gate when it is enabled. However, when it is disabled, it produces a high impedance output, effectively disconnecting the output node from the power supply and ground. This feature helps to minimize power consumption in the circuit [20], [21].

D-Latches are the basic building blocks for digital IC implementation and are used in many applications. Clock skew is the time difference of the clock signal. Parasitic effects in CMOS refer to unintended or undesired electrical characteristics that arise due to the inherent nature of the CMOS fabrication process or the layout of the integrated circuit. These effects can impact circuit performance, introduce errors, and degrade overall system functionality [22], [23]. CML topology is frequently used for D-Latch design where high-speed operation is required [24]–[26]. The traditional MCML topology consists of source, load and pull-down network. The pull-down network performs the logical implementation [27]. Two differential inputs A and Abar are applied as inputs. It produces the output as inverter/buffer logic at out and out bar nodes. The novel low voltage folded (LVF) D-Latch design improves its performance. It utilizes a current mirror circuit along with a stack of transistors to enhance performance. The design was validated through simulations conducted using cadence virtuoso, utilizing 45 nm CMOS technology with 0.6 V supply and 27 °C of temperature, operating at a frequency of 1 GHz. The proposed D-Latch achieves very low power of 4.285µW with a minimum delay of 80.62 ps and a power delay product of 0.35 fJ. The output noise as low as -167.5 dB. The swing voltage is 0 to 580 mV. The percentage of performance improvement in terms of average power, propagation delay, noise, swing voltage, and power delay product is 62.11%, 51.23%, 26.13%, 96%, and 81.28% respectively.

This paper is organized into some sections: i) Section 2 describes existing folded MCML D-Latch with the mathematical equations based on the literature; ii) Section 3 presents the proposed LVF MCML D-Latch; iii) Section 4 analyses the simulation results, performance comparison with existing D-Latch; and iv) Section 5 concludes the paper.

2. RELATED WORK

Figure 1 shows the conventional D-Latch using MCML [28]. It comprises two stages of transistor pairs for logic function implementation and transistor M_1 for bias current I_{ss} generation. The differential circuit are the clock (CLK) inputs activate transistors M_2 and M_3 which are present in the lower part of the transistor pair that alternatively drives the transistors M_4, M_5, M_6, and M_7 which is the upper part of the transistor pair. When the CLK input is high, M_2 becomes ON and M_3 becomes off hence via M2, the bias current propagates which drives the upper part of transistors M_4 and M_5 based on D input. When the CLK input is low, M_3 becomes ON and M_2 becomes off, hence through M_3 transistor the current propagates, which drives the upper part of transistors M_6 and M_7. Hence the D-Latch maintains the hold condition because the output does not change based on the input value. In the existing folded D-Latch [29] in Figure 2, the differential CLK is given as input to drive the M_1 and M_2 transistors. This directs $I_{ss,}$ the bias current, to the current mirror transistors.

The differential input signal of M_3 and M_4 transistors samples the signal, while the transistors M_5 and M_6 hold the received signal because of the positive feedback. The differential voltage for D and clock signals are V_{CMD} and V_{CMCLK} respectively. D-Latch swing voltage V_{swing} represented in (1) and output signals are given by [29],

$$V_{Swing} = 2I_{ss}R_L \quad (1)$$

for D–Latch proper output, the conditions (2)-(5) have to be satisfied with the transistors in the saturation region,

$$V_{DS9,10} = V_{CMD} - V_{GS3-6} > V_{DS_{sat}9,10} \quad (2)$$

$$V_{DS3,4} = V_{DD} - \frac{V_{Swing}}{2} - (V_{CMD} - V_{GS3-6}) > V_{DS_{sat3,4}} \quad (3)$$

$$|V_{DS13}| = V_{DD} - (V_{CMCLK} - |V_{GS1,2}|) > |V_{DS_{sat13}}| \quad (4)$$

for the conventional MCML inverter,

$$V_{CMD} = V_{DD} - \frac{V_{Swing}}{4} \quad (5)$$

From the P-channel metal oxide semiconductor (PMOS) MCML inverter in Figure 2, the input clock signal is generated. To reduce the supply voltage V_{DD}, the value of V_{CMCLK} given in (6) should be,

$$V_{CMCLK} = \frac{V_{Swing}}{4} \quad (6)$$

based on (6), the (7)-(9) represent the values of $V_{DD,min}$ and V_{ov}.

$$V_{DD,min} = \frac{V_{Swing}}{4} + V_{Gs3-6} + V_{DS_{sat9,10}} \quad (7)$$

$$V_{DD,min} = \frac{V_{Swing}}{4} + V_{TH} + 2V_{ov} \quad (8)$$

$$V_{ov} = V_{GS} - V_{TH} \quad (9)$$

Where V_{OV} and V_{TH} are the overdrive voltages and threshold voltages respectively. In this design, clock and data cannot set with the same common-mode signal. If the same clock and data signal is used, it makes $V_{DS1,2}$ a zero value. Hence this makes the circuit less optimization in propagation delay. To optimize the circuit with less power and propagation delay, a novel LVF MCML D-Latch is designed.

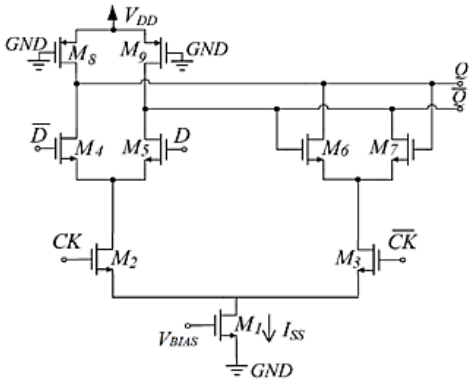

Figure 1. Conventional MCML D-Latch [28]

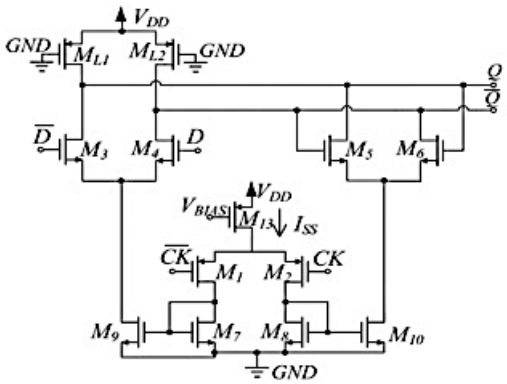

Figure 2. Existing folded MCML D-Latch [29]

3. PROPOSED LVF MCML D-LATCH

Figure 3 shows the novel design for a low voltage folded (LVF) D-Latch using MCML. In comparison to conventional and existing circuits, this proposed LVF MCML D-Latch is capable of operating at a low voltage of 600 mV. It offers enhanced optimization by allowing independent operation of the clock and data signals. The LVF D-latch introduces M_{14} and M_{15} transistors to maintain equal voltage differences (Vds) across the current mirror transistors. When the bias voltage of M_{14} and M_{15} matches the D input voltage, the transistors M_7, M_8, M_9, and M_{10} are biased with the same drain-source voltage. Hence, in the novel LVF D-Latch, the common mode voltages of the clock and data values can be assigned individually or with equal values. This feature enhances the optimization of the circuit, especially under low voltage conditions, resulting in improved accuracy. The enhanced accuracy leads to better noise regulation and reduced delay at low voltages. The layout for the proposed D-Latch is shown in Figure 4. The LVF D-Latch can operate at a minimum voltage of [29] represented in (10)-(12) as $V_{DD,min,LVF}$.

$$V_{DD,min,LVF} = \frac{V_{Swing}}{4} + V_{Gs3,4,5,6} + V_{DS_{sat9,10}} \quad (10)$$

$$V_{DD,min,LVF} = \frac{V_{Swing}}{4} + V_{TH} + 2\,(V_{GS} - V_{TH}) \quad (11)$$

Where $V_{GS}–V_{TH}$ is the overdrive voltage of the proposed LVF D-Latch and V_{TH} is the MOS threshold voltage. Referring to the 45 nm CMOS technology, V_{TH} is typically 0.35 V, the overdrive voltage can be made between 0.05 to 0.1 V and 2(V_{GS} –*VTH*) becomes 2 × 0.05 V = 0.1 V. From Figure 5, the swing voltage of the LVF D-Latch is approximately 0.6 V, hence the (11) becomes,

$$V_{DD,min,LVF} = \frac{0.6}{4} + 0.35 + 0.1 = 0.6\ \text{V} \quad (12)$$

In addition to this, a stack of two N-channel Metal Oxide Semiconductor (NMOS) transistors such as M_{16}, M_{17} and M_{18}, M_{19} is connected. These transistors are biased with the same bias voltage as M_{13}. This stack of transistor arrangement reduces the leakage power which is generated at the input stage of the transistor pair. This makes the circuit more optimized. Hence it improves the circuit performance with minimum power and operates at a voltage of 600 mV. The stacking effect refers to the reduction of sub-threshold leakage current in transistors when they are in the off state, which is achieved by dividing or splitting the transistors. By stacking the transistors, the effective threshold voltage is increased, reducing the leakage current that would otherwise flow through a single transistor. This technique helps to improve the power efficiency, when the transistors are not actively conducting.

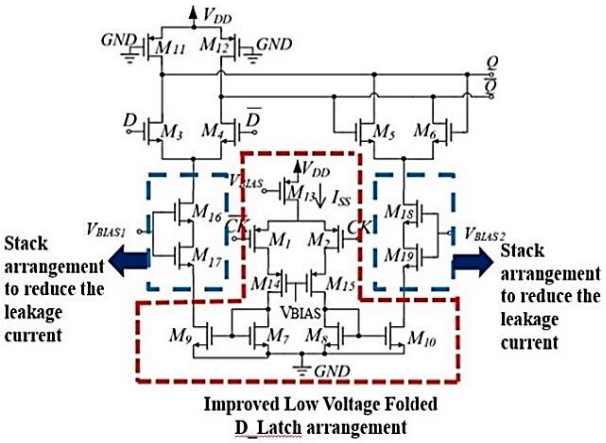

Figure 3. Proposed LVF MCML D-Latch

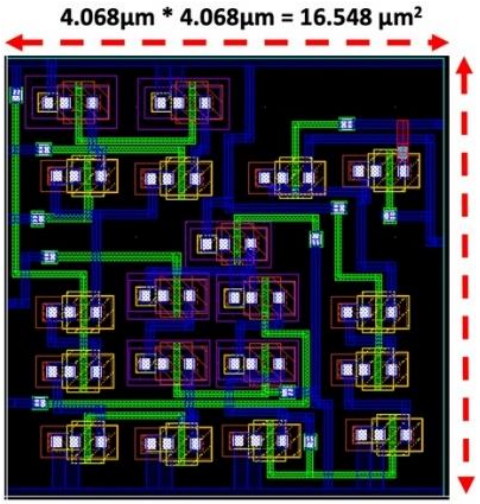

Figure 4. Layout design of proposed D-Latch

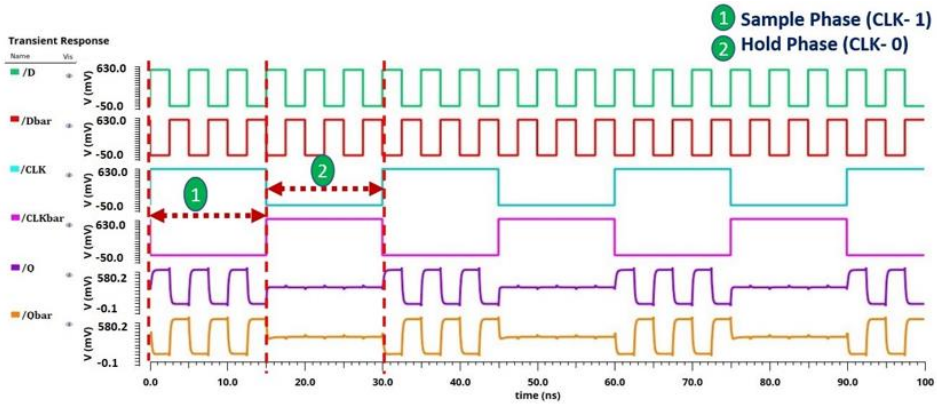

Figure 5. Transient response of the proposed LVF D-Latch

Figure 5 illustrates the operation of the proposed LVF D-Latch under various T_{ON} and T_{OFF} conditions. The input signals to the circuit are the clock (CLK) and data (D) signals. The circuit functions as a sample and hold device. During the sample phase, when CLK=1 and D=1, transistors M_1, M_7, M_9 are turned ON, along with transistor M_3. Similarly, when CLK=1 and D=0, transistors M_1, M_7, M are turned ON, along with transistor M_4. In this phase, the circuit samples the D-Latch input and produces the corresponding output. During the HOLD phase, when CLK=0 and D=1, transistors M_2, M_8, M_{10} are turned ON, along with transistor M_6. Likewise, when CLK=0 and D=0, transistors M_2, M_8, M_{10} are turned ON, along with transistor M_5. In this phase, the circuit retains the previous output value. Hence in the LVF D-Latch, with specific transistor configurations depending on the CLK and D inputs it performs the desired functions in the sample and hold phases.

4. SIMULATION RESULTS

Table 1 provides information about the simulation environment used for the analysis. The process corners mentioned in Table 1 are categorized as slow slow (SS), slow fast (SF), fast slow (FS), typical typical (TT), and fast fast (FF). Monte-Carlo analysis and parametric analysis are also performed. Different temperature analysis is performed with 0 °C to 100 °C. The circuit operates with the frequency of 1 GHz.

Table 1. Simulation environment

Simulation environment	Specifications
CMOS technology	45 nm
Supply voltage	0.6 V
Process corner	TT, FF, SS, SF, FS
Frequency	1 GHz
Temperature	27 ℃

4.1. Analysis of power, propagation delay, power delay product, and noise

Table 2 presents a comparison of power, delay, noise and PDP values of D-Latch. The evaluation is performed at 45 nm CMOS technology with 0.6 V supply. The proposed circuit demonstrates an average power consumption of 4.385 μW, along with a minimum delay of 85.62 ps, power delay product of 0.35 fJ with minimum noise of -167.5 dB. Table 3 provides details regarding power consumption, delay, and output noise at different temperatures. To illustrate the performance achieved by the proposed circuit, Table 4 provides the performance improvement in percentage. The proposed circuit exhibits a significant improvement, with a power enhancement of 62.11%, a delay reduction of 51.23%, and a power delay product improvement of 81.28%, compared to the existing folded topology.

Table 2. Simulation results with different process corners

Parameter	Different topology of MCML D-Latch	Different process corners				
		TT	FF	SS	FS	SF
Power (μW)	Existing D-Latch [29]	11.31	17.01	6.662	10.36	10.81
	Proposed D-Latch	4.385	7.274	2.121	3.595	4.214
Propagation Delay (ps)	Existing D-Latch [29]	165.32	122.29	210.3	150.34	198.4
	Proposed D-Latch	85.62	39.18	158.8	66.62	113.8
Power Delay Product (fJ)	Existing D-Latch [29]	1.87	2.08	1.42	1.56	2.14
	Proposed D-Latch	0.35	0.28	0.34	0.24	0.48
Noise (dB)	Existing D-Latch [29]	-132.8	-134.6	-130.7	-131.3	-131.6
	Proposed D-Latch	-167.5	-169.3	-165.9	-166.1	-166.3

4.2. Monte-Carlo and parametric analysis

Figure 6 shows the histogram plot of the Monte-carlo analysis for the proposed LVF D-Latch of Figure 6(a) power, Figure 6(b) propagation delay, and Figure 6(c) noise. The simulations involve 200 samples that consider random statistical variations. From the histogram plot, it is evident that the mean value of the power distribution is 4.385 μW, which aligns closely with the TT results presented in Table 2 that represents the stability of the proposed design. The parametric analysis of the proposed D-Latch was conducted by varying temperature values to assess D-Latch performance.

Figure 7 shows the temperature Vs power and delay waveforms. The propagation delay at different process corners shown in Figure 8. Figure 9 depicts the performance improvement in percentage of Figure 9(a) power and Figure 9(b) propagation delay. Figure 10 illustrates the performance comparison of D-Latch with

different process corners of Figure 10(a) power, Figure 10(b) propagation delay, and Figure 10(c) power delay product.

Table 3. Power, delay, and output noise of proposed D-Latch at different temperatures

S.no	Temperature (°C)	Power (µW)	Delay (ps)	Output Noise (dB)
1.	0	4.53	78.93	-167.9
2.	25	4.32	79.63	-167.6
3.	50	4.10	80.04	-167.2
4.	75	3.89	80.34	-166.9
5.	100	3.68	80.62	-166.7

Table 4. Performance improvement in percentage of the proposed D-Latch

Parameter	Existing folded D-Latch [29]	Proposed LVF_ D-Latch	Percentage improvement
Power (µW)	11.31	4.285	62.11 %
Propagation Delay (ps)	165.32	80.62	51.23 %
PDP (fJ)	1.87	0.35	81.28 %
Noise (dB)	-132.8	-167.5	26.13 %

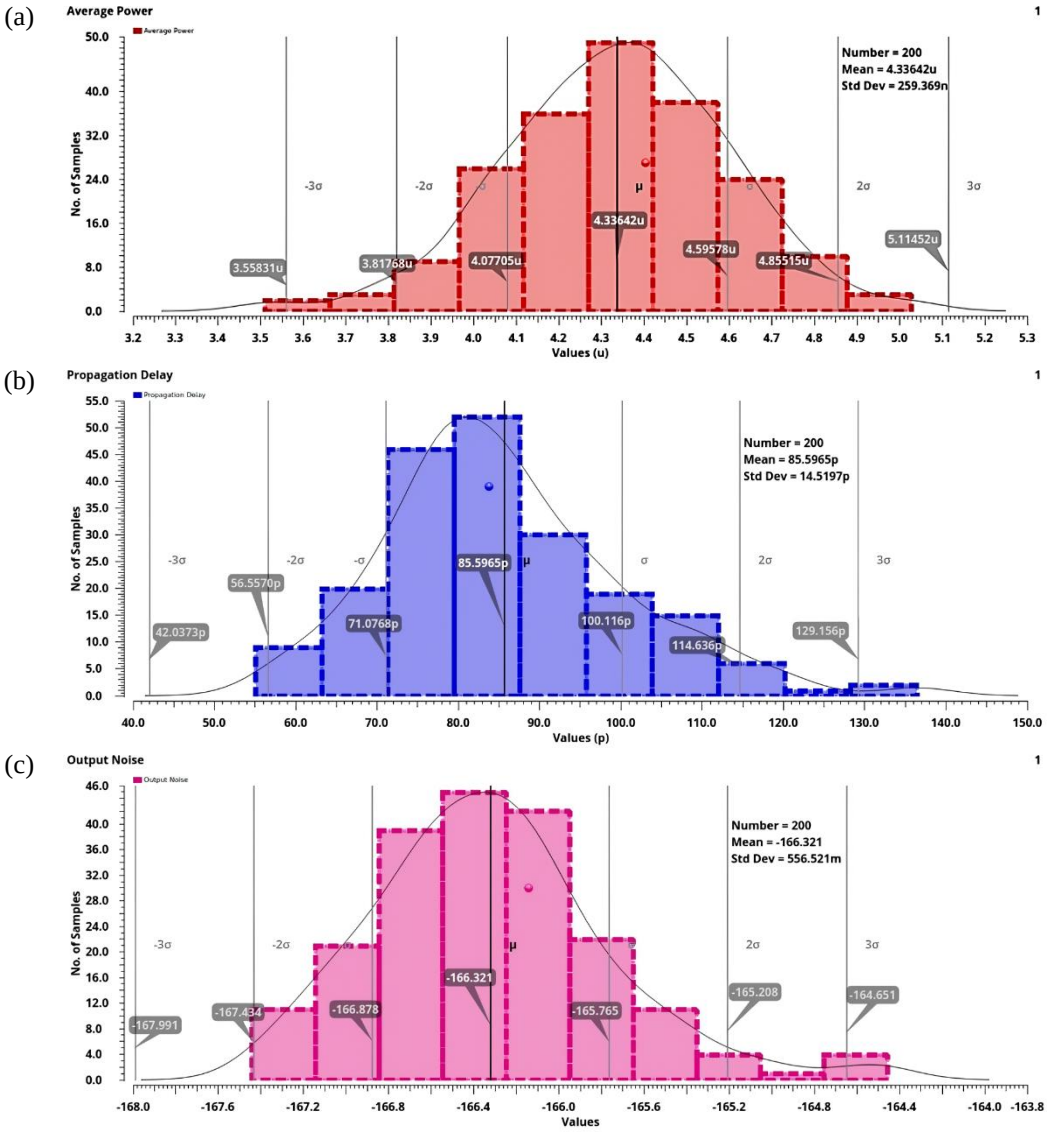

Figure 6. Monte carlo analysis for the proposed LVF D-Latch of (a) power, (b) propogation delay, and (c) noise

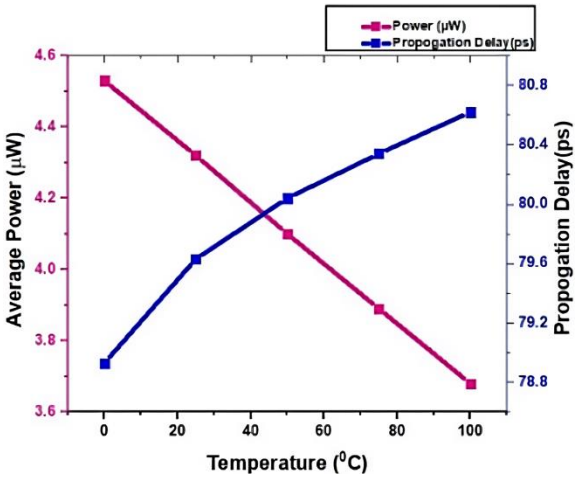

Figure 7. Temperature vs power and delay

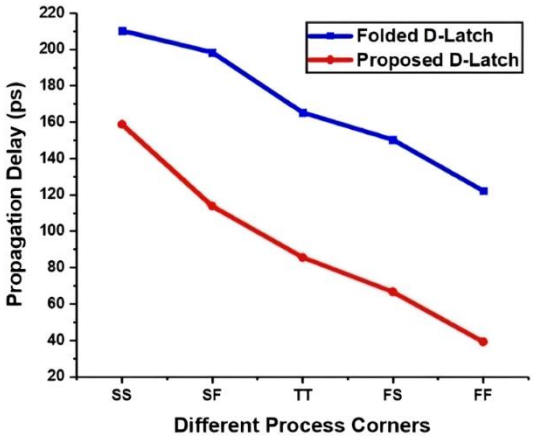

Figure 8. Process corners vs propagation delay

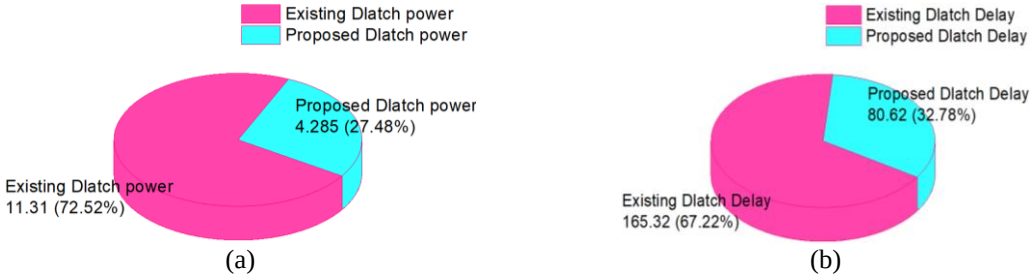

Figure 9. Performance improvement in percentage of (a) power and (b) propagation delay

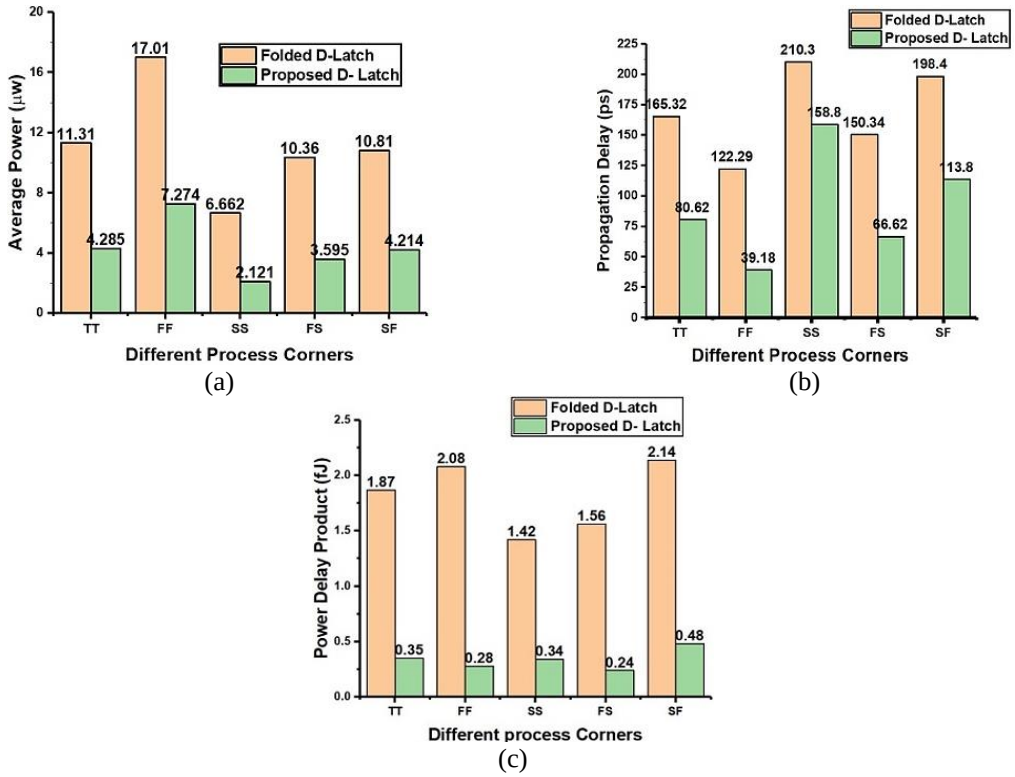

Figure 10. Performance comparison of D-Latch with different process corners vs (a) power, (b) propagation delay, and (c) power delay product

5. CONCLUSION

In this paper, LVF MCML D-Latch circuit is analyzed along with the existing folded D-Latch at 0.6 V and 27 °C of temperature in 45 nm CMOS technology and operating at a frequency of 1 GHz. The proposed LVF D-Latch demonstrates excellent performance, with a power consumption as low as 4.385 µW, a minimum delay of 85.62 ps, and a power delay product of 0.35 fJ across different process corners. The output noise is remarkably low, measuring at -167.5 dB. The swing voltage range of the proposed D-Latch is from 0 to 580 mV. To further validate the results, Monte Carlo simulations are conducted, and the histogram plots of power, delay, and noise analysis are analyzed. The proposed topology is also subjected to parametric analysis, considering different temperatures, and the corresponding power, delay, and noise values are measured. Moreover, the estimated layout area of the proposed design is only 16.548 μm^2, indicating its compactness and efficiency. Based on the achieved results, the proposed LVF MCML D-Latch circuit exhibits excellent performance, making it suitable for applications in mixed-signal environments that require low power consumption, high-speed operation, and can be utilized in high-frequency PLL applications.

ACKNOWLEDGEMENT

The authors would like to thank the Department of Electronics and Communication Engineering, SRM Institute of Science and Technology, Kattankulathur, for providing the resources (EDA Lab – Cadence Virtuoso tool) to this research.

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