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CSA-based harmonic elimination controlled reduced switch multilevel inverter for standalone PV system

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ABSTRACT

A standalone photovoltaic (PV) system has emerged as a clean energy solution for application in remote areas. To establish such a system a suitable converter is required for voltage boosting as well as to produce high-quality output as required by the load. To achieve this, multilevel inverters (MLIs) are the proven substitute in PV systems. A conventional MLI uses multiple sources and switches that increase the cost and complexity. To provide a complete stand-alone system solution that addresses this issue, reduced component switched capacitor (SC) based seven-level MLI is disclosed in this paper. A new crow search algorithm (CSA) based selective harmonic elimination (SHE) method is employed to estimate the switching angles. The dominant harmonic orders are removed from the 7-level SC-MLI output while the desired firing angles for the switches are evaluated. Using only seven switches, the circuit boosts the voltage to 1.5 times with the aid of self-balanced capacitors. Therefore, the circuit does not require an additional control circuit for voltage balancing. The overall system is designed in MATLAB/Simulink environment to test under different operating conditions. An experimental prototype of the 7-level SCMLI is also designed to validate the CSA-based SHE control and MLI performance in real time.

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1. INTRODUCTION

Independent clean power supply portrays a prime role in the case of cities, remote areas as well as remote crop fields in rural areas. For this purpose, a stand-alone PV System can contemplate an efficacious solution. For solar PV systems, extraction of maximum power and extraction of boosted-constant voltage; is the first phase in the fabrication of an energy system, which can be noted [1]. Effective maximum power point tracking (MPPT) [2] algorithms can contrivances with effective converters to get reliable and improved output from PV-based systems. The transformer-less system for energy conversion for clean power systems is increasing the popularity of multi-level inverters (MLI) day by day. Moreover, low switching loss and low voltage stress on the semiconductor switches make MLI more reliable to use in high and medium-power applications.

The cascaded h-bridge MLI (CHB MLI) structure is more popular among all the conventional topologies as it uses a smaller number of capacitors, diodes, and need not require a complex voltage balancing strategy. In PV applications the MLIs require individual DC sources and multiple switches to bring out the aimed voltage levels at the output. This becomes a major consternation of all the conventional MLI

topologies, another major concern for CHB MLI is the lower order harmonics which will degrade the efficiency of the system and also may create torque pulsation in various electric drives. In different literature, these two problems are tried to figure out [3], [4]. Some researchers focused on the elimination of a number of components (elimination of switches and sources) by providing innovative topologies and some focused on harmonic elimination techniques to reduce the THD for PWM techniques.

The Reduced MLI design can be developed by taking the help of switched capacitors. With an effective switching scheme and self-balancing scheme for charging-discharging of capacitors, a greater number of levels can be achieved. This reduces the cost of MLI as lower number of driver circuits will be used for this. Voltage boosting can be obtained which eliminate the use of separate boost converter for PV applications. Some of the structures that implements this concept are discussed in [5]. But they use multiple DC sources for getting the aimed output levels. The SC-MLI structures given in [6], [7] uses less number of switches but the total standing voltage (TSV) is high for these cases that increases the cost. Therefore, the focus of this paper is to provide a low-cost SC-MLI topology with lower TSV with boosting capability.

To get low harmonics several control and modulation techniques are proposed which can enhance the performance of MLIs. They come under two categories, one is low-switching frequency control techniques and high-frequency control techniques. Switching loss is the major concern in the case of high-frequency controlling schemes in spite of the benefit of lowering the current THD. In this regard, the selective harmonic elimination (SHE) scheme (part of the fundamental switching control schemes) is widely used. the dominant lower-order harmonics can be annihilated resulting in lower THD. Higher-order harmonics can be lowered as proposed by researchers in [8]. In SHE, optimized switching angles for the power switches needed to be computed to diminish targeted lower-order harmonics for several modulation indexes. For this, nonlinear transcendental equations are solved, and the suitable solutions are stored in look-up tables. The optimized solution of transcendental equations can be derived using different suitable methods such as numerical methods like Neuton-Raphson (NR), but the issue is to identify the suitable initial value [9]. Evolutionary algorithms like particle swarm optimization (PSO) [10], bee algorithm (BA), colonial competitive algorithms (CCA), generalized pattern search (GPS), genetic algorithm (GA) [11]–[14]. Firefly based algorithm (FA) serves this purpose but implementation complexity and computation time is the major concern for these. In PV applications, with fixed dc source systems, a particular order of harmonics can be banished, but when the optimal dc sources are increased it cannot move out the targeted harmonics over a large range of modulation indexes. The key problem in this method is difficult in practical implementation as there is a dynamic change in each input dc source for a particular modulation index. BA is a more complex algorithm than GA, but GA ineffectual to compute the solution for asymmetrical MLI. Kachitvichyanukul in [15] various evolutionary algorithms are compared based on convergence speed, and implementation complexity for SHE, PSO algorithm has shown better accuracy and lower complexity.

The researchers in [16]–[18], modified PSO algorithms are used to get suitable optimized switching angles for seven-level MLIs, but the concern is the local minima particles are more enticed to global best locations. The main issue with FA is the lower convergence rate and the incapability of storing the previously obtained solutions. Further, a detailed review of different SHE schemes has been carried out for different MLIs in [19], which suggests SHE scheme is reliable compared to other existing modulation schemes. Saleh *et al.* in [20], a thorough comparison of fundamental frequency control schemes such as SHE and nearest level control is carried out. The control scheme is tested on a multi-DC 13-level structure for different modulation index. Newton Raphson method-based SHE scheme is applied to remove the dominant lower-order harmonics. An improved genetic algorithm-based control in [21] is applied for an asymmetrical 9-level inverter to suppress the 5^{th}, 7^{th}, and 11^{th}-order harmonics. The fundamental frequency SHE scheme has been compared with a high-frequency pulse-width modulation scheme in [22]. Tests are carried out on the 7-level inverter to justify the advantages of the SHE schemes. Artificial neural network (ANN)-based SHE scheme with real-time switching has been verified in [23]–[25]. A comparison is performed with PSO-based SHE control and ANN scheme. The harmonic reduction performance of ANN-based control is found superior to the PSO scheme. A novel moth-flame-based SHE scheme tested for different MLIs performs better compared to traditional differential evolution algorithms [26].

To solve the above-discussed issues, a new swarm intelligence algorithm crow search algorithm (CSA) recently evolved based on the intelligence behavior of crows, which can provide a better solution with less complexity and a smaller number of parameters and flexibility. CSA is developed by Askarzadeh in 2016 [27], [28]. This algorithm gains attention due to a smaller number of parameters and easy implementation. This method provides a solution by searching using the population of points, which gives a better solution than a single-point search in the conventional method. Therefore, to get a suitable firing angle for each power switch SHE technique is applied and the nonlinear equations are solved using the CSA in this paper. The paper presents a system design for a stand-alone PV system with improved 7L-MLI (with a smaller number of components) and THD is reduced by eliminating targeted harmonics using the CSA-based

SHE technique. Next, section 2 presents the organization of different components of a stand-alone PV system and the improved topology for the seven-level inverter is described with a comparison with existing topologies. Section 3 contains the details of the implementation of CSA-based SHE, for THD reductions. The simulation of the proposed system and results are summarized in section 4. The proposed method is implemented by developing a prototype to validate the simulation result and theoretical analysis in section 5. Finally, conclusions are drawn in section 6.

2. PROPOSED STAND-ALONE PV FED 7-LEVEL MLI SYSTEM

Figure 1 shows the proposed stand-alone system, which incorporates a single source. The input can be connected directly to PV array. The input is fed to combination seven switches (T_1-T_7), two capacitors (C_1-C_2) and 2 diodes (D_1-D_2) as shown in Figure 1. This circuit synthesizes 7-level output, i.e., (0, ±0.5 V_{DC}, ±V_{DC}, ±1.5 V_{DC}). The boosted output is obtained with fewer components as compared to a conventional MLI. For instance, a CHB MLI requires 12 switches to produce a 7-level output, which is quite high compared to the proposed design. The operation of the circuit is tested using SHE-PWM technique incorporating CSA algorithm.

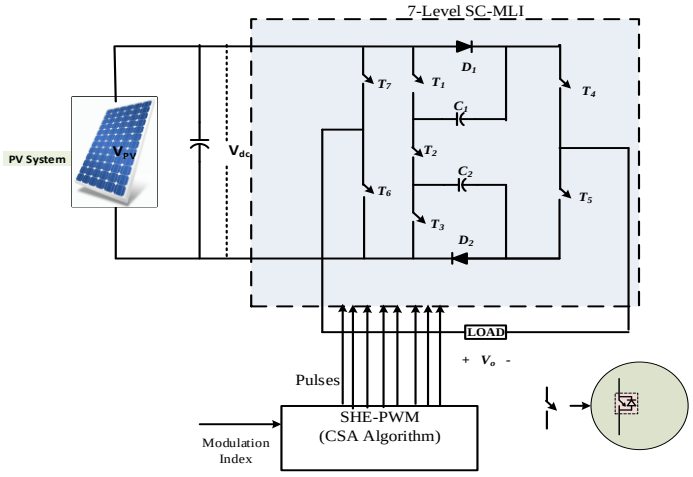

Figure 1. Overall circuit diagram of proposed stand-alone PV fed MLI system

The summary of switching sequence for each level is mentioned in Table 1. The Figure 2 shows the detail current flow in each level. The disclosed circuit operation to get the desired level of output across the load is summarized as follows:

- Zero level: The current path is provided by turning on T_2, T_4, and T_7. This furnishes zero voltage across the output with charging of C_1 and C_2 up to 0.5V_{DC}. The current path can be visualized in Figure 2(a).
- 1st positive -level: The voltage of capacitor C_1 appears across the load with the conduction of T_1, T_4, and T_7. C_2 does not come in the path in this pattern so remains unchanged. In Figure 2(b), the current path is illustrated. The output of voltage is equal to the parallel capacitor C_1 (0.5V_{DC}).
- 2nd positive-level: When T_2, T_4, and T_6 conduct C_1 and C_2 are charged due to a series connection. The source voltage appears across the output (V_{DC}) which can be realized as in Figure 2(c). The current path is completed through load is completed by using T_4 and T_6.
- Top positive-level: In this Level capacitor C1 discharges with the conduction of T_1, T_4, and T_6. The voltage across the source and charged capacitors across the load, cause the highest level of output voltage (1.5 V_{DC}). The current path can be illustrated in Figure 2(d).
- 1st negative-level: The current path is completed by the conduction of T_3, T_5, and T_6. The C is in discharging condition whereas no effect on C_1. The negative voltage (-0.5 V_{DC}) will be generated across the load due to the opposite polarity during the discharge of capacitors. The current path can be illustrated in Figure 2(e).
- 2nd negative-level: For this level, the current path is completed with T_2, T_5, and T_7 Conduction. C_1 and C_2 is undercharging condition as they are in a series path. The voltage across the load is -V_{DC} the source is connected with an opposite polarity that can be verified from Figure 2(f).

– Top negative-level: When T_3, T_5, and T_7 are in ON state, the voltage across C_1, C_2, and the source appears across the load with opposite polarity. The out voltage is the contribution of capacitor voltage and source voltage. The current path projected in Figure 2(g).

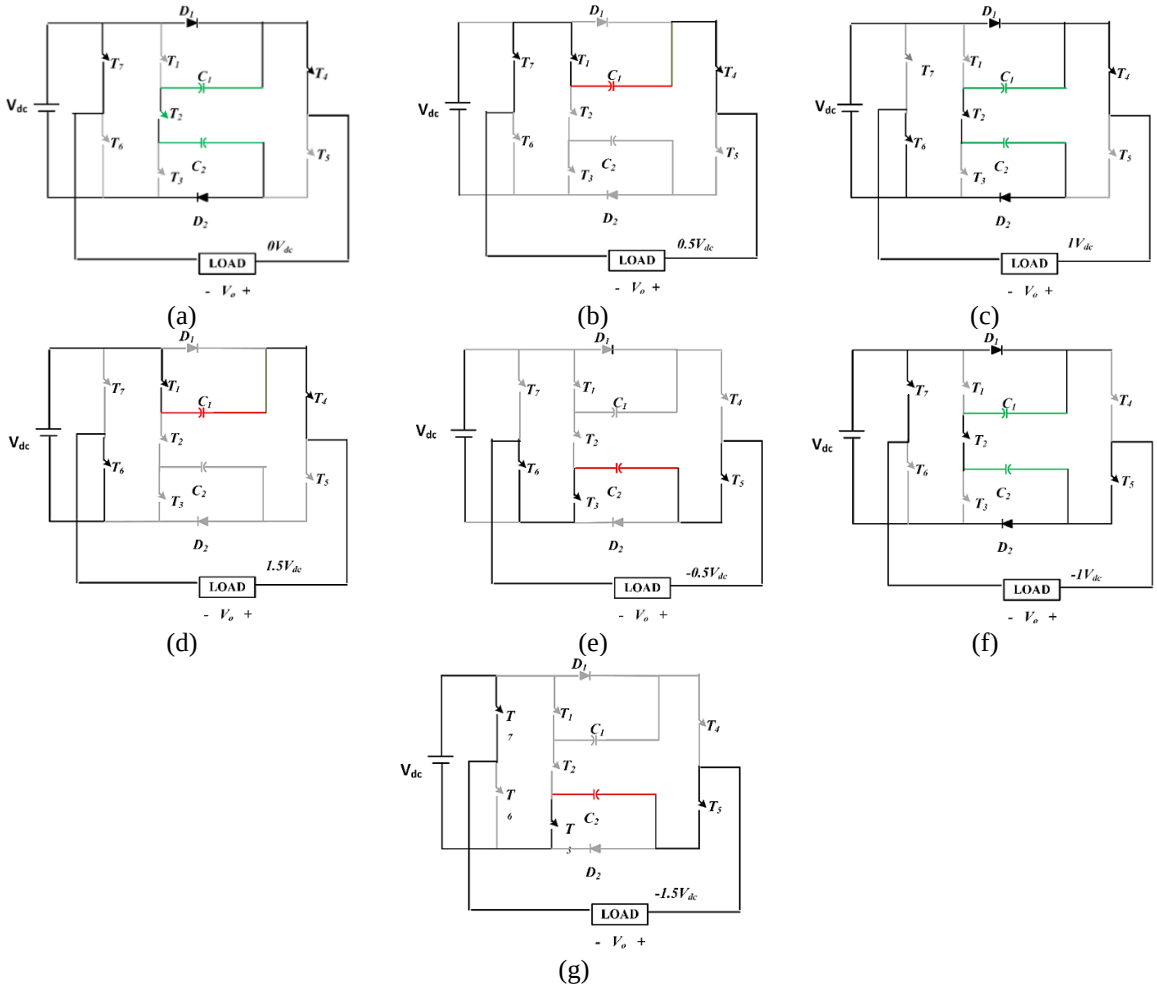

Figure 2. Current path for each level output, (a) 0 V_{DC}, (b) 0.5 V_{DC}, (c) 1 V_{DC}, (d) 1.5 V_{DC}, (e) -0.5 V_{DC}, (f) -1 V_{DC}, and (g) -1.5 V_{DC}

Table 1. Switching scheme for proposed SC-MLI

Output voltage level	Switch in conduction mode	Capacitor (C_1, C_2) status
0 V_{dc}	T_7, T_4, T_5	C_1 (charging), C_2 (charging)
0.5 V_{dc}	T, T_4, T_7	C_1 (discharging), C_2 (no effect)
1 V_{dc}	T_2, T_4, T_6	C_1 (charging), C_2 (charging)
1.5 V_{dc}	T_1, T_4, T6	C_1 (charging), C_2 (no effect)
-0.5 V_{dc}	T_6, T_3, T_5	C_1 (no effect), C_2 (discharging)
-1 V_{dc}	T_7, T_2, T_5	C_1 (charging), C_2 (charging)
-1.5 V_{dc}	T_7, T_3, T_5	C_1 (no effect), C_2 (discharging)

2.1. Comparative analysis of the proposed SCMLI with various topology

The 7L-SCMLI that is suggested in this paper is compared with existing 7-level MLI topologies (top-1-top-8) proposed recently, by taking some key features into consideration, such as the number of power electronics switches utilized, number of capacitors and diodes incorporated in the structure. Table 2 includes a thorough comparison of different MLI topologies with the proposed MLI. The ability to enhance the output voltage and total standing voltage (TSV) associated with the switches are taken into consideration, to know the level of advancement in the suggested topology. The voltage stress on each switch is taken into the

calculation as it is a deciding factor for the selection of type switch and rating for MLI. The MLI circuit analyzed in [6] provides 3 times boosting in output, but the level of complexity and the cost increases due to the presence of 16 semiconductor switches with 3 switched capacitors, the stress on switches is quite high. For 7-level generation and 3 times boosting capability, the circuit design projected in top-2 [7] uses 14 switches and 2 capacitors. The TSV is 14 V_{DC}, which is again a concern for high-voltage applications. Three times boosting capability is also provided by topologies presented in top-3 [29] and top-4 [30] with a comparatively lower number of switches and capacitors but the TSV is higher than the former designs. The TSV is low in the case of top-5 [31], top-6 [32], and top-7 [33], but the boosting capability was reduced to 1.5 times. The number of capacitors increased, which will cause higher complexity for the charging and discharging scheme. The MLI-circuit in top-8 [34], uses the lowest number of switches with lower TSV but is not able to provide a boost to the output. On the contrary, the proposed MLI design provides 7-level output with 1.5 times boosting, with the utilization of 7 switches and 2 capacitors, which is lower than other topologies. The TSV is also low at 6.5 times the $V_{DC.}$ The utilization of switches, diodes, driver circuits, switched-capacitors, total blocking voltage of switches, and number of dc sources utilized in the circuit contribute to the increasing of cost of the system. To compare the different topologies, a cost factor is calculated as (1).

$$cost\ factor = [N_{sw} + N_{DR} + +N_D + N_C + \left(\delta \times \frac{T_{SV}}{GAIN}\right)] \times \frac{N_{dc}}{N_L} \quad (1)$$

The weight factor (δ) is chosen as per the priority given to switch count or total standing voltage. If the priority is switching count ($\delta = 0.5$), if the priority is TSV ($\delta = 1.5$) is taken for the comparative analysis.

Table 2. Comparison of proposed structure with existing topologies

Factors are taken for analysis	Top-1	Top-2	Top-3	Top-4	Top-5	Top-6	Top-7	Top-8	Proposed topology
Number of switches utilized (N_{SW})	16	14	12	9	10	10	8	7	7
Number of capacitors utilized (N_C)	3	2	2	2	4	3	2	3	2
Number of diodes utilized (N)	0	2	0	1	0	0	2	2	2
Number of DC source utilized (N_{DC})	1	1	1	1	1	1	1	1	1
Gain achieved	3	3	3	3	1.5	1.5	1.5	1	1.5
TSV (x V_{DC})	14	14	16	17	8	7	7	5	6.5
COST FACTOR ($\delta = 0.5$)	5.33	4.81	4.01	3.34	3.73	3.55	3.1.3	3.01	2.82
COST FACTOR ($\delta = 1.5$)	5.88	5.46	4.76	4.13	4.48	4.2	3.78	3.71	3.43

3. HARMONIC REDUCTION USING CSA-BASED SHE

The CSA-based approach for SHE is implemented to eradicate 3rd and 5th harmonics from the output of the improved seven-level topology. The switching angles are calculated and saved in a look-up table by using CSA algorithm, then applied for the simulation of suggested MLI structure. With elimination of the 3rd and 5th harmonics from the output voltage, the THD decreases, which makes the system more reliable for practical applications. The suitable angle for switches for eliminating low-order harmonics are evaluated by the proposed CSA algorithm discussed further.

3.1. Crow search algorithm (CSA) concept

CSA is based on the nature of crow intelligence to search its food. Crow is considered as intelligent as they have largest brain in terms of body-to-brain ratio, they can warn their species for any danger, remember the previous location of food and can take the help of any other crow to steal their food. They have capability of handling complex problems. The working of CSA can be summarized as follows: Considering two crows (C_i) and (C_j) in the population. A constant parameter is defined as the flying capacity of each crow. FC_i represents flying capacity of C_i, in nth iteration. AP is awareness probability. AP_i^n gives the awareness probability of C_i in iteration 'n'. RN_i is a random number for C_i. $L^{i,n}$ shows the current location of C_i in 'n' iteration. The C_i can update its location by using the following steps:

- Step-1: The implementation of algorithm starts with selection of population size and setting of termination conditions. Selecting the number of crow (C_i) in population and maximum number of iteration (Im), a fitness function is evaluated to get value for each crow and stored in the initial memory location. The value of flying capacity and AP is selected. The hiding location is stored in L_i for each crow.
- Step-2: After evaluation of the fitness function the position is updated. This step includes, upgradation of the position of the crow by taking the help of any other crow (C_j) and producing a random value. The upgradation is incorporated by the following equation. $L^{i,n+1}$ is the location of C_i for n+1 iteration.

- Step-3: If the awareness probability (AP) is smaller than this random value than the Crow Ci will follow Cj to know the location of new crow. Fitness function of each crow will be evaluated. It will give the local best solution. $P^{j,n}$ is updated can be updated by using (2).

$$P^{i,n+1} = \begin{cases} L^{i,N} & ; FC_i^{n+1} \; is \; better \; than \; from \; FC_i^n \\ P^{j,n} & ; \qquad otherwise \end{cases} \tag{2}$$

- Step-4: Upgradation of position of crow and testing of solution boundaries. Termination condition is tested. The search by the agent will continue till the termination condition is satisfied. This process will help to find out the required solution within the limit. The flying capacity and awareness probability are also updated.
- Step-5: If the termination condition is satisfied it will return the best position otherwise it will find the nearest best and update the memory location again to improve the exploration and exploitation, flying capacity can be varied by (3) and (4). Where n_{max} gives the maximum number of iteration and n_L gives the current iteration number. FC_i^n and AP will vary linearly in each iteration. The crow will be guided by current location and operator min ($P^{j,n}$) to the nearest best solution.

$$FC_i^n = 2\frac{n_{max}-n_L}{n_{max}} + 0.5 \tag{3}$$

$$AP = 1 - \frac{n_{max}-n_L}{n_{max}} \tag{4}$$

3.2. Implementation of CSA algorithm for proposed MLI

The firing angles are calculated in MATLAB 2020A Simulink environment with the parameters taken in Table 3 using the SHE technique. Different other techniques such as FA, GA, PSO are taken for comparison with proposed CSA based approach. The CSA based SHE is discussed in the earlier section is implemented for generation of suitable switching pulses for proposed MLI. The main target of CSA based SHE is to eliminate the 5th and 7th order harmonics from output.

Table 3. Applied algorithm with their parameters

Applied algorithm	Parameters taken
PSO	Acceleration coefficients C_1, C_2 = 2.0, swarm size = 100, minimum inertia = 0.4 and maximum inertia 0.9, maximum number of iteration 200
FA	Absorption coefficient (l)=1, initial attractive ness (A0) = 0.98, k = 2, c = 0.2, fireflies count=1000, iteration count=200.
GA	Probability of crossover and mutation=0.2 and 0.02, population size=100, generation count = 200
CSA	Initial iteration = 2.5, awareness probability (AP) = 0.2, population size = 100, maximum number of iterations = 200.

The output of seven level inverter shows the odd symmetry thus Fourier series expression of MLI can be shown as follows:

$$V(\omega t) = \sum_{x=1,3,5}^{\infty} V_x \sin(x\omega t)$$
$$V_x = \begin{cases} \frac{4V_{dc}}{x}\left[\cos x\alpha_1 + \cos x\alpha_2\right] & ; for \; odd \; x \\ 0 & ; for \; even \; x \end{cases} \tag{5}$$

with the constraint

$$0 < \alpha_1 < \alpha_2 < \alpha_3 \leq 90$$

where V_x is the magnitude of x^{th} harmonic, ω denotes the fundamental switching frequency, α is taken as switching angle. To get appropriate firing angle the following transcendental equations to be solved:

$$V_1 = \cos\alpha_1 + \cos\alpha_2 + \cos\alpha_3 = 3M \tag{6}$$

$$V_3 = cos\ 3\alpha_1 + \cos 3\alpha_2 + \cos 3\alpha_3 = 0 \tag{7}$$

$$V_5 = \cos 5\alpha_1 + \cos 5\alpha_2 + \cos 5\,\alpha_3 = 0 \quad (8)$$

M=modulation index, 0<*M*<1. To get the appropriate switching angle, the solution of (6)-(8) is obtained with the help of CSA algorithm. The 3rd and 5th order harmonics are targeted to eliminate. To keep the error in limited range and to eliminate 3rd and 5th order harmonics H is taken as 0.1. The objective function for this is defined as

$$OF = \frac{1}{H} * \left[\left|M - \frac{|V_1|}{N_{dc}V_{dc}}\right| + \left(\frac{|V_3|}{N_{dc}V_{dc}}\right) + \left(\frac{|V_5|}{N_{dc}V_{dc}}\right)\right. \quad (9)$$

The CSA is nature inspired algorithm, its steps for calculating firing angle is described through a flow-chart in Figure 3. The flow chart shows the algorithm starts with initialization of required parameters, and followed by evaluation of each search agent and search of best solution. Then the position is updated by updating the awareness probability and flying capacity using (2), (3) to get switching angles. This process is continued till the termination criteria is fulfilled.

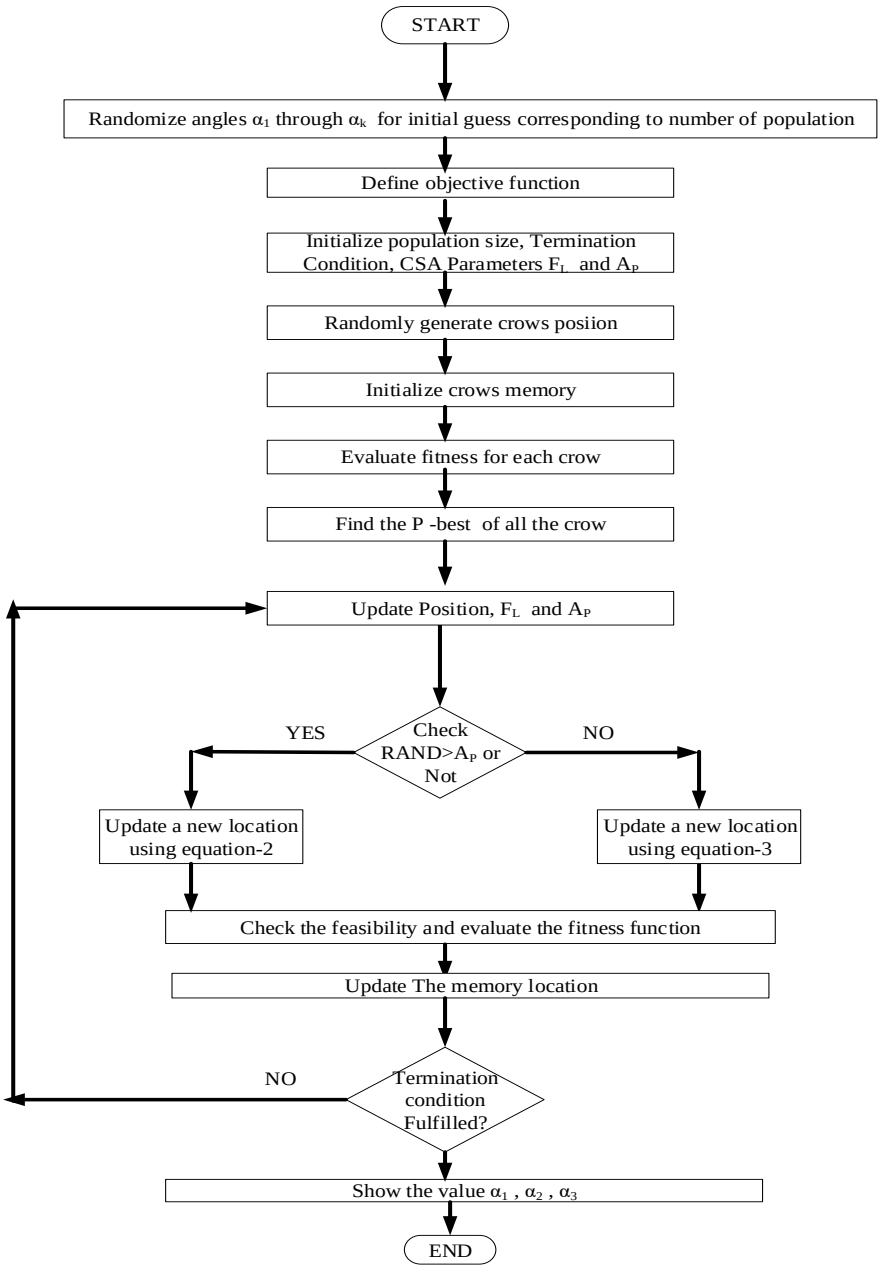

Figure 3. Flow Chart for CSA

3.3. Comparison of CSA with FA, GA, and PSO

The FA and GA and PSO along with CSA are implemented for the same configuration in same environment. The parameters taken for different algorithm is given in Table 3. The switching angle generated with SHE-PWM technique with different algorithm and preserved in look up table in offline. The harmonic spectra obtained in each case is compared in Figure 4. The target is 3rd and 5th harmonics as they are dominant in output. The initial iteration is 2.5 and the maximum population size is chosen 200 (for each algorithm) to compare their proficiency with different M. The THD with the proposed MLI with CSA based harmonic elimination is 10.02 as the 3rd and 5th order harmonic are removed from the output can be observed.

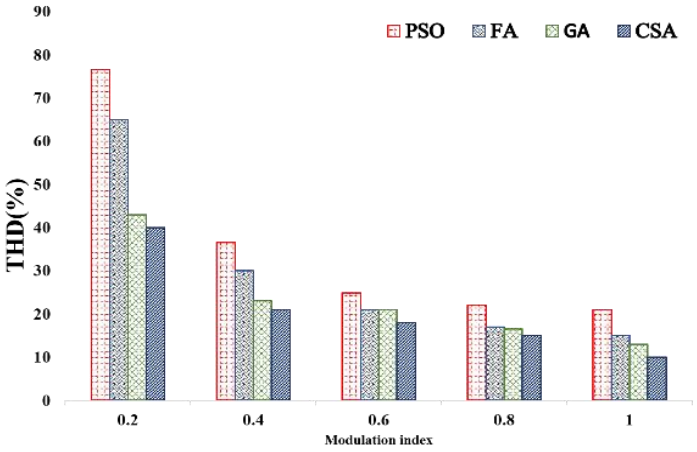

Figure 4. Comparison of THD for 7-level circuit at different modulation index

4. SIMULATION RESULT ANALYSIS

The proposed SC-MLI design's reliability is validated in simulation in MATLAB/Simulink with different test conditions. Seven insulated gate bipolar transistor (IGBT) switches with antiparallel diodes are utilized in the topology. The capacitor value is chosen 2200 µF with minimum voltage ripple consideration [22]. The proficiency of control techniques verified by applying SHE-PWM control using CSA. The switching angles corresponding to *M* values are assessed offline technique and stored in a look up table. The input voltage is varied from V_{DC} = 70 V (from 0 to 0.14 sec) to V_{DC} = 100 V (from 0.14 to 0.18 sec) with M 0.9. It can be verified the output voltage is successfully boosted 1.5 times in Figure 5(a) (see in Appendix) and with resistive load of 40 Ω at M 0.2 in Figure 5(b) (see in Appendix). The output from proposed system is capable to cope up with sudden change in R-L load is verified in Figure 5(c) (see in Appendix). The inductive load is varied from 35 Ω to 70 mH (from 0 to 0.14 sec) to 50 Ω to 250 mH (from 0.14 to 0.18 sec) with M 0.9. The capacitors voltages V_{c1} and V_{c2} are almost equal in both the conditions. A bosting of 1.5 times can be marked in each test condition. The harmonic spectra are analyzed at low M (0.2) as well as at high M (0.9) in Figure 5(d) (see in Appendix) which shows reduced TD at high M and this shows suitable CSA based harmonic elimination. Figure 5(e) (see in Appendix) illustrate the power loss for proposed SC-MLI. The losses are mainly switching loss (P_s), conduction loss (P_c) and capacitor ripple loss (P_{rip}). Power rating is varied by changing the loading. The total power loss is about 9.6 W for 0.2 kW output and 17 W for 0.3 kW power rating. The maximum efficiency evaluated is 96.51%, which may further vary considering different rating devices.

5. EXPERIMENTAL SETUP AND RESULT DISCUSSION

A prototype is further developed in the laboratory as shown in Figure 6(a). The main components are seven IRF540 MOSFETS, TLP250 driver for isolated amplified pulses, Arduino Mega controller and a power quality analyzer. The inverter is operated with 70 V input and 50 Hz output frequency using CSA control scheme.

The required signals to controlling the switches fed from controller circuit (TLP250) based driver circuit. Figure 6(b) shows the 7-level output voltage and capacitor voltages with only resistive load at low value of M (0.2). The results can be analyzed in Figure 6(c) with high M (0.9) which emphasizes the desirability of high M.

The capability to handle effectively to the instant inductive load change can be substantiated in Figure 6(d) physically, as earlier validated from simulation result. The output voltage is also taken in case of sudden frequency change (frequency changed to twice) to encourage the workability at dynamic conditions. The frequency has been changed from 50 to 100 Hz and output shown in Figure 6(e). It can be affirmed in Figure 6(f), that proposed system is capable of removing the 3rd and 5th harmonics as targeted and reduce the THD 10.732 at M 0.9 and at M 0.2 the THD is increased. The analysis is in line with the theoretical findings from CSA and simulation analysis.

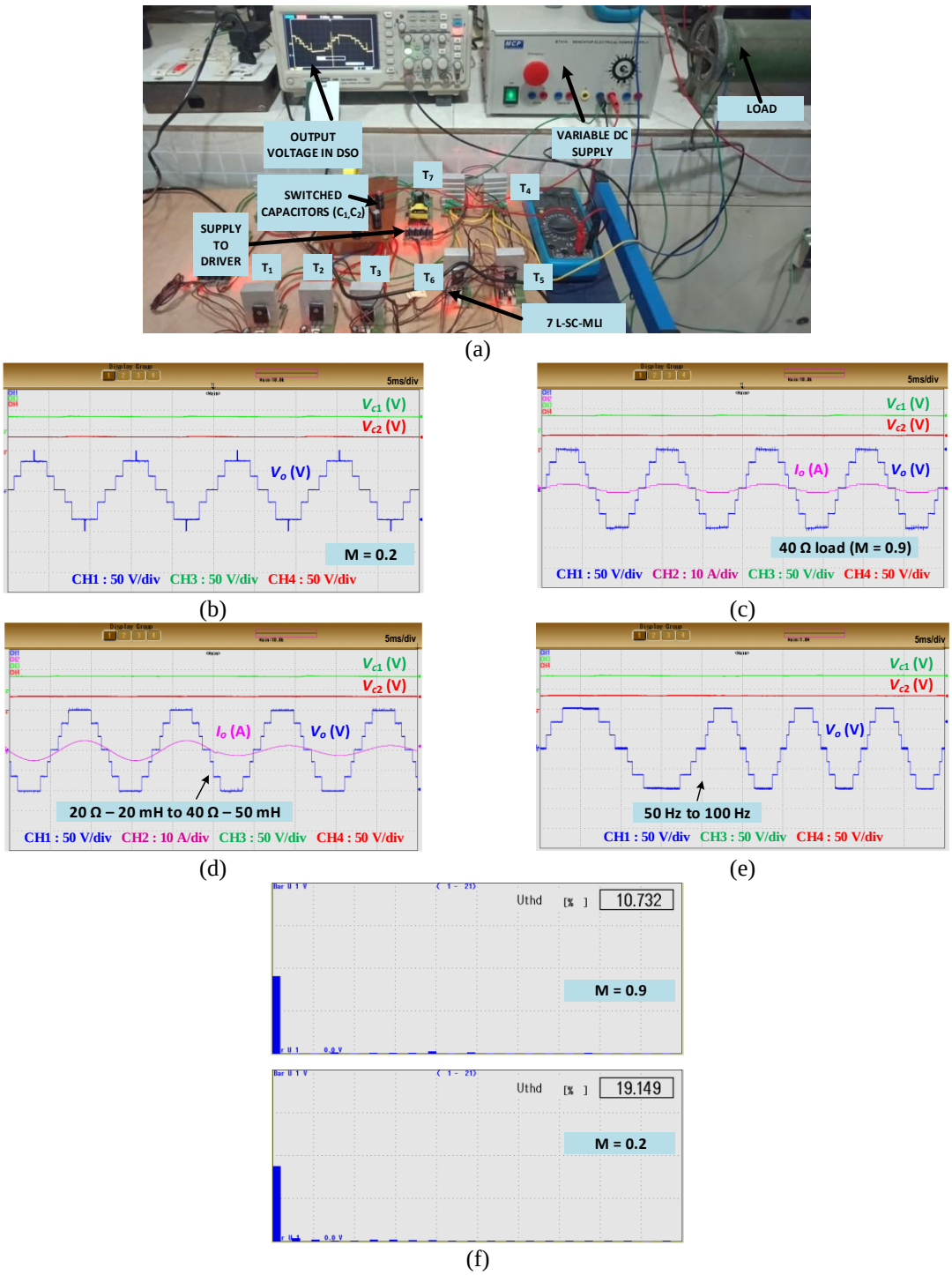

Figure 6. Experimental analysis (a) experimental setup of the proposed MLI, (b) results: output voltage, current and capacitor voltages with low M, (c) with resistive load with high M (0.9), (d) with variation in inductive load, (e) with dynamic frequency change 50 to 100 Hz, and (f) THD analysis with low and high M

6. CONCLUSION

This work introduced a 7-level SC-MLI that can be seen as a sustainable solution for the implementation of it with a stand-alone PV system. With this system, the output from the source can be increased 1.5 times using 7 switches. This results in a low-cost solution for remote areas. The TSV and cost factor are analyzed with existing topologies validates the effectiveness of new structure presented in this work. The suitable switching angles are evaluated by the CSA-based SHE algorithm. The reduction of THD compared with other algorithms such as PSO, FA, and GA are justified. The voltage quality is improved with CSA-SHE, i.e., the harmonic analysis is carried out by for low and high modulation index shows reduced THD at high modulation value. The suggested scheme is tested under different loading conditions with different loads. The 3rd and 5th harmonic components are successfully eliminated by CSA based SHE technique. The output has been taken out in various dynamic condition in simulation environment as well as in experimental test setup in laboratory that shows the feasibility of working with the emerging optimization technique.

APPENDIX

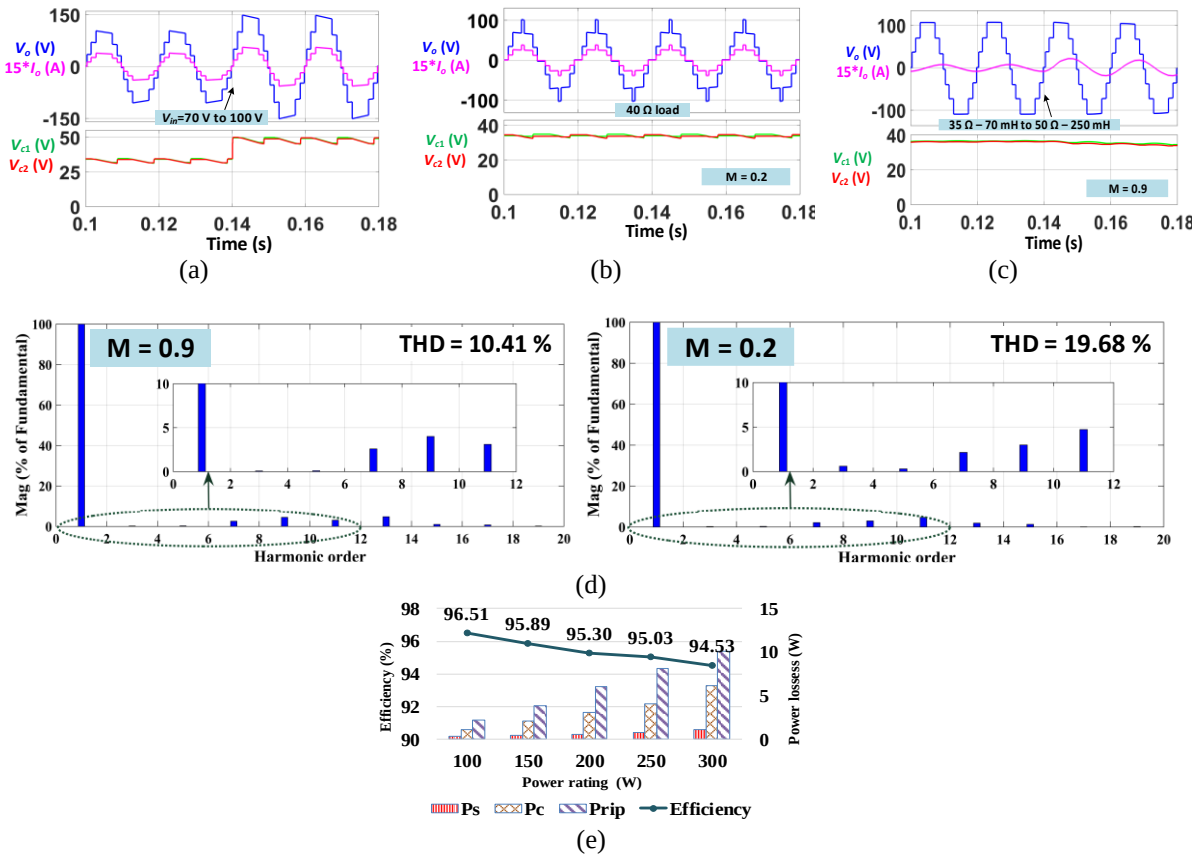

Figure 5. Simulation results for developed system: output voltage, current and capacitor voltages (a) with variation of input voltage, (b) with resistive load with M (0.2), (c) with variation in inductive load (d) THD analysis with high and low M, and (e) power loss and efficiency evaluation

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