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The optimization of a GaN-based current aperture vertical electron transistor

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ABSTRACT

The main objective of this paper is to simulate and optimize a current aperture vertical electron transistor (CAVET) based on gallium nitride (GaN), which combines both a two-dimensional electron gas (2DEG) and a vertical structure using the SILVACO-TCAD simulator. The dimensions of the structure were reduced by 45% to minimize the size and improve the performances of the proposed device; also, a part of aluminum nitride (AlN)was added to the current blocking layer (CBL) to modulate the conduction band profile. The results obtained from the simulation of our structure demonstrated a maximum drain current of 1.8 A/mm, Pinch-off voltage (V_P) of -6 V, drain induced barrier lowering (DIBL) of 166 mV/V, maximum transconductance (g_m) of 570 mS/mm, gate-leakage of 7.10^{-7} A, cut-off frequency (f_t) of 200 GHz, maximum oscillation frequency (f_{Max}) of 400 GHz. The proposed device exhibited outstanding performance while consuming low power, making it well-suited for use as a low-noise amplifier (LNA) in satellite reception applications.

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1. INTRODUCTION

Gallium nitride (GaN) is the preferred material for high power electronic devices due to its high critical electric field, high electron mobility, and its large band gap [1]. Due to its exceptional properties, such as a high breakdown field, high power density, and high mobility of the channel electron (2-DEG), thehigh electron mobility transistor (HEMT) with GaN is extensively used in high-power and high-frequency applications. This channel is created by the difference in the polarization of charges at the AlGaN/GaN heterostructure [2]. Most of GaN power devices have been in lateral geometry, however studies have shown that the vertical GaN geometry is preferable compared to the lateral, because of several advantages including the ease of packing, reduction of chip surface, mitigation of direct current-radio frequency (DC-RF) dispersion because the high field regions can be buried under the gate electrode, and high breakdown voltage [3].

Several vertical structures have been suggested and demonstrated, including current aperture vertical electron transistors (CAVETs) [4], [5], junction field-effect transistor (JFETs), trench metal-oxide semiconductor field-effect transistor (MOSFETs) [6], [7], fin power FETs, and GaN interlayer based vertical trench MOSFET (OG-FETs) [8]. Among these structures, the vertical GaN HEMT using a CAVET like structure is the subject of our study. CAVET, or a capacitively-coupled normally-off AlGaN/GaN HEMT vertical transistor, is a transistor that includes a narrow aperture filled with a conducting material, separating the source and the drain, with an insulating layer in between. The source is comprised of a two-dimensional

electron gas (2DEG) generated in the GaN material near the AlGaN/GaN heterointerface, while the drain is made up of n-type GaN [9]. A current blocking layer (CBL) prevents electrons from passing through the aperture in a CAVET device. In this device, source contacts are deposited on each edge of the aperture while the drain metal is bonded to the n-doped region situated below the aperture.

The electrons flow vertically from the source through the 2DEG towards the drain, but they cannot pass through the aperture due to the CBL's presence. The CBL is responsible for preventing the flow of current through any path other than the aperture, ensuring that the current passes through the desired channel.The gate, which is located above the aperture, is of the Schottky type and is responsible for modulating the charge in the 2DEG. This modulation of charge in the 2DEG enables control over the amount of current that passes through the aperture and flows into the drain [10].

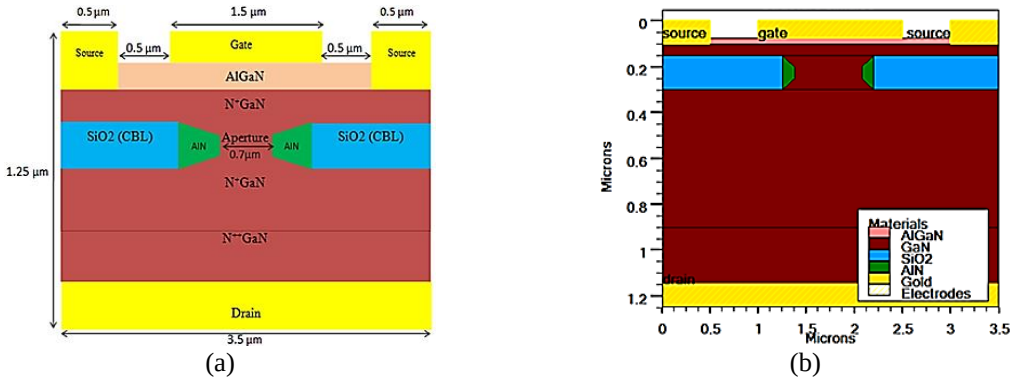
Recently, high-power devices based on the GaN CAVET structure have shown significant progress [11] in power and microwave applications. These applications are part of the field of radio frequencies (RF), where the useful signal is conveyed by a transmitter-receiver transmission chain. The low noise amplifier (LNA) is an electronic circuit which constitutes the head amplifier of a reception chain. Its role is to amplify the power of the RF signal and to eliminate any foreign signal (noise) disturbing the useful signal. The LNA is one of the basic functional blocks in communications systems. These performances are closely linked to the transistors which constitute it [12]–[16].

In this paper, we analyze a DC and AC performances of CAVET based on GaN including maximum drain current (I_{Max}), pinch-off voltage (V_P), drain induced barrier lowering (DIBL), maximum transconductance (g_m), gate-leakage, cut-off frequency (f_t), maximum oscillation frequency (f_{Max}) and capacity. This is by reducing the size of the design to obtain excellent properties with minimal side effects, and adding a part of nitrate of aluminum (AlN) into the current blocking layer (CBL) to modulate the conduction band energies and supress the leakage current. Our device was simulated using Silvaco ATLAS program.

2. STRUCTURE AND MODELLING

The schematic cross section of our structure is shown in Figure 1. It consists of a buffer layer (GaN) heavily doped to ensure good ohmic contact with n- doping concentration of $3e^{20}$ cm^{-3} and a thickness of 0.25 µm, a thick drift layer (GaN) weakly doped which provides high V_{BR} in the reverse direction [17], with n-doping concentration of $1e^{18}$ cm^{-3} and a thickness of 0.6 µm, followed by a current blocking layer (CBL) and an aperture introduced into the structure. The aperture layer (GaN) with n-doping concentration of $1e^{18}$ cm^{-3}, thickness of 0.15 µm and width of 0.7 µm, all others geometrical dimension is in Figure 1(a).The current blocking layer (CBL) is an insulating region assures a direct vertical current passage by any other path except from the source contacts via the 2DEG at the AlGaN/GaN heterostructure to the drain without gate control, it is formed by the SiO_2 party and the part of aluminum nitride or AlN (the proposed device's conduction band profile is modulated by AlN material) [18].

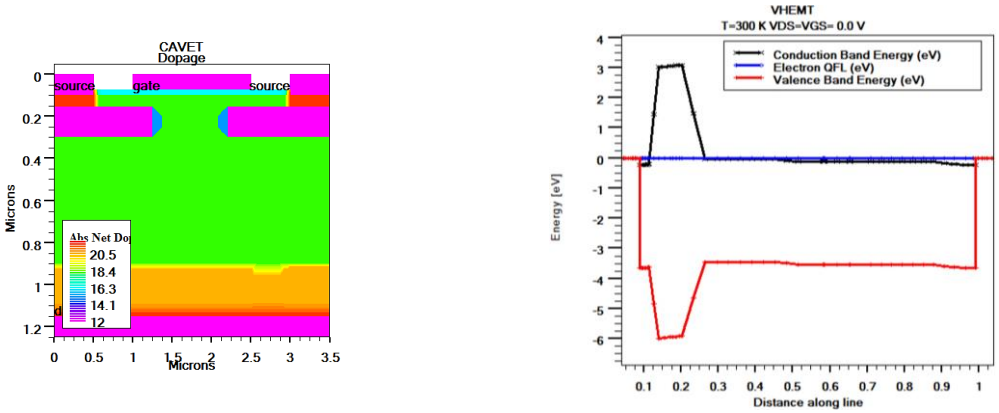
This is followed by a channel (GaN) and a barrier layer (AlGaN) which allows the formation of 2DEG, the channel layer (GaN) lightly doped with n-doping concentration of $1e^{18}$ cm^{-3} and thickness of 0.05 µm, the barrier layer (AlGaN) with a thickness of 0.025 µm and the total composition is 24%. The gate electrode is a Schottky contact, the source and drain electrodes are ohmic. The metal used for these two contacts is gold (Au). The gate length is 1.5 µm and the spacing between the source and the gate is 0.5 µm in both sidesare mention in Figure 1(b).



(a) (b)

Figure 1. Schematic 2D of the proposed CAVET (a) the longitudinal section of the device and (b) 2D structure in TCAD-Silvaco

The doping profile of the structure obtained by Silvaco tools is presented in Figure 2(a). The red color designates the heavily doped regions, and the weakly doped regions with the purple color. Doping is used in this work under the drain and sources electrodes with a concentration of 1.10^{21} cm^{-3}. The importance of this high doping is to simulate the diffusion of electrons in the semiconductor and to achieve very good ohmic contacts. In Figure 2(b), the energy band diagram of the structure is shown, with the conduction and valence band energies plotted as a function of depth from the surface along the vertical direction of the structure. The potential well is created due to the presence of a heterojunction at the interface of AlGaN and GaN materials. AlGaN, being a large gap material, and GaN, being a small gap material, create a discontinuity in the conduction profile at their interface, resulting in the formation of a potential well. This potential well is responsible for creating the two-dimensional electron gas (2DEG). Figure 2(b) also shows that the height of the conduction band energy reaches 2.5 eV, the presence of AlN in the CBL of the structure results in an increased electronic barrier height, which effectively reduces vertical leakage through the CBL at higher drain bias. This phenomenon is described in more detail in reference [19].



(a) (b)

Figure 2. Doping and band parameter variable in CAVET device (a) divide of the doping in the structure area and (b) diagram band of the vertical cutting structure in the device

3. RESULTS AND DISCUSSION

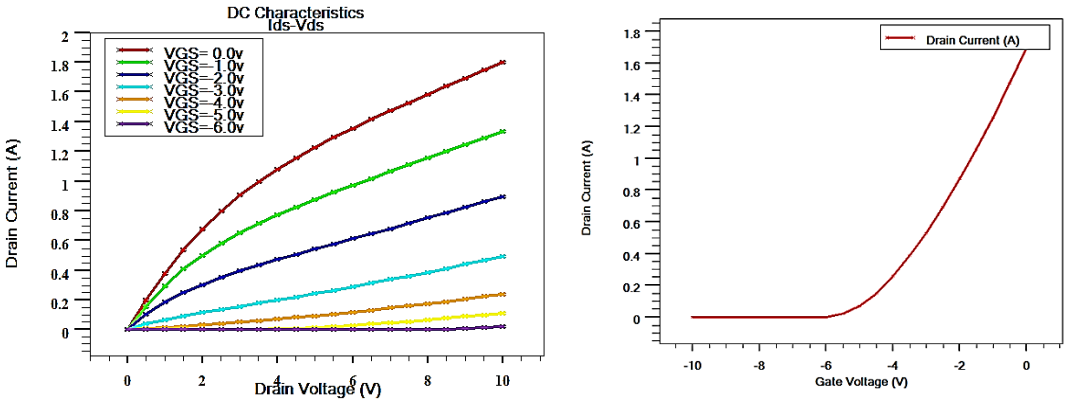
3.1. DC analysis

Figure 3(a) presents the output characteristic of our AlGaN/GaN CAVET, the characteristic curve plots the I_{DS} current as a function of the V_{DS} voltage, while varying the gate-source control voltage V_{GS} from 0 to -6 V, over the range of the V_{DS} from 0 to 10 V. The I_{DS} reach a maximum value of 1.8 A at V_{GS} = 0 V. As the gate-source control voltage becomes more negative, the I_{DS} current decreases due to the lowering of the Fermi level with respect to the energies involved in the channel, which in turn reduces the electron density in the channel and leads to a decrease in I_{DS} current. At the threshold voltage V_{TH}, the drain-source current becomes zero. The I_{DS} current does not reach saturation especially at low values of V_{DS}, because the aperture is not sufficiently conductive which will maintain the applied voltage [20].

Figure 3(b) presents the transfer characteristic I_{DS} (V_{GS}), this plot illustrates how the I_{DS} varies with respect to the V_{GS}, while the V_{DS} is held constant at 10 V. From the linear plot of this characteristic, the pinch-off voltage can be determined, which is the V_{GS} control bias needed to pinch the electron gas and empty the potential well. For a V_{DS} of the 10 V, the threshold voltage V_{TH} extracted from plot is -5.8 V and the pinch voltage V_P is of the order of -6 V, we identified it at this value by fixing the doping of the channel layer at 1×10^{18} cm^{-3}, and the length of the aperture region at 1 µm because our device is widely used in high frequency and high-power applications.

In Figure 4, the I_{DS} is plotted against the gate voltage for two different drain-source voltage (V_{DS}) values: 1 V and 10 V. Increasing the V_{DS} reduces the potential barrier between the source and the channel, especially when they are in close proximity. Drain induced barrier lowering (DIBL) is among the necessary parameters that indicate the quality of the device. This parameter is crucial for determining the behavior of short-channel transistors at high drain voltages, and is primarily utilized in digital applications. Its value is estimated by the ratio between the variation of the threshold voltage (V_{TH}) and the variation of the drain-source voltage (V_{DS}) [$\Delta V_{TH}/\Delta V_{DS}$] [21]. Table 1 shows how to calculate the value of DIBL; the threshold voltages obtained by extraction are -4.5 V and -6 V, respectively for the drain-source voltages of 1.0 V and

10 V. We find a DIBL of the 166 mV/V is a good value in our study, despite it a bit considerable compared to the values found in the lateral transistor, this is caused by the short channel effects (SCE), in addition to the miniaturized size of the design and its vertical structure.



(a) (b)

Figure 3. I–V characteristics: (a) I_{DS} as a function of the V_{DS} for different bias of the V_{GS} and (b) I_{DS} as a function of the V_{GS} at V_{DS} = 10 V

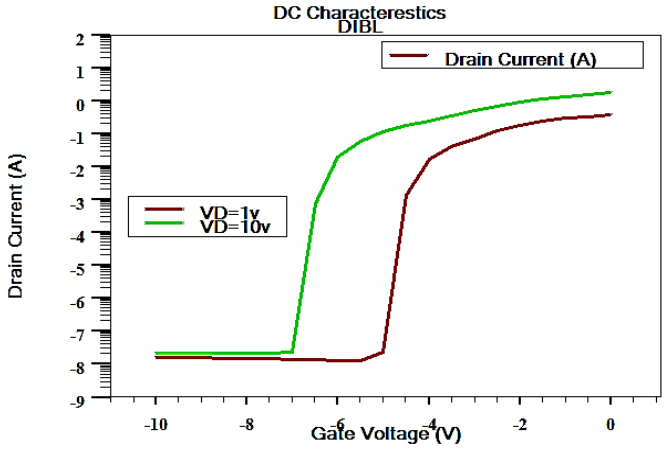


Figure 4. Drain current as a function of gate voltage for V_{DS} = 1 V and 10 V

Table 1. DIBL calculation for device

Drain-source voltage(V)	Tension de seuil V_{TH}(V)	DIBL (mV/V)
1 V	-4.5	DIBL=abs$\left[\frac{\Delta V_{TH}}{\Delta V_{DS}}\right]$ =
10 V	-6	abs $\left[\frac{-1.5}{9}\right]$DIBL=166mV/V

Figure 5(a) presents the transconductance for a V_{DS} fixed at 10 V. Transconductance refers to the change in I_{DS} that occurs in response to a change in V_{GS}, while maintaining a constant V_{DS}. For a voltage V_{DS} equal to 10 V; we notice that gm increases with V_{GS} to reach its maximum value which is about 570 mS/mm. This large value means that we have good control of gate on the channel. The total leakage current in a CAVET is composed of three paths, leakage through the CBL, leakage from the gate, and the leakage of electrons that flow from the source through the aperture beneath the two-dimensional electron gas (2 DEG) to the drain without gate modulation [22].

Figure 5(b) shows gate leakage current plotted in logarithmic scale as a function of the V_{GS}. This V_{GS} is varied from -10 to 2 V while keeping the V_{DS} constant at 10 V. In any transistor configuration, it is

necessary that the off-state leakage current be reduced to a minimum. We notice from Figure 5(b) that the device gives an invariant leakage current with the polarization of the gate, it is of the order of 7×10^{-7} A. According to Yaacov *et al*. [23], the presence of a depression in the surface beneath the gate leads to an increase in electric fields, which in turn causes the observed leakage value. It is a low value allows minimizing the consumption, and it indicates the good quality of the simulated device.

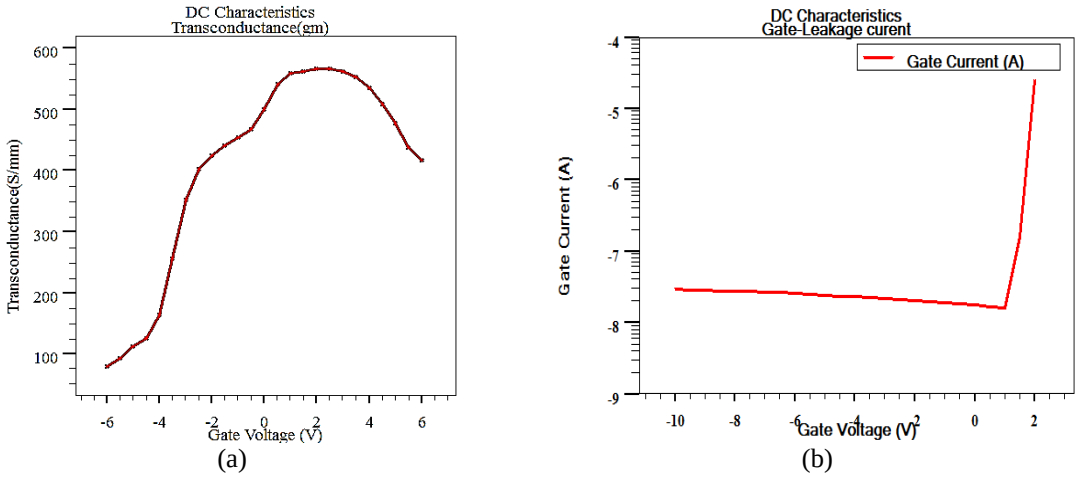


Figure 5. DC characteristics on the (a) transconductance and (b) gate leakage current

3.2. AC analysis

Figure 6(a) presents the evolutions of the gains as function of the frequency which are calculated for V_{DS} = 10 V and V_{GS} = 0 V. The current gain (H_{21}), unilateral power gain (G_T), the maximum stability gain (GMS) and the maximum available gain (GMA) are the most important in determining the microwave performance of the transistor. We calculate the gains when the CAVET becomes stable that is to say in the frequencies where the stability factor is greater than 1.The stability factor is shown in Figure 6(b), in the first is greater than 1 from 200 GHz. The maximum current gain is equal to 165 dB, up to a frequency of 1 kHz. The unilateral power gain has a maximum value equal to 80 dB. The transition frequency (f_t) is 200 GHz. The maximum oscillation frequency (f_{Max}) is around 500 GHz. The maximum values of the stable gains are of the order of 85 dB. While, Figure 7 shows the transconductance as a function of frequency. The figure shows that the transconductance is the same until it reaches the resonance frequency. It degrades to a minimum value of 110 mS/mm.

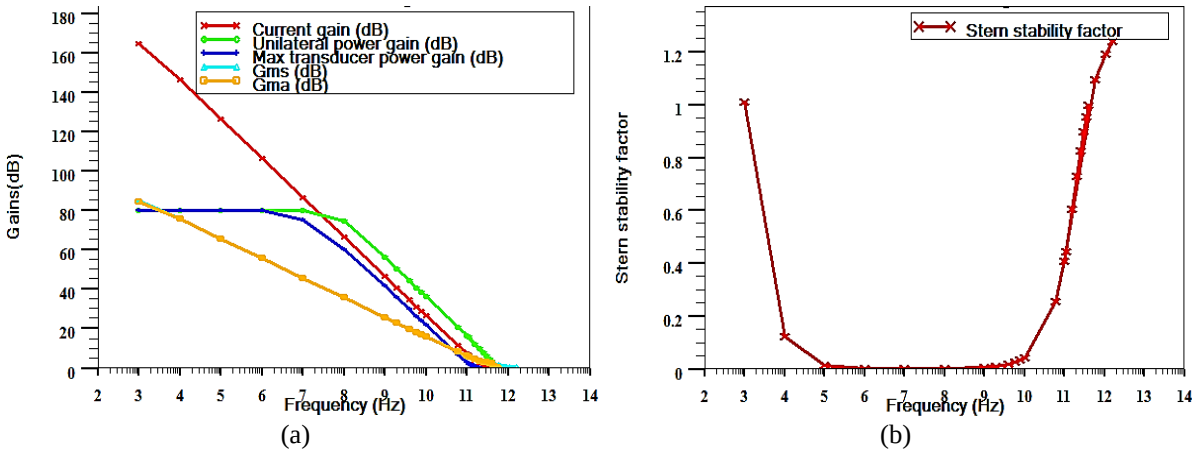


Figure 6. AC characteristics at V_{GS} = 0 V and V_{DS} = 10 V as a function of frequency on the (a) characteristics of gains and (b) stability factor

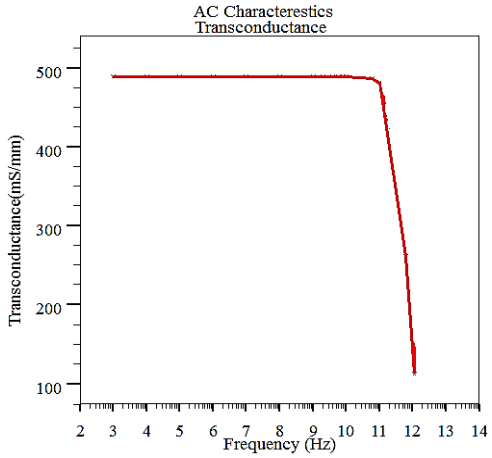


Figure 7. Transconductance as a function of frequency

3.3. Capacities analysis

Figure 8(a) shows the variation of the gate-drain (C_{GD}), gate-source (C_{GS}) and drain-source (C_{DS}) capacitances as a function of the gate-source voltage. We know that capacitance is the ability of a material to store electrical charge. The power consumed in the transistor could be reduced by such a capacity. The C_{GS} and C_{GD} capacitances represent the variations of the charge accumulated in the space charge zone below the gate. C_{GS} determines this variation modulated by the voltage V_{GS} for a constant voltage V_{GD}; C_{GD} also determines the variation of the charge accumulated in the deserted zone, located under the gate modulated by the voltage V_{GD} for a constant voltage V_{GS}. The figure shows that C_{GD} Capacity is practically the same regardless of the value of V_{GS}; it is of the order of the 9 pF/µm. For the C_{GS} capacity, in the off state, the capacitance is of the order of 0.8 pF/µm. For $V_{GS} \geq V_{GS0}$, C_{GS} increases from the 0.8 pF/µm up to 9 pF/µm it saturates. For the C_{DS} capacity which is the overall device capacity, in the blocked state, the capacitance is of the order of 0.1 pF/µm, for $V_{GS} \geq V_{GS0}$, C_{DS} decreases up to 9 fF/µm to start a rapid growth up to 0.5 pF/µm after it saturates.

Figure 8(b) presents the variation of all capacitances as a function of frequency. The figures show that C_{GD} capacitance is practically the same regardless of the frequency. After the transition frequency, which is 200 GHz, the C_{GS} and C_{DS} capacities decrease until reaching their minimum values which are respectively 0.5 pF/µm and 3 fF/µm.

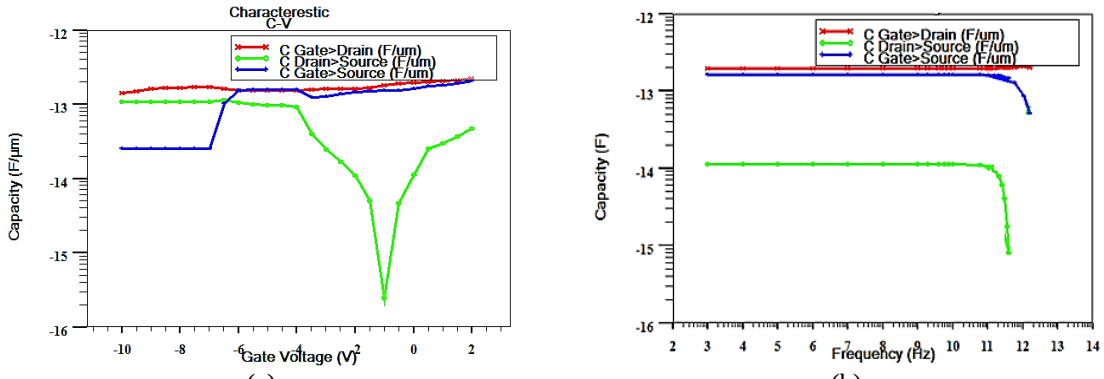


Figure 8. Capacities characteristics on the (a) gate-drain, gate-source, drain-source capacitance as a function of the V_{GS} and (b) capacitances as a function of frequency

3.4. Results comparison

Table 2 presents the data from the literature study of a CAVET with different performances exhibited. After a thorough review and comparison, all of these works are dedicated to presenting an

approach that highlights the major developments in this field, particularly in activities aimed at enhancing RF performance. The characteristics of the proposed device make it exceptionally well-suited for demanding high-power and high-frequency applications in challenging environments.

Table 2. Comparison of the results obtained with recent published works

	[24]	[25]	[26]	This work
I_{Dss} [A]	0.25	0.97	1.0	1.8
V_P [V]	-3.4	-6.0	2.5	-6.0
Gm [S/m]	//	0.26	0.83	0.57
f_T [GHz]	34.5	24.3	32.4	200
f_{Max} [GHz]	125	55.2	38.2	500
Gains [dB] @ 100 GHz	34.2	17.5	//	45
C_{DS} [pF]	//	32	//	9.8
C_{GS} [pF]	//	38	400	10.2

4. CONCLUSION

In this work, a miniaturized current aperture vertical electron transistor (CAVET) based on GaN was proposed, and its DC, AC, and capacitance performances were investigated using the TCAD SILVACO Tools simulator. The results demonstrate that a device with smaller dimensions not only delivers better performances and high efficiency. It is also exhibiting a promising potential for advancing technological solutions in high-power applications.

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REFERENCES

[1] N. M. Shrestha, Y. Y. Wang, Y. Li, and E. Y. Chang, "A novel AlGaN/GaN multiple aperture vertical high electron mobility transistor with silicon oxide current blocking layer," *Vacuum*, vol. 118, pp. 59–63, 2015, doi: 10.1016/j.vacuum.2014.11.022.

[2] S. Kim and K. Yang, "Enhanced Breakdown Characteristic of AlGaN/GaN HEMTs Using a Gate/Drain Double Field-Plate Structure," *Extended Abstracts of the International Conference on Solid State Devices and Material*, pp. 208–209, 2005.

[3] N. M. Shrestha, Y. Li, and E. Y. Chang, "Simulation study on electrical characteristic of AlGaN/GaN high electron mobility transistors with AlN spacer layer," *Japanese Journal of Applied Physics*, vol. 53, no. 4 SPEC. ISSUE, 2014, doi: 10.7567/JJAP.53.04EF08.

[4] S. Chowdhury, B. L. Swenson, and U. K. Mishra, "Enhancement and Depletion Mode AlGaN/GaN CAVET With Mg-Ion-Implanted GaN as Current Blocking Layer," *IEEE Electron Device Letters*, vol. 29, no. 6, pp. 543–545, Jun. 2008, doi: 10.1109/LED.2008.922982.

[5] D. Shibata *et al.*, "1.7 kV/1.0 mΩcm 2 normally-off vertical GaN transistor on GaN substrate with regrown p-GaN/AlGaN/GaN semipolar gate structure," in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2016, pp. 10.1.1-10.1.4. doi: 10.1109/IEDM.2016.7838385.

[6] T. Oka, T. Ina, Y. Ueno, and J. Nishii, "1.8 mΩ·cm 2 vertical GaN-based trench metal–oxide–semiconductor field-effect transistors on a free-standing GaN substrate for 1.2-kV-class operation," *Applied Physics Express*, vol. 8, no. 5, p. 054101, May 2015, doi: 10.7567/APEX.8.054101.

[7] R. Li, Y. Cao, M. Chen, and R. Chu, "600 V/ 1.7 Ω Normally-Off GaN Vertical Trench Metal–Oxide–Semiconductor Field-Effect Transistor," *IEEE Electron Device Letters*, vol. 37, no. 11, pp. 1466–1469, Nov. 2016, doi: 10.1109/LED.2016.2614515.

[8] D. Ji, W. Li, and S. Chowdhury, "A Study on the Impact of Channel Mobility on Switching Performance of Vertical GaN MOSFETs," *IEEE Transactions on Electron Devices*, vol. 65, no. 10, pp. 4271–4275, 2018, doi: 10.1109/TED.2018.2864260.

[9] D. Ji *et al.*, "Normally off Trench CAVET with Active Mg-Doped GaN as Current Blocking Layer," *IEEE Transactions on Electron Devices*, vol. 64, no. 3, pp. 805–808, 2017, doi: 10.1109/TED.2016.2632150.

[10] R. Yeluri *et al.*, "Design, fabrication, and performance analysis of GaN vertical electron transistors with a buried p/n junction," *Applied Physics Letters*, vol. 106, no. 18, 2015, doi: 10.1063/1.4919866.

[11] H. S. Kang, J. H. Seo, Y. J. Yoon, M. S. Cho, and I. M. Kang, "DC and RF analysis of geometrical parameter changes in the current aperture vertical electron transistor," *Journal of Electrical Engineering and Technology*, vol. 11, no. 6, pp. 1763–1768, 2016, doi: 10.5370/JEET.2016.11.6.1763.

[12] A. M. Abdelmonem, A. S. I. Amar, A. Almslmany, I. L. Abdalla, and F. A. Farag, "Design and implementation of a broad-band high gain low noise amplifier for 3G/4G applications," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 23, no. 2, pp. 725–732, 2021, doi: 10.11591/ijeecs.v23.i2.pp725-732.

[13] A. B. Ibrahim, C. Z. Zulkifli, S. A. Ariffin, and N. H. Kahar, "High frequency of low noise amplifier architecture for WiMAX application: A review," *International Journal of Electrical and Computer Engineering*, vol. 11, no. 3, pp. 2153–2164, 2021, doi: 10.11591/ijece.v11i3.pp2153-2164.

[14] S. A. Z. Murad, A. Azizan, and A. F. Hasan, "Ultra-low power 0.45 mw 2.4 ghz cmos low noise amplifier for wireless sensor networks using 0.13-µm technology," *Bulletin of Electrical Engineering and Informatics*, vol. 9, no. 1, pp. 396–402, 2020, doi: 10.11591/eei.v9i1.1852.

[15] L. T. Phuong, B. Journet, and D. B. Gia, "Design and fabrication of A Ku-band low noise amplifier using FR-4 substrate," *Telkomnika (Telecommunication Computing Electronics and Control)*, vol. 18, no. 1, pp. 552–561, 2020, doi: 10.12928/TELKOMNIKA.v18i1.13196.
[16] M. Muhamad, H. Hussin, and N. Soin, "Design of 130nm RFCMOS differential low noise amplifier," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 19, no. 1, p. 172, 2020, doi: 10.11591/ijeecs.v19.i1.pp172-177.
[17] W. J. Witte, "Building blocks of vertical GaN-based devices," 2015. [Online]. Available: https://publications.rwth-aachen.de/record/484115/files/484115.pdf
[18] S. A. Loan, S. Verma, A. G. Alharbi, and A. M. Murshid, "Polarization engineered enhancement mode high breakdown voltage GaN CAVET," *2017 9th IEEE-GCC Conference and Exhibition, GCCCE 2017*, 2018, doi: 10.1109/IEEEGCC.2017.8447991.
[19] Z. Zhao, J. Du, Z. Zhao, and Q. Luo, "A novel high-voltage GaN current aperture vertical electron transistor with polarization-doped current blocking layer," *Nanoscience and Nanotechnology Letters*, vol. 6, no. 9, pp. 825–829, 2014, doi: 10.1166/nnl.2014.1866.
[20] S. Chowdhury and U. K. Mishra, "Lateral and vertical transistors using the Algan/GAN Heterostructure," *IEEE Transactions on Electron Devices*, vol. 60, no. 10, pp. 3060–3066, 2013, doi: 10.1109/TED.2013.2277893.
[21] A. Belarbi and A. Hamdoune, "Numerical simulation and comparative assessment of DG-HEMT device for high-frequency application," *International Journal of Nanoelectronics and Materials*, vol. 12, no. 1, pp. 93–104, 2019.
[22] S. Chowdhury, M. H. Wong, B. L. Swenson, and U. K. Mishra, "CAVET on bulk GaN substrates achieved with MBE-regrown AlGaN/GaN layers to suppress dispersion," *IEEE Electron Device Letters*, vol. 33, no. 1, pp. 41–43, 2012, doi: 10.1109/LED.2011.2173456.
[23] I. Ben-Yaacov, Y. K. Seck, U. K. Mishra, and S. P. DenBaars, "AlGaN/GaN current aperture vertical electron transistors with regrown channels," *Journal of Applied Physics*, vol. 95, no. 4, pp. 2073–2078, 2004, doi: 10.1063/1.1641520.
[24] H. Ahn, H. Ji, D. Kang, S. M. Son, S. Lee, and J. Han, "A 26–30 GHz GaN HEMT Low-Noise Amplifier Employing a Series Inductor-Based Stability Enhancement Technique," *Electronics (Switzerland)*, vol. 11, no. 17, 2022, doi: 10.3390/electronics11172716.
[25] A. Danielraj, S. Deb, A. Mohanbabu, and R. S. Kumar, "The impact of a recessed Δ-shaped gate in a vertical CAVET AlGaN/GaN MIS-HEMT for high-power low-loss switching applications," *Journal of Computational Electronics*, vol. 21, no. 1, pp. 169–180, 2022, doi: 10.1007/s10825-021-01816-2.
[26] N. Zeng, Y. Yin, K. Li, F. Liao, and H. Huang, "Polarization doping modulated heterojunction electron gas in AlGaN/GaN CAVETs," *Semiconductor Science and Technology*, vol. 35, no. 9, 2020, doi: 10.1088/1361-6641/aba0cb.

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