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Simulation model development and experimental validation of a PFC converter

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ABSTRACT

The most common interface to the electric grid of small power loads, which is based on a diode bridge followed by a bulk capacitor, generates a large number of low-frequency harmonics in the input current. To comply with the IEC 61000-3-2 and IEEE 519 standards it is needed to optimize the interface in terms of current harmonics and the topology composed by a diode bridge and a DC/DC boost converter operating in the critical conduction mode is one having a greater number of comparative advantages. There is a large number of controllers in the market but also a lack of the associated simulation models exists. This paper focuses on the development, validation and testing of a simulation model that mimics an existing integrated circuit and allows for an accurate prediction of the real behavior of the complete converter. The experimental results validate the model with high fidelity and confirm the added value of the topology and control method applied either in transient and steady-state operation.

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1. INTRODUCTION

Small electric power loads, i.e. less than 200 W, are connected to the public power grid through simple diode bridges with a bulk capacitor at the output but they can cause various problems, initially raised in research [1] and, more recently, in [2]. These problems implied the appearance of standards (IEC 61000-3-2 and IEEE 519) that establish different limits for certain characteristics, in particular with regard to current harmonics. On the other hand, the emergence of new semiconductors turned possible to improve some parameters of these interface converters. Thus, the widespread adoption of electronic switches based on silicon carbide (SiC) and/or gallium nitride (GaN) semiconductors, allowed for new and better solutions [3], [4]. Increased performance and reduced size are always important objectives in the design of a switched mode power supply, especially with regard to energy savings, greater portability, and a smaller environmental footprint.

Compliance with the referred standards and specifications led to the development of interfaces based on different topologies, e.g. semi-bridgeless or bridgeless referred, among others, in [5]–[7], and containing active devices in order to be able to adequately control the input current and increase the efficiency, as analyzed in [8] and [9]. The different topologies are distinguished by several parameters: the number of controlled semiconductors they use, the size and type of passive components, i.e., inductors and capacitors [10]–[13], the voltage gain. Some aspects of electromagnetic interference (EMI) are also different depending on the topology, as reported in [8]. In the low power range, all solutions comply well with the standards and do not present relevant issues regarding the currents (as they are small) that active and passive elements of the topology must

support. In this power range, and particularly for light emitting diode (LED) driving, the boost integrated fly back rectifier with energy storage (BIFRED) topology with only one controlled MOSFET is a successful topology [14].

To control these power factor correction (PFC) converters there are several control architectures, all of them using the same structure: outer output voltage control loop; inner current control loop; synchronization with the grid voltage. However, there are some additional control approaches that do not use any kind of synchronization with the grid voltage, namely the discontinuous conduction mode and the one-cycle control method [15]. Also, the versatile power balanced control is used in research [16] to directly obtain a voltage gain lower than one without synchronization and using a buck-boost DC/DC converter while keeping a small device count.

Several integrated circuits (ICs) have appeared on the market implementing, although in a different way, the control requirements for this interface. Interfaces based on bridgeless topologies, require other control methods, slightly different from those applied to diode bridge-based solutions [6], [8], [13], [17]. In the same way, there are integrated circuits on the market dedicated to the control of some variants of the bridgeless solution. In addition to these, the most modern solutions are based on dedicated microcontrollers such as those from NXP, Infineon and STMicroelectronics.

An accurate simulation model of a control circuit as well as of the power circuit is a helpful tool mainly when used in conjunction with the design guidelines provided by the integrated circuit (IC) manufacturer for predicting the converter behavior in different steady-state and transient conditions. However, simulation models of most control ICs are not freely available and turn difficult to obtain a prior knowledge (based on simulation studies) related to the converter performance. The performance indicators considered most relevant in this work are the alternating current (AC) distortion and the output voltage dynamics, [11]; they directly interfere in the quality of the AC interface [17], and in the requirements of the direct current (DC) stage where they are connected to.

In this paper it is developed a simulation model based on one IC block diagram and the topology based on diode bridge followed by a boost converter and controlled in the critical conduction mode (CRM). This helps the designer and allows a faster development of the complete converter. The rest of the paper is organized as: i) Section 2 discusses methods for converter design and modelling; ii) Section 3 explains how the simulation model is developed and the parameters used for validation and testing; iii) Section 4 presents the most relevant simulation results related to the issues analyzed in the work and demonstrates, with an experimental set-up using the same parameters employed in simulation, the model accuracy and its performance. The section also discusses available options and additional related features; and iv) Section 5 outlines the relevant conclusions of the work.

2. CONVERTER DESIGN AND MODELING APPROACH

The PFC converter's control system is designed in order to fulfill the following main requirements: fast output voltage dynamics with limited voltage ripple; current controller imposing nearly sinusoidal AC current, with minimal zero crossing distortion and negligible higher order harmonics, and unitary power factor; compensation for variable magnitude of the AC voltage. Almost all existing controllers in the market satisfy these requirements, based on analog and/or mixed-signal ICs. However, simulation models capable of predicting the performance of part of them without building hardware prototypes are not freely available. The main diagrams of both the power factor correction converter's power circuit, including EMI filter, and the generic control methods are shown in Figure 1.

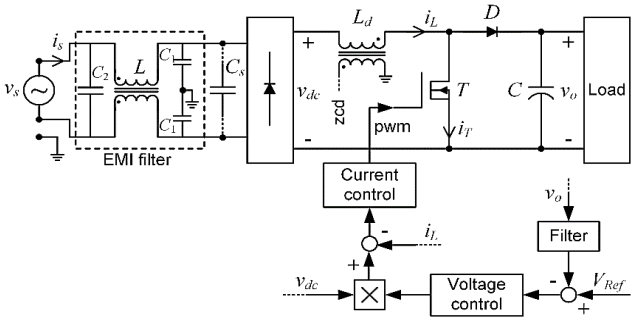


Figure 1. Global power circuit and generic/simplified control approach of the diode bridge-based PFC converter with CRM control method

2.1. Output voltage dynamics and ripple compensation

The PFC converter is a unidirectional power flow circuit; its dynamics are different under different conditions, particularly when the output power changes suddenly from full load to very low load. In this case, and from a generic point of view, the energy stored in the inductor is transferred to the capacitor, and in order not to cause too high and overvoltage, the capacitor must be correctly sized. This means that there may be a non-negligible ripple in the output voltage at steady-state and full load. This ripple must therefore be attenuated before it is used by the voltage controller that sets the reference for the current. However, low-pass filtering limits the dynamic range of the voltage controller. To overcome this restriction, two approaches are common: introducing a notch filter tuned to twice the frequency of the mains voltage; estimating the voltage ripple and subtracting it from the measured DC voltage [18]. The notch filter transfer function, $G_{NF}(s)$, being w_o the frequency to be eliminated and Q the quality factor, is given by (1).

$$G_{NF}(s) = \frac{s^2+\omega_o^2}{s^2+2s\omega_o/Q+\omega_o^2} \quad (1)$$

To take advantage of this filter, it is needed a high Q and a precisely adjusted filter. If these conditions are not met, the filter's performance degrades rapidly. As the output voltage ripple is only approximated by the second harmonic component, other harmonic components are processed by the voltage controller, and when multiplied by the sinusoidal AC voltage, are transmitted to the current reference, increasing its distortion. Moreover, in the event of rapid dynamic changes, the filter's temporal response is poor in relation to the application.

Considering that the converter is operating at a frequency much higher than the grid frequency and has no losses, it can be assumed that the instantaneous powers at the input and output of the converter are almost equal, i.e. $p_i(t) = p_o(t)$. This approximation makes it possible to identify the low-frequency (LF) component of the ripple in the output voltage, which occurs at twice the grid frequency. In steady-state the instantaneous power at the input stage is given by (2).

$$p_i(t) = \sqrt{2}V_s\, sin(\omega t)\sqrt{2}I_s\, sin(\omega t) = V_s I_s(1 - cos(2\omega t)) \quad (2)$$

Where V_s and I_s are the root-mean-square values of the input voltage and the input current, respectively, and w is the grid angular frequency. The pulsating instantaneous power propagates to the output, and after some simple manipulations, the low-frequency output voltage ripple is given by (3). Where I_o is the actual DC load current, C is the total output capacitance and w is the grid angular frequency.

$$\Delta v_o(t) \cong -\frac{I_o}{2\omega C} sin(2\omega t) \quad (3)$$

The estimated voltage ripple is subtracted from the measured DC voltage thus allowing a larger bandwidth in the voltage controller. However, the implementation of this compensation term requires three conditions: a sine wave at twice the AC frequency, which is commonly implemented using a phase-locked loop (PLL), the equivalent DC capacitor at the converter output and the load current. These are three important conditions which are not simple to satisfy, and therefore, the use of this method is only justified in high performance systems.

2.2. Switching frequency

As it is intended to obtain an almost sinusoidal current in the AC side, the presence of some type of current control in the converter is essential. The current controller dynamics is an important factor in order to impose a good tracking in relation to the AC voltage waveform. In fact, the current controller is the main factor that distinguishes the different control methods of the PFC converter. From the various possible solutions, the average current controller is the only that has a conventional linear current controller with constant switching frequency [19].

The CRM control method has several advantages, which should be highlighted: absence of linear current controller, possibility of current limitation in the transistor, low switching losses in the diode, and transistor, less electromagnetic noise. In this method, the switching frequency, F_s, is variable over each AC voltage half-cycle and its expression is given by (4).

$$F_s(t) = \frac{|v_s(t)|(V_o-|v_s(t)|)}{P_o}\frac{1}{L_d\Delta I_L}, \quad (4)$$

where $v_s(t)$ is the instantaneous AC voltage, V_o is the DC output voltage, L_d is the inductance, P_o is the output power and ΔI_L is the current ripple in the same inductor.

In the CRM control method, it is obvious that ΔI_L is proportional to $|v_s(t)|$ and, for an estimate of the switching frequency variation along the half-cycle, ΔI_L can be replaced by $\Delta I_L = K|v_s(t)|$. Additional manipulations relating K with the output power allows to obtain as in (5).

$$F_s(t) = \frac{V_s^2}{2L_d P_o} \frac{V_o - |v_s(t)|}{V_o} \quad (5)$$

It is observed in (5) that F_s varies also with the load power level, increasing with the reduction of the output power. For reference, Table 1. gives the parameters used in the simulation analysis of the converter; they will also be used in the experimental set-up. As an example, Figure 2(a) shows the evolution of F_s during a half-cycle for two output power values: nominal power and light load (20% of P_n). This dependency of F_s with the load level requires a strategy for maintaining this frequency within acceptable limits either for the switching devices in terms of losses and for the generated EMI noise. For the specifications given in the Table 1, Figure 2(b) shows the evolution of F_s (with nominal power) where the constant *on* time is nearly 20 µs and a large interval of switching frequencies is observed.

Table 1. Simulation and experimental parameters

Parameter	Value
Nominal input AC voltage, V_s	65 V_{RMS}, 50 Hz
Nominal output voltage, V_o	120 V
Rated output power, P_n	120 W
DC inductance, L_d	320 µH
Output capacitance, C	1 mF
Switching frequency, F_s	variable
AC capacitance, C_s	2 µF
EMI filter: C_1, C_2, L_s	2.2 nF, 100 nF, 10 mH

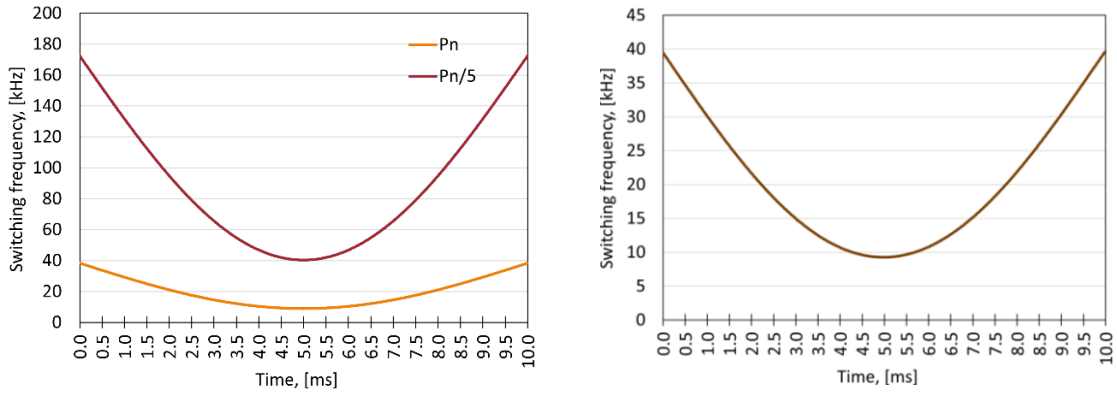


Figure 2. Switching frequency variation during a half-cycle: (a) with nominal power (Pn) and light load (Pn/5) and (b) with Pn using the MC33262 and the parameters in Table 1

2.3. Input current distortion

One of the most important parameters that qualifies each control method is the LF harmonic distortion. This low-frequency content has different roots: the current reference defined by the DC voltage controller, the current (discontinuous) in the inductor in the zero crossing zones of the AC voltage, the EMI filter needed to eliminate the high-frequency components of the current in the inductor [20], [21]. In particular, the interaction between the EMI filter and the input capacitor should be carefully analyzed when designing C_s, either in conventional topologies [22], [23], and in interleaved-based ones [24].

Current distortion at zero crossings exists in all control methods but without the same importance. It can only be partially compensated, as demonstrated in previous research [25]–[27]. In any topology, the harmonic distortion depends on the load power, degrading with smaller loads, due to larger intervals of zero current and smaller currents, even using high performance controllers [28]–[30].

3. METHOD

For controlling the PFC converter, it was selected the MC33262, available from ON Semiconductor manufacturer [31], and it has been developed a simulation model including the main control and protection features of this IC. It is given in Figure 3 the simplified block diagram of the main control functions of the IC using the blocks available in PSIM simulation software; the MOSFET current is measured by a shunt resistor and the DC-bus voltage (V_{DC}) by a resistive voltage divider.

The simulation of the PFC converter under CRM control is made for different operating conditions, focusing on aspects related to the distortion of the current in the AC source at the zero crossings, the frequency spectrum of the AC current, and the dynamic response of the output voltage. The main parameters for analysis are the waveform of the AC current and the regulation of the DC voltage. For illustration purposes it was modeled, simulated and built a PFC converter, where the passive components were sized according to the guidelines in research [31], with the parameters given in Table 1.

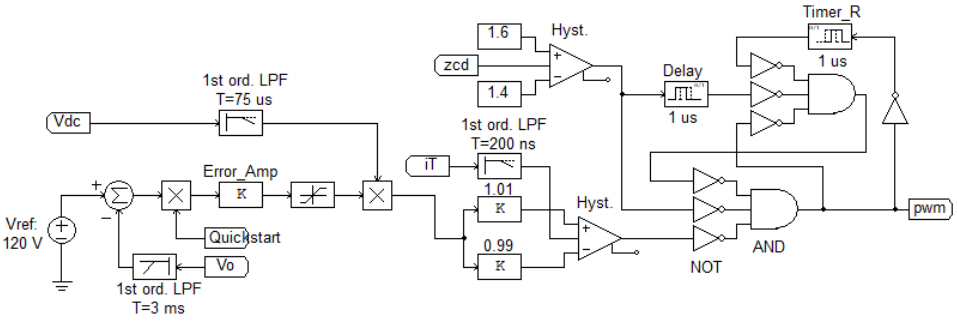


Figure 3. Simplified control block diagram, based on the MC33262, modelled with PSIM software (low-pass filter (LPF), time constant (T), zero current detector (zcd), transistor current (iT), and hysteresis comparator (Hyst))

3.1. Switching frequency design

The design guide for using the MC33262 provides expressions for sizing the boost inductor, the output capacitor and an estimation of the switching frequency. Similarly, to the ideal/theoretical CRM operation principle, the IC works on the basis of an almost fixed *on* time for the active switch, t_{on}, and a variable *off* time, t_{off}, given by (6) and (7), respectively.

$$t_{on} = \frac{2P_o L_d}{\eta V_s^2} \tag{6}$$

$$t_{off} = t_{on} \frac{|v_s(t)|}{V_o - |v_s(t)|} \tag{7}$$

The expression for the resulting switching frequency variation is similar to (5), only including the converter efficiency, η. It is given by (8).

$$F_s(t) = \frac{\eta V_s^2}{2L_d P_o} \frac{V_o - |v_s(t)|}{V_o}. \tag{8}$$

4. RESULTS AND DISCUSSION

The steady-state operation of the converter, regarding the input current, is shown in Figure 4(a) for light load (15 W) and Figure 4(b) for nominal load (120 W). In both cases it can be noticed a nearly sinusoidal waveform thus with a very low total harmonic distortion (THD) factor. In nominal load conditions there is a visible ripple in the input voltage due to the EMI filter needed in the AC side to eliminate the high frequency components of the inductor current.

4.1. Simulation results

Figure 5(a) shows a detailed view of the zero crossing of the AC current in light load condition while Figure 5(b) is in nominal load. Since the voltage (V_{ac}) is very small (near zero) in this time interval and the

current (I_{ac}) is supposed to be also very small either during the complete cycle and in the zero crossings, in light load the distortion is more visible. The effect is intensified by the EMI filter when its current is quite low compared to the nominal one. In order to further analyze the zero crossing of the AC input current, Figure 6(a) shows the relation between the zero-crossing detector signal (ZCD) of the inductor current (i_{ac}) and the generated PWM signal in light load and Figure 6(b) in nominal load condition.

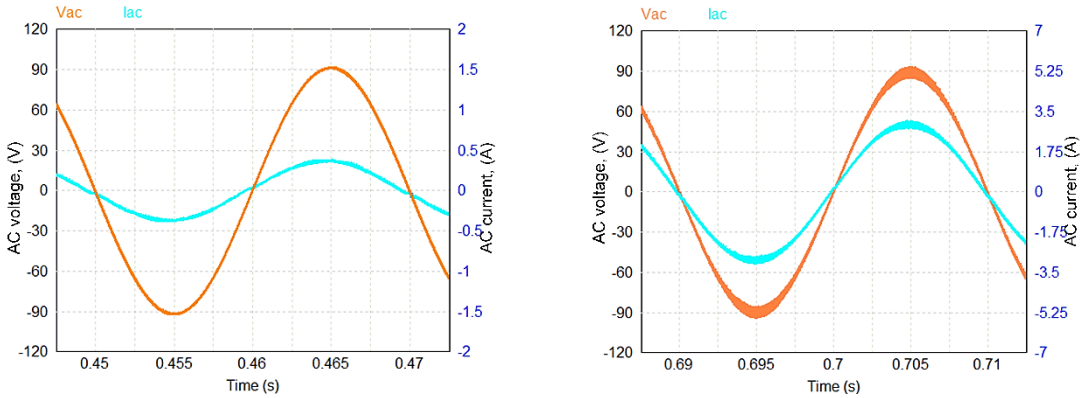


Figure 4. AC voltage (Vac) and current (Iac): (a) at light load [scales: 30 V/div, 0.5 A/div] and (b) at nominal load [scale: 1.75 A/div], [time: 2.5 ms/div]

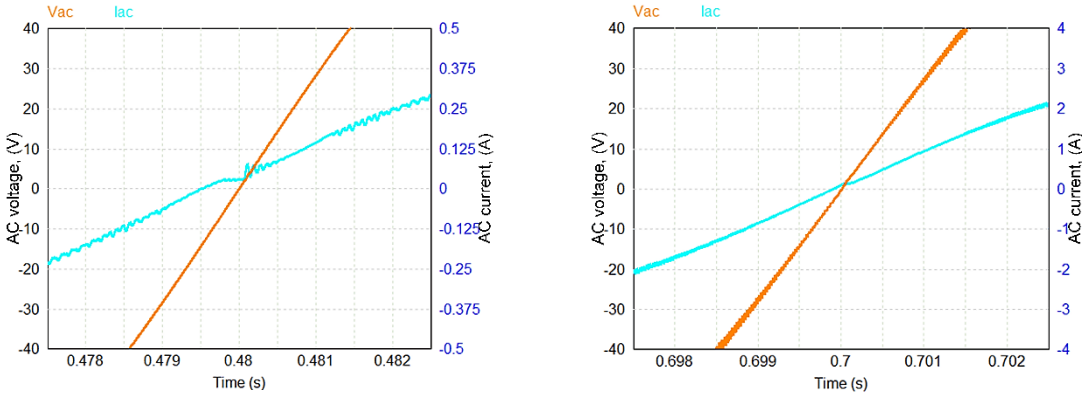


Figure 5. Zero crossing detail of the input voltage and current: (a) at light load [scales: 10 V/div, 0.125 A/div], and (b) at nominal load [scale: 1 A/div], [time: 500 µs /div]

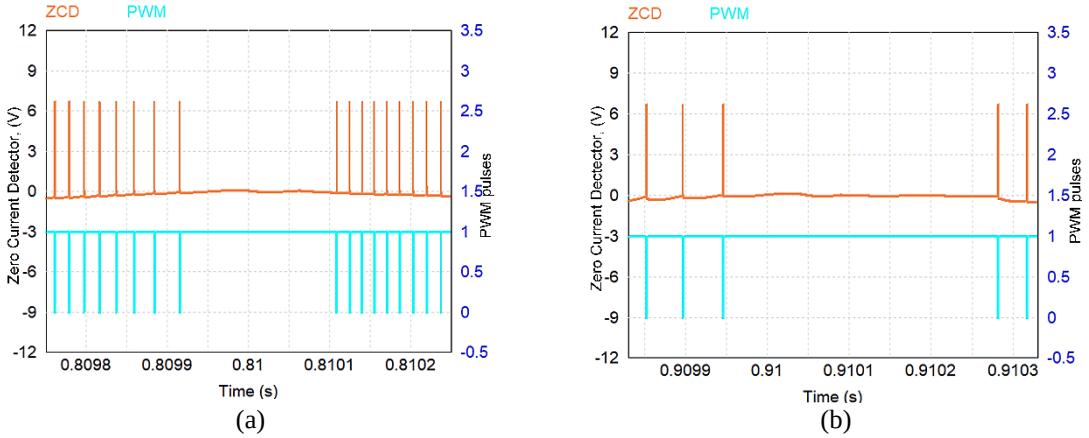


Figure 6. Zero crossing detection signal (ZCD) and PWM signal: (a) at light load and (b) at full load, [time: 50 µs /div]

It can be noticed the absence of PWM signals in the vicinity of the zero crossing of the AC voltage, either at t=0.81 s and at t=0.91 s. As shown in Figure 6(a), it can also be verified the increased switching frequency in the light load condition. The main consequence of the small distortion in the zero crossings is the appearance of some LF spectrum components, shown in Figure 7(a) for the operation in light load; they don't appear in Figure 7(b) for nominal load. The resulting THD is 3.1% for light load and 2.2% for nominal load.

Other important feature of the PFC converter is the output voltage dynamics. Under steep load changes it is expected some transient variation in the output voltage. The selected IC is designed for a relatively small bandwidth without feedforward of the load current, but including an overvoltage protection comparator.

In Figure 8(a) is shown the converter behavior (output DC voltage (V_o) and AC input current (I_{ac})) when the load changes from light load (nearly 15 W) to nominal load (120 W) and in Figure 8(b) in the opposite direction, where it can be seen the nonlinear behavior of the IC regarding the output overvoltage protection. The implemented experimental prototype used the same parameters as those in the simulation model, given in Table 1. The converter is controlled by the IC MC33262 from ON Semiconductor and, for better comparison and discussion, the experimental results shown follow the same order as in the simulation section.

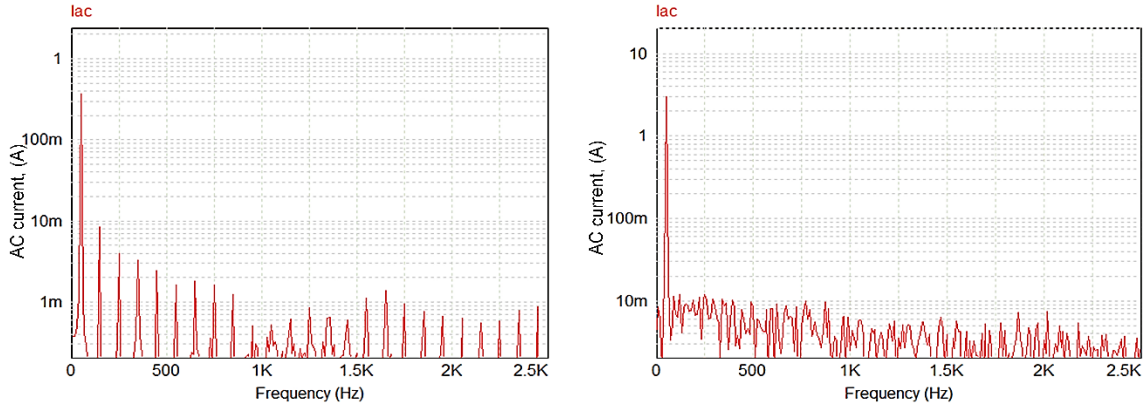


Figure 7. Frequency spectrum of the AC input current: (a) at light load, and (b) at nominal load

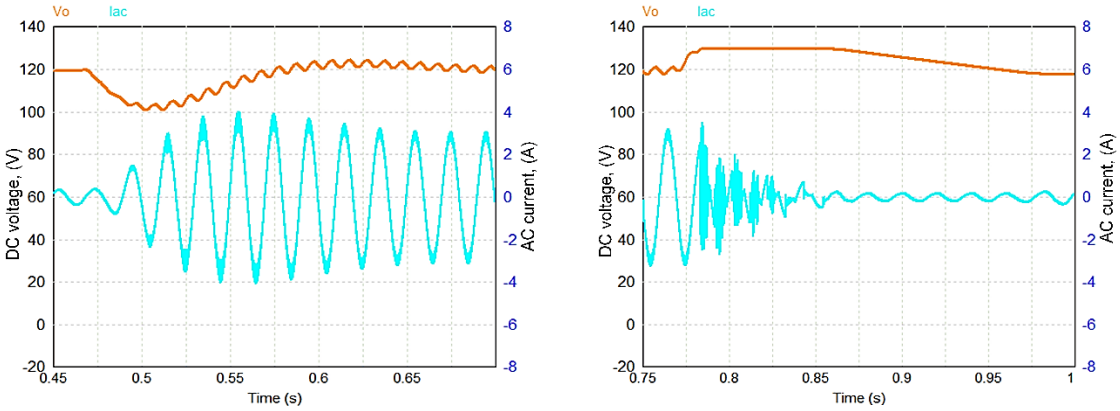


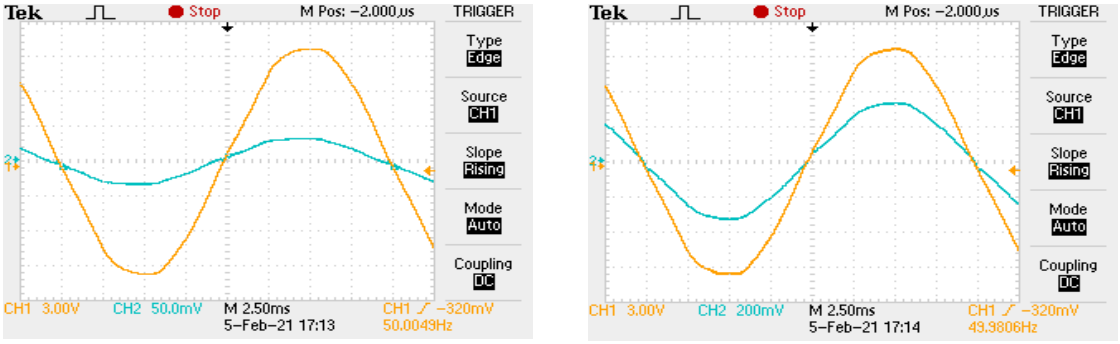
Figure 8. Output voltage dynamics: (a) load step change from 10% to 100% of the nominal power and (b) from 100% to 10% of the nominal power [scales: 20 V/div, 2 A/div, time: 25 ms/div]

4.2. Experimental results

In Figure 9(a) are shown the steady-state waveforms for the AC voltage and AC input current in light load condition and, in Figure 9(b), for nominal load power. The experimental results compare quite well with the ones in Figures 4(a) and 4(b), respectively. However, it should be mentioned that the experimental AC voltage has a THD of 2.2% thus imposing an additional distortion in the AC current.

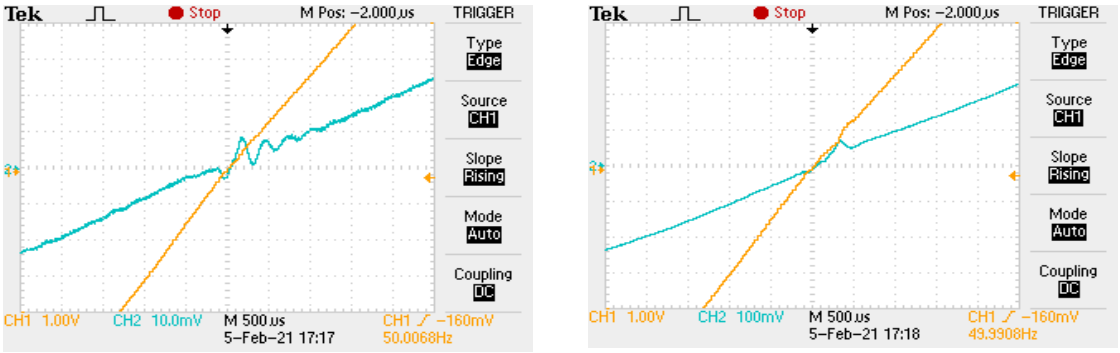
The experimental results regarding the zero crossing of the AC input current are shown in Figure 10(a) for light load and Figure 10(b) for nominal load. They can be compared with the ones presented in Figures 5(a)

and 5(b), respectively, obtained in simulation conditions. The oscillations visible in the light load operation have higher magnitude that their simulated equivalents. The main reason for the small distortion in the zero crossing is the absence of PWM pulses in this zone. Regarding this cause, a similar behavior is obtained either in simulation environment and in the experimental prototype; Figures 11(a) and 11(b) (experimental) and Figures 6(a) and 6(b) (simulation) show very close results.



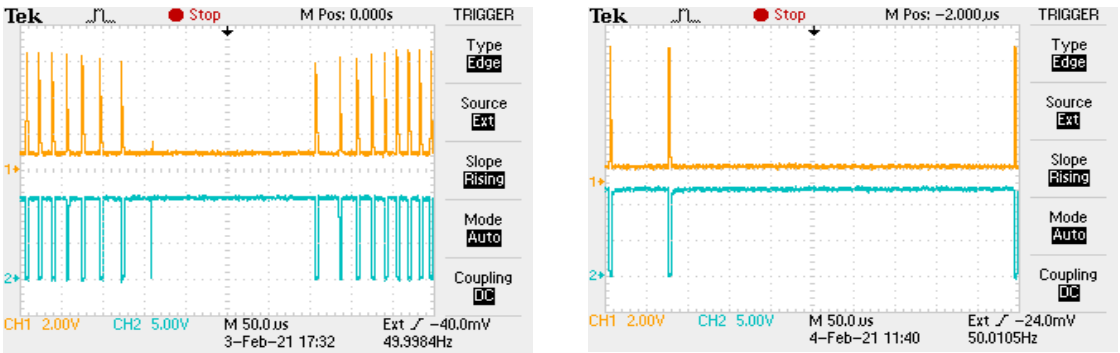
(a) (b)

Figure 9. Steady-state AC voltage (V_{ac}-brown) and current (I_{ac}-blue): (a) at light load [scales: 30 V/div, 0.5 A/div] and (b) nominal load [scales: 2 A/div]



(a) (b)

Figure 10. Zero crossing of the input current: (a) at light load [voltage signal V_{ac} - brown, scale: 10 V/div, current signal I_{ac}: blue, scale: 0.1 A/div] and (b) at nominal load [scale: 1 A/div]



(a) (b)

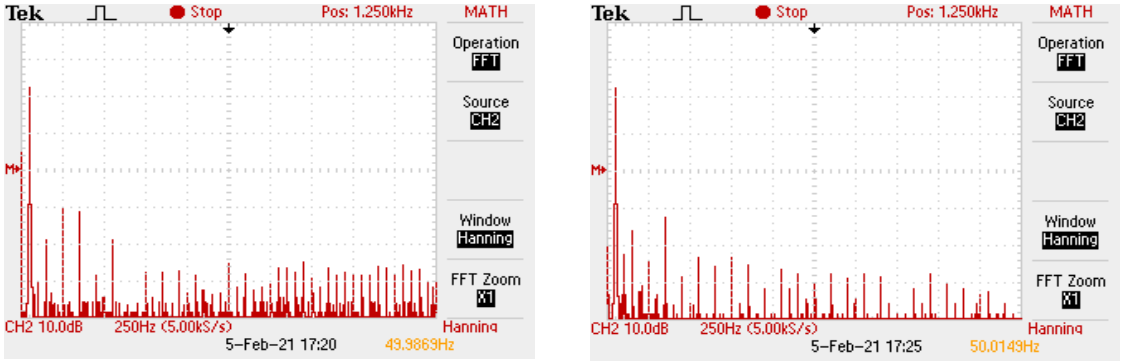
Figure 11. Zero crossing detection signal (ZCD-brown) and switching signal (PWM-blue): (a) at light load and (b) nominal load, [voltage signal scale: 2 V/div, PWM signal scale: 5 V/div]

As referred in the simulation section, the main consequence of the zero-crossing distortion is a slightly increase of the THD of the AC current compared to ideal conditions; Figures 12(a) and 12(b) show experimental results for the frequency spectrum of the AC current under light load and nominal load conditions,

respectively. Their comparison with the simulation ones, as seen in Figures 7(a) and 7(b), is difficult to perform due to the presence of a small distortion in the grid voltage, as referred above. However, the low-frequency components are present in all results being more evident in the light load operation.

A broader perspective of the low-frequency distortion is given by the THD of the AC current in the complete load range. This parameter, obtained from the experimental prototype is given in Table 2. In the full output power range, the THD is maintained at very low levels, highlighting the fact that part of this distortion is created by the AC input voltage, as referred before.

As above for the steady-state operation, this section presents results in the same sequence as those discussed in the simulation section. For load changes from 15 W to 120 W and from 120 W to 15 W, Figures 13(a) and 13(b) show the waveforms of the DC output voltage (V_o) and the AC input current (I_{ac}). These results can be compared with the ones in Figures 8(a) and 8(b), respectively, for the same conditions.

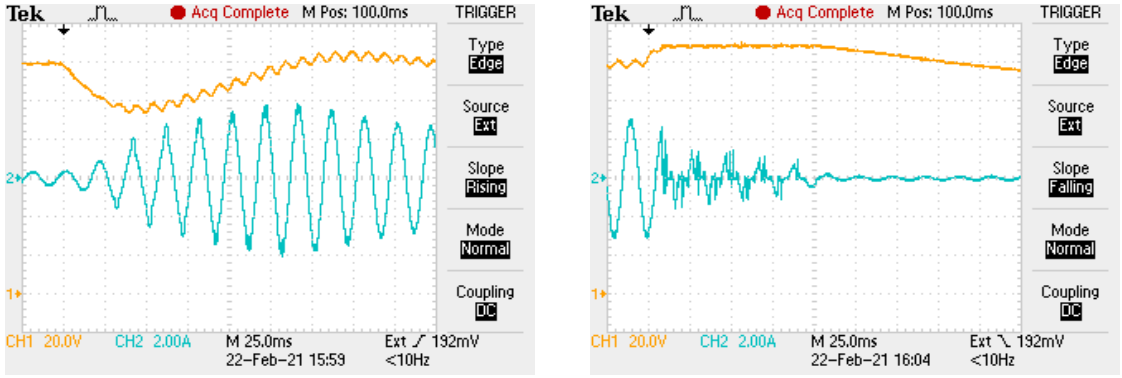


(a) (b)

Figure 12. Frequency spectrum of the AC input current: (a) at light load, P_o=25 W and (b) nominal load, P_o=120 W

Table 2. AC current THD according to the load power level

Parameter	Value						
Load power (W)	15	20	40	60	80	100	120
THD (%)	3.0	2.1	1.8	2.0	2.0	1.9	2.3



(a) (b)

Figure 13. Output voltage dynamics in load changing conditions: (a) step from 10% to 100% of the nominal power and (b) step from 100% to 10%

A very similar behavior is noticed thus validating the developed simulation model operating in quite different conditions. Another very important parameter of any converter is its energy efficiency. For the studied converter, the data gathered, giving the evolution of the efficiency for the whole power range, is summarized in Table 3. The efficiency is quite high in the complete range although it can be increased if the semiconductors would be based on SiC technology as referred in the section 1.

Table 3. Converter efficiency according to the load power level

Parameter	Value						
Load power (W)	15	20	40	60	80	100	120
Efficiency (%)	91.3	92.0	93.5	93.2	94.5	92.0	90.0

4.3. Discussion

The schematic diagram of the real IC is a complex one but it was possible to identify and model its most important control and protection blocks and related features. When comparing the simulation and experimental results it can be stated that the developed model performs very well in all conditions. Details that occur in the simulation stage also appear in the prototype, i.e., the model correctly predicts the real performance. A relevant one is the output voltage dynamics during load power steps, the other being the PWM generation at the AC voltage zero crossings with frequency variation and pulse dropping.

The AC current distortion (measured by the THD) created by the zero crossing is maintained within very low values in the whole load power range. However, it also depends on the AC voltage distortion in the point of coupling, that is, the specific application environment. The output voltage dynamics could be better but it should be noted that the converter is usually part of a larger system and the DC-bus voltage is further conditioned by additional power electronics stages either low power DC/AC inverters or DC/DC converters.

5. CONCLUSION

This paper proposed and validated a simulation model for predicting the performance of a PFC converter controlled in the critical conduction mode and using a commercial IC, representative of the large offer in the market. The most relevant aspects, related to the zero-crossing distortion of the AC input current and the output voltage dynamics were analyzed either with the developed simulation model and using an experimental set-up. An almost perfect match between simulation and experimental results demonstrated the model accuracy and its performance in predicting the converter behavior.

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