International Journal of Power Electronics and Drive Systems (IJPEDS)
Vol. 15, No. 2, June 2024, pp. 1308~1318
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v15.i2.pp1308-1318

Primary side control technique for capacitive power transfer system without any wireless feedback

Supapong Nutwong, Nattapong Hatchavanich, Anawach Sangswang, Ekkachai Mujjalinvimut, Mongkol Konghirun
Department of Electrical Engineering, King Mongkut's University of Technology Thonburi, Bangkok, Thailand

Article Info

Article history:

Received Jul 14, 2023
Revised Nov 23, 2023
Accepted Dec 7, 2023

Keywords:

Capacitive power transfer
Load variation
Output voltage regulation
Primary side control
Wireless feedback

ABSTRACT

The output voltage of capacitive power transfer (CPT) system will change if the load resistance is varied. This paper presents a method to regulate the output voltage using a controller that is located on the primary side, known as the primary side control technique. It does not require any additional components and wireless feedback, which lowers the cost and complexity of CPT system compared to the conventional control technique. Instead of directly measuring the output voltage on secondary side, it is estimated through the measured capacitor voltage on primary side. Modified sine wave control of the full-bridge inverter is adopted to regulate the output voltage. The proposed control technique is validated by the simulation via PSIM software using the practical parameters of capacitive coupler presented in the literature. Simulation results of the output voltage control against the step change in desired output voltage and load resistance indicate the performance of proposed control technique.

Corresponding Author:

Nattapong Hatchavanich
Department of Electrical Engineering, King Mongkut's University of Technology Thonburi
126 Pracha Uthit Rd., Bang Mod, Thung Khru, Bangkok, 10140, Thailand
Email: nattapong.hat@kmutt.ac.th

1. INTRODUCTION

Capacitive power transfer (CPT) is a novel technique for wirelessly transmitting electrical energy across an air gap through electric field between conductive plates. Safety, convenience, and automated operation can be obtained from this technique. It has lower cost, weight, and loss compared to the inductive power transfer (IPT) technique [1]–[3]. Nowadays, it has been adopted in various applications, such as biomedical implants [4]–[6], portable devices [7]–[9], electric vehicles [10]–[13], unmanned aerial vehicles (UAVs) [14]–[16], autonomous underwater vehicles (AUVs) [17]–[19], and rotary applications [20]–[25].

In practical CPT system, variation of the load is inevitable, e.g., the change in state of charge (SOC) of battery while it is charging. This causes the equivalent load resistance to vary which resulted in fluctuations of output voltage and output power. Therefore, the close loop control is indispensable to this system. The close loop control technique presented in previous research can be categorized by the location of controller as primary side control, secondary side control, and dual side control. The dual side control technique is introduced in [23] where the full-bridge inverter in primary circuit is used to perform frequency tracking. The compensation circuits on both primary and secondary side are controlled to perform the impedance matching, which is done by using the additional controllable inductors. The combined frequency tracking and matching network can regulate a target current to the secondary side at best power transfer conditions. However, this technique needs controllable inductors which are costly and difficult to control. The secondary side control technique is presented in previous research [24] which uses the half-bridge inverter in primary side. The extra

DC-DC buck-boost converter is added in the secondary side to control the equivalent output resistance. Although the optimal equivalent resistance against the load variations can be achieved via tracking the maximum power point, it requires an additional circuit which increases the component counts, cost, and loss to the system. The primary side control technique is presented in [25]–[29]. The class E inverter is adopted in [25] and [26]. The transferred power is controlled by switching extra capacitors parallel to the inverter switch [25]. This also increases the component counts and complexity to the system. Lu and Nguang [26] proposed any extra component is added to the circuit, but it needs wireless feedback to enable the control. Similarly, wireless communication between primary and secondary side is required in [27] and [28] to control the active-clamped half-bridge (ACHB) inverter and full-bridge inverter, respectively. A three-phase bridge inverter is used in the primary circuit [29]. The burst-mode current control is adopted to regulate the dc output current. Although wireless feedback is not required, three current sensors are needed in this technique.

As discussed earlier, the control technique introduced in previous research requires additional components on primary and/or secondary circuit and wireless feedback, which increases the cost, complexity, and loss to the system. To overcome this issue, the primary side control technique for CPT system without need of additional components and wireless feedback is presented in this paper. It requires only one voltage sensor in the proposed control technique. Instead of directly measuring the output voltage on the secondary side and wirelessly feeding it back to primary side, the output voltage is estimated through the measured voltage across a capacitor on the primary side. The output voltage is regulated via the full-bridge inverter with modified sine wave control. The proposed control technique is verified by the simulation results using the practical parameter of capacitive coupler [30]. For comparison purposes, the proposed control technique is compared with the previous control techniques as listed in Table 1.

Table 1. Comparison between proposed control technique and previous control techniques

Sources	Inverter topology	Control technique	Additional components on primary side	Additional components on secondary side	Wireless feedback	Number of sensors
[23]	Full-bridge	Dual side	Controlled inductor	Controlled inductor	No	5
[24]	Half-bridge	Secondary side	None	Buck-boost	No	2
[25]	Class E	Primary side	Switching capacitor	None	Yes	1
[26]	Class E	Primary side	None	None	Yes	1
[27]	ACHB	Primary side	None	None	Yes	1
[28]	Full-bridge	Primary side	None	None	Yes	2
[29]	Three-phase bridge	Primary side	None	None	No	3
This work	Full-bridge	Primary side	None	None	No	1

2. SYSTEM ANALYSIS

2.1. System description

The proposed capacitive power transfer system is shown in Figure 1. A full-bridge inverter circuit is used to convert a smooth DC voltage (V_{dc}) into a high-frequency AC voltage (V_{in}). The capacitive coupler consists of four conductive plates which are P_1, P_2, P_3, and P_4. The plate P_1 and P_2 are located on the primary side whereas P_3 and P_4 are located on secondary side. Using the practical capacitive coupler as presented in [30], the plate length (l) and the air gap between plates (d) can be defined as 300 mm and 180 mm, respectively. Since the capacitive coupler requires a reactive power to wirelessly transfer the electrical energy across an air gap between plates via electric field, the double-sided LC compensation circuit (created by L_1, C_1, L_2, and C_2) is adopted to compensate for the required reactive power. If this compensation circuit is properly tuned, the system will operate at resonance state. Equivalent series resistance (ESR) of resonant inductor L_1 and L_2 are defined by R_1 and R_2, respectively. A resistor (R_L) on secondary-side is a load of the system. In this proposed system, the output voltage (V_{out}) can be regulated by the controller on primary side, known as primary side controller, without need of any measurement on secondary side and wireless communication between both sides. Only the voltage across capacitor C_1 on primary side (V_1) is measured and sent to the controller. After the output voltage is estimated and compared with the desired (reference) value, the controller will send gate signals to the full-bridge inverter circuit to adjust the effective magnitude of inverter voltage (V_{in}). This will regulate the output voltage.

2.2. Circuit analysis

To simplify the analysis, it is based on some assumptions: The circuit is considered as high-quality factor (high Q) circuit where the inverter current (I_{in}) is sinusoid. Therefore, the first harmonic approximation (FHA) can be applied. Since equivalent series resistance (ESR) of resonant inductors are increasing with frequency due to the skin effect, they are included in the analysis. The ESR of resonant capacitors are neglected

due to the multilayer ceramic chip capacitors (MLCCs) which have very low dissipation factor and very low ESR at high frequency are adopted and All switches are ideal.

The simplified equivalent circuit of proposed capacitive power transfer system is shown in Figure 2, based on the two-port model of capacitive coupler. The inverter voltage is replaced by its fundamental component, which is denoted by $V_{in,1}$. The capacitors C_p and C_s are defined as primary capacitor and secondary capacitor, respectively. The voltage-controlled current sources I_p and I_s can be expressed as (1) and (2).

$$\vec{I}_p = j\omega C_m \vec{V}_2 \tag{1}$$

$$\vec{I}_s = j\omega C_m \vec{V}_1 \tag{2}$$

Where C_m is the mutual capacitance. As referred to the practical capacitive coupler presented in [30], the value of C_p, C_s, and C_m can be specified as 9.8 pF, 9.8 pF, and 2.8 pF, respectively. Each element in secondary circuit can be represented in terms of its admittance. Their parallel connection can be shown in Figure 3.

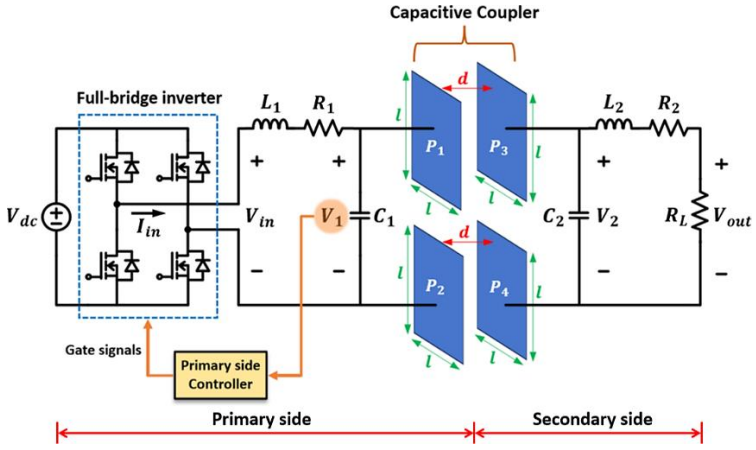

Figure 1. Proposed capacitive power transfer system

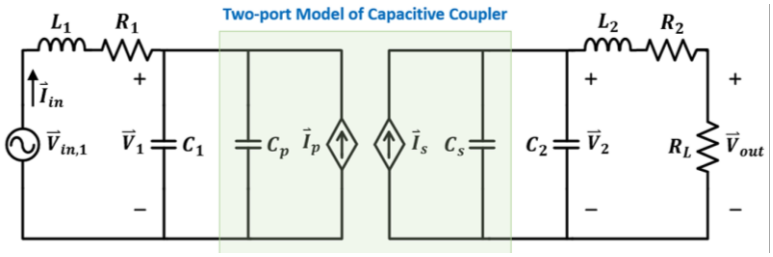

Figure 2. Simplified equivalent circuit of proposed CPT system

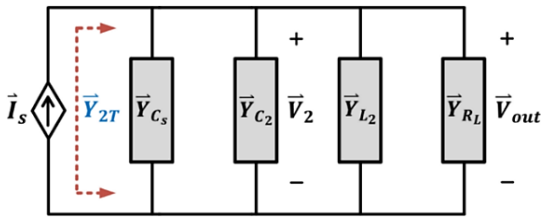

Figure 3. Parallel connection of the admittance in secondary circuit

Each admittance in Figure 3 is defined by (3)-(6).

$$\vec{Y}_{C_s} = j\omega C_s \tag{3}$$

$$\vec{Y}_{C_2} = j\omega C_2 \quad (4)$$

$$\vec{Y}_{L_2} = \frac{-j\omega L_2}{R_{Leq}^2+\omega^2 L_2^2} \quad (5)$$

$$\vec{Y}_{R_L} = \frac{R_{Leq}}{R_{Leq}^2+\omega^2 L_2^2} \quad (6)$$

Where $R_{Leq} = R_2 + R_L$ is the equivalent load resistance. The equivalent secondary admittance (Y_{2T}) which is the parallel combination of each admittance in the secondary circuit can be obtained by (7).

$$\vec{Y}_{2T} = \frac{R_{Leq}+j\left(\omega^3 C_s L_2^2+\omega^3 C_2 L_2^2+\omega C_s R_{Leq}^2+\omega C_2 R_{Leq}^2-\omega L_2\right)}{R_{Leq}^2+\omega^2 L_2^2} \quad (7)$$

The imaginary part of Y_{2T} will be equal to zero if the system operates at resonant frequency (ω_0). This can be achieved by tuning the value of C_2 by (8).

$$C_2 = \frac{L_2-C_s\omega_0^2 L_2^2-C_s R_{Leq}^2}{R_{Leq}^2+\omega_0^2 L_2^2} \quad (8)$$

Parallel connection of the admittance in primary circuit is shown in Figure 4 where the current source I_{in} is derived from the source transformation technique.

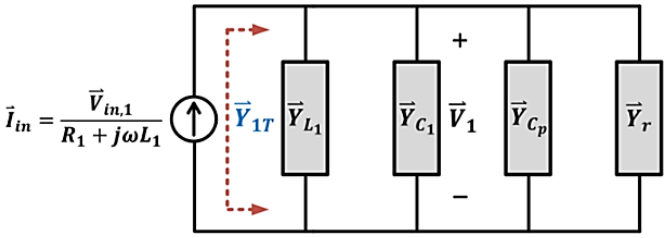

Figure 4. Parallel connection of the admittance in primary circuit

Since $\vec{Y}_{2T}$ is identical to $\vec{Y}_{R_L}$ at the resonant frequency (ω_0), the admittance that reflects from secondary to primary circuit, which is denoted by Y_r, can be as (9):

$$\vec{Y}_r = \frac{\omega_0^2 C_m^2\left(R_{Leq}^2+\omega_0^2 L_2^2\right)}{R_{Leq}} \quad (9)$$

The equivalent primary admittance (Y_{1T}) which is the parallel combination of each admittance in the primary circuit can be obtained by (10).

$$\vec{Y}_{1T} = \frac{R_{Leq}R_1+C_m^2\omega_0^2\left(R_{Leq}^2+\omega_0^2 L_2^2\right)\left(R_1^2+\omega_0^2 L_1^2\right)-j\left[\omega_0 L_1 R_{Leq}-\omega_0 C_1 R_{Leq}\left(R_1^2+\omega_0^2 L_1^2\right)-\omega_0 C_p R_{Leq}\left(R_1^2+\omega_0^2 L_1^2\right)\right]}{R_{Leq}\left(R_1^2+\omega_0^2 L_1^2\right)} \quad (10)$$

The imaginary part of Y_{1T} will be equal to zero if the capacitor C_1 is tuned to (11).

$$C_1 = \frac{L_1-C_p R_1^2-C_p L_1^2\omega_0^2}{R_1^2+\omega_0^2 L_1^2} \quad (11)$$

The at resonant state, the voltage across capacitor C_1 (V_1) is given as (12).

$$\vec{V}_1 = \frac{\vec{I}_{in}}{\vec{Y}_{1T}} = \frac{\vec{V}_{in,1}R_{Leq}\left(R_1^2+\omega_0^2 L_1^2\right)}{(R_1+j\omega_0 L_1)\left[R_{Leq}R_1+C_m^2\omega_0^2\left(R_{Leq}^2+\omega_0^2 L_2^2\right)\left(R_1^2+\omega_0^2 L_1^2\right)\right]} \quad (12)$$

From (12), the magnitude of voltage V_1 can be obtained by the (13).

$$\left|\vec{V}_1\right| = \frac{R_{Leq}\left|\vec{V}_{in,1}\right|\sqrt{R_1^2+\omega_0^2L_1^2}}{R_{Leq}R_1+C_m^2\omega_0^2\left(R_{Leq}^2+\omega_0^2L_2^2\right)\left(R_1^2+\omega_0^2L_1^2\right)} \quad (13)$$

Where $\left|\vec{V}_{in,1}\right|$ is the magnitude of fundamental component of inverter voltage. The voltage across capacitor C_2 (V_2) can be expressed as (14).

$$\vec{V}_2 = \frac{\vec{I}_s}{\vec{Y}_{R_L}} = \frac{j\omega_0C_m\vec{V}_1\left(R_{Leq}^2+\omega_0^2L_2^2\right)}{R_{Leq}} \quad (14)$$

Substitute (12) into (14), the magnitude of voltage V_2 is obtained as (15).

$$\left|\vec{V}_2\right| = \frac{\omega_0C_m\left|\vec{V}_{in,1}\right|\left(R_{Leq}^2+\omega_0^2L_2^2\right)\sqrt{R_1^2+\omega_0^2L_1^2}}{R_{Leq}R_1+C_m^2\omega_0^2\left(R_{Leq}^2+\omega_0^2L_2^2\right)\left(R_1^2+\omega_0^2L_1^2\right)} \quad (15)$$

By applying voltage division technique to the far-right loop of a circuit shown in Figure 2, voltage across the equivalent load resistance is given as (16).

$$\vec{V}_{RL_{eq}} = \frac{R_{Leq}\vec{V}_2}{R_{Leq}+j\omega_0L_2} = \frac{R_{Leq}\left(R_{Leq}-j\omega_0L_2\right)\vec{V}_2}{R_{Leq}^2+\omega_0^2L_2^2} \quad (16)$$

Substitute (14) into (16), the magnitude of voltage $\vec{V}_{RL_{eq}}$ is obtained as (17).

$$\left|\vec{V}_{RL_{eq}}\right| = \frac{\omega_0C_mR_{Leq}\left|\vec{V}_{in,1}\right|\sqrt{R_1^2+\omega_0^2L_1^2}\sqrt{R_{Leq}^2+\omega_0^2L_2^2}}{R_{Leq}R_1+C_m^2\omega_0^2\left(R_{Leq}^2+\omega_0^2L_2^2\right)\left(R_1^2+\omega_0^2L_1^2\right)} \quad (17)$$

From (17), the magnitude of output voltage can be calculated as (18).

$$\left|\vec{V}_{out}\right| = \frac{R_L\left|\vec{V}_{RL_{eq}}\right|}{R_2+R_L} = \frac{\omega_0C_mR_L\left|\vec{V}_{in,1}\right|\sqrt{R_1^2+\omega_0^2L_1^2}\sqrt{R_{Leq}^2+\omega_0^2L_2^2}}{R_{Leq}R_1+C_m^2\omega_0^2\left(R_{Leq}^2+\omega_0^2L_2^2\right)\left(R_1^2+\omega_0^2L_1^2\right)} \quad (18)$$

It is obviously seen from (18) that the magnitude of output voltage ($\left|\vec{V}_{out}\right|$) varies with the change in load resistance (R_L). However, it can be regulated by adjusting the magnitude of an input voltage $\left|\vec{V}_{in,1}\right|$.

3. PRIMARY SIDE CONTROL TECHNIQUE

The method to regulate the magnitude of output voltage based on the primary side controller is presented in this paper. The measurements on the secondary side and wireless communication between primary and secondary side are not required in the proposed technique. Only the voltage across a resonant capacitor on the primary side is measured and taken as the feedback signal for controller. This reduces the component counts and complexity of CPT system.

As discussed in section 2, the magnitude of output voltage can be regulated by controlling the magnitude of fundamental component of inverter voltage ($\left|\vec{V}_{in,1}\right|$). This can be done by adjusting the waveform of inverter voltage (V_{in}). To achieve this waveform shaping, the modified sine wave control technique for full-bridge inverter is adopted in this work which can be shown in Figure 5. The waveform of inverter voltage obtained in this technique is identical to the phase-shift (PS) control strategy [31]–[33], which is a modified sine wave. In PS control, the duty cycle of each gate signal is fixed at 50 percent and the shape of inverter output voltage is adjusted by shifting the phase between the gate signals. On the other hand, in modified sine wave technique presented in this paper, duty cycle of each gate signal is varied. Gate signals of switch S_1 (V_{G1}) and switch S_2 (V_{G2}) are active for DT seconds where D is a duty cycle and T is a switching period. The phase difference between V_{G1} and V_{G2} is fixed at 180 degrees. Gate signals of switch S_3 (V_{G3}) and switch S_4 (V_{G4}) operate in the complementary manner to V_{G1} and V_{G2}, respectively. If V_{G3} and V_{G4} are active at the same time, the inverter voltage (V_{in}) will be equal to zero. The duty cycle of V_{G1} and V_{G2} range between 0 (0%) and 0.5 (50%). When D = 0.5, the V_{in} is a square wave. If $0 < D < 0.5$, it will be a modified sinewave. It is noted that the switching frequency is constant throughout the operation.

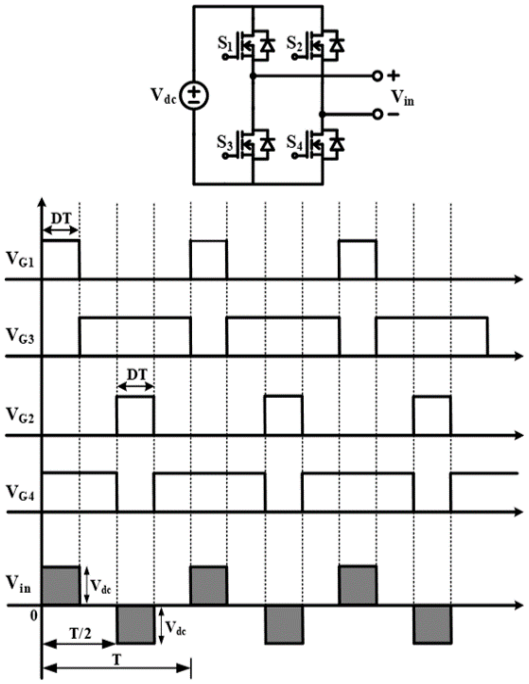

Figure 5. Timing diagram of the full-bridge inverter with modified sine wave control

As referred to Figure 5, the magnitude of fundamental component of inverter voltage can be controlled by adjusting the duty cycle (D) of gate signals V_{G1} and V_{G2}, which can be calculated by (19).

$$\left|\vec{V}_{in,1}\right| = \frac{4V_{dc}}{\pi}\cos\left(\frac{\pi}{2} - \pi D\right) \tag{19}$$

As considered in (13) and (18), load resistance and the magnitude of output voltage can be estimated through the measured value of voltage V_1. The estimated values of load resistance and the magnitude of output voltage are defined as R_L^{est} and $\left|\vec{V}_{out}^{est}\right|$, respectively. By substituting (19) into (13), load resistance can be estimated by (20).

$$R_L^{est} = \alpha\left(\beta + \sqrt{\gamma + \delta + \rho}\right) - R_2 \tag{20}$$

Where $\alpha, \beta, \gamma, \delta$, and ρ are defined as (21)-(25).

$$\alpha = \frac{-1}{2C_m^2\omega_0^2\left|\vec{V}_1\right|\left(R_1^2+\omega_0^2L_1^2\right)} \tag{21}$$

$$\beta = R_1\left|\vec{V}_1\right| - \frac{4V_{dc}}{\pi}\cos\left(\frac{\pi}{2} - \pi D\right)\sqrt{R_1^2 + \omega_0^2L_1^2} \tag{22}$$

$$\gamma = -4C_m^4L_1^4L_2^2\omega_0^{10}\left|\vec{V}_1\right|^2 - 8C_m^4L_1^2L_2^2R_1^2\omega_0^8\left|\vec{V}_1\right|^2 \tag{23}$$

$$\delta = -4C_m^4L_2^2R_1^4\omega_0^6\left|\vec{V}_1\right| + \omega_0^2L_1^2\left[\frac{4V_{dc}}{\pi}\cos\left(\frac{\pi}{2} - \pi D\right)\right]^2 + R_1^2\left|\vec{V}_1\right|^2 \tag{24}$$

$$\rho = -8R_1\left|\vec{V}_1\right|\frac{V_{dc}}{\pi}\cos\left(\frac{\pi}{2} - \pi D\right)\sqrt{R_1^2 + \omega_0^2L_1^2} + R_1^2\left[\frac{4V_{dc}}{\pi}\cos\left(\frac{\pi}{2} - \pi D\right)\right]^2 \tag{25}$$

If the estimated value of load resistance is obtained, the magnitude of output voltage can be estimated using (18) as (26).

$$\left|\vec{V}_{out}^{est}\right| = \frac{\omega_0C_mR_L^{est}\left[\frac{4V_{dc}}{\pi}\cos\left(\frac{\pi}{2}-\pi D\right)\right]\sqrt{R_1^2+\omega_0^2L_1^2}\sqrt{\left(R_2+R_L^{est}\right)^2+\omega_0^2L_2^2}}{\left(R_2+R_L^{est}\right)R_1+C_m^2\omega_0^2\left(\left(R_2+R_L^{est}\right)^2+\omega_0^2L_2^2\right)\left(R_1^2+\omega_0^2L_1^2\right)} \tag{26}$$

It is noted in (20) and (26) that load resistance and the magnitude of an output voltage can be simply estimated by measuring the magnitude of voltage across the capacitor C_1 ($|\vec{V}_1|$), which can be done on primary side.

The workflow of proposed primary side control technique for CPT system is shown in Figure 6. First, the signal of voltage across the capacitor C_1 (V_1) is sent to the peak detector circuit to obtain its magnitude. Then, resistance of the load is estimated by using (20)-(25). After the load resistance is identified, the magnitude of output voltage is then estimated by using (26). Next, the estimated value of output voltage ($|\vec{V}_{out}^{est}|$) is compared with the desired or reference value ($|\vec{V}_{out}^{*}|$). The error is then sent to PI controller to adjust the duty cycle of the gate signals V_{G1} and V_{G2}. Finally, gate signals for the full-bridge inverter circuit are obtained.

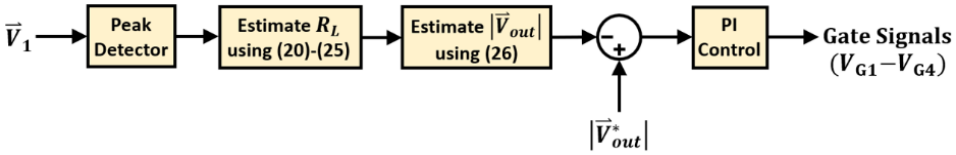

Figure 6. Block diagram of the proposed primary side control technique for CPT system

4. SIMULATION RESULTS AND DISCUSSION

To validate the proposed primary side control technique, computer simulation of the CPT system is performed as shown in Figure 7 through PSIM software. The two-port model of capacitive coupler is replaced by the equivalent π-model where $C_p' = C_p - C_m$ and $C_s' = C_s - C_m$. The voltage sensor is used to measure the voltage across the capacitor C_1 (V_1). By multiplying the rms value of V_1 with $\sqrt{2}$, the magnitude of V_1 ($|\vec{V}_1|$) is obtained. The duty cycle (D) is extracted from the gate signal of switch S_1 (V_{G1}). The estimation of load resistance and magnitude of an output voltage is implemented in the Simplified C Block. This block receives two signals which are $|\vec{V}_1|$ and D. The output signal from this block is the estimated magnitude of output voltage ($|\vec{V}_{out}^{est}|$). This signal will be compared with the desired value ($|\vec{V}_{out}^{*}|$). After sending their error to PI controller, the command signal which is the duty cycle of gate signals V_{G1} and V_{G2} of full-bridge inverter are obtained. By comparing this signal with a sawtooth signal through the comparator circuit, the square wave pulse is obtained which is taken to be the gate signal. The NOT gate is adopted to invert the gate signals (V_{G3} is opposite to V_{G1} and V_{G4} is opposite to V_{G2}). The circuit parameters used in the simulation are listed in Table 2. It is noted that the value of C_p, C_s, and C_m are from the practical capacitive coupler presented in [30]. The value of C_1 and C_2 are calculated using (11) and (8), respectively. The switching frequency of inverter circuits (f_s) is set to constant and identical to the system resonant frequency.

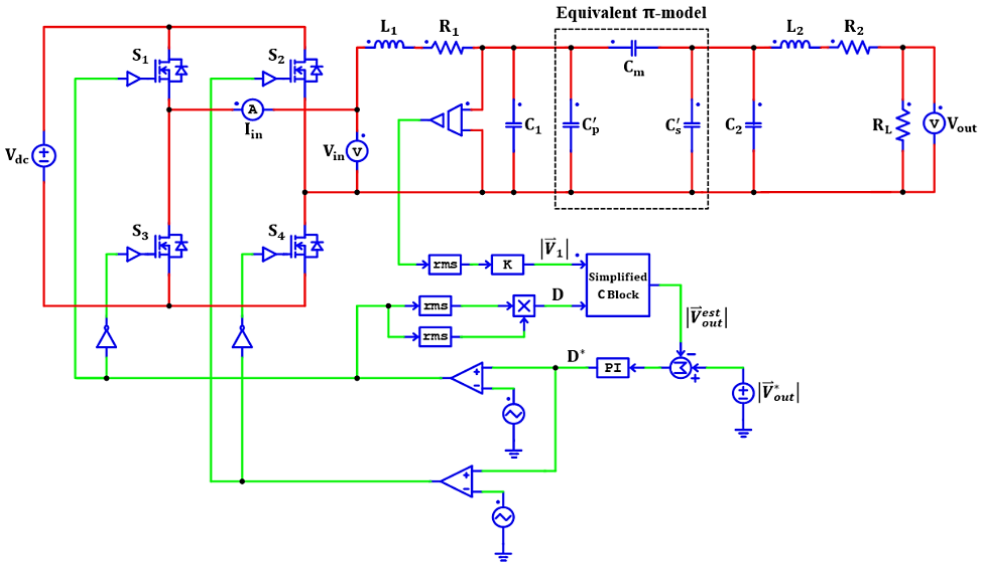

Figure 7. Simulation circuit of the proposed CPT system

Table 2. Parameters used in the simulation circuit

Parameters	Values	Parameters	Values
Capacitance of primary capacitor (C_p)	9.8 pF	Secondary compensation inductance (L_2)	86.8 µH
Capacitance of secondary capacitor (C_s)	9.8 pF	ESR of primary resonant inductor (R_1)	1 Ω
Mutual capacitance (C_m)	2.8 pF	ESR of secondary resonant inductor (R_2)	1 Ω
Primary compensation capacitance (C_1)	119.9 pF	Load resistance (R_L)	20 – 40 Ω
Secondary compensation capacitance (C_2)	119.8 pF	Input DC voltage (V_{dc})	20 V
Primary compensation inductance (L_1)	86.8 µH	Switching frequency (f_s)	1.5 MHz

Simulation result of the output voltage step response is shown in Figure 8. First, the desired magnitude of an output voltage ($|\vec{V}^*_{out}|$) is set to 20 V. Then, it is instantly changed to 40 V at 0.5 milliseconds (0.5m). As seen from the measured magnitude of an output voltage ($|\vec{V}^{mea}_{out}|$), it is controlled to follow this step change. The waveform of inverter voltage (V_{in}) and inverter current (I_{in}) are modified sinewave and sinusoid, respectively. If the pulse width of V_{in} is increased, the magnitude of output voltage will be boosted up. This can be achieved by increasing the duty cycle of V_{G1} and V_{G2}. The magnitude of I_{in} is also rising with the output voltage.

Simulation result of the output voltage regulation against load variation is shown in Figure 9. First, the load resistance is set to 40 Ω. Then, it is instantly changed to 20 Ω at 0.5 milliseconds (0.5m). The desired magnitude of an output voltage is fixed at 20 V throughout the operation. As seen from the measured magnitude of output voltage, it decreases for a moment when load resistance is reduced. However, with the proposed controller, it is regulated to increase to the desired value (20 V).

Considering conduction losses in the switches and ESR of resonant inductors, efficiency of the proposed system is analyzed from the simulation results of input power (P_{in}) and output power (P_{out}) as shown in Figure 10. On-resistance of each MOSFET is assumed to be 100 mΩ and the ESR of resonant inductor is indicated in Table 2. The measured DC input power and AC output power are 36.1 Watts and 29.6 Watts, respectively. Thus, the system efficiency is obtained as 82 percent.

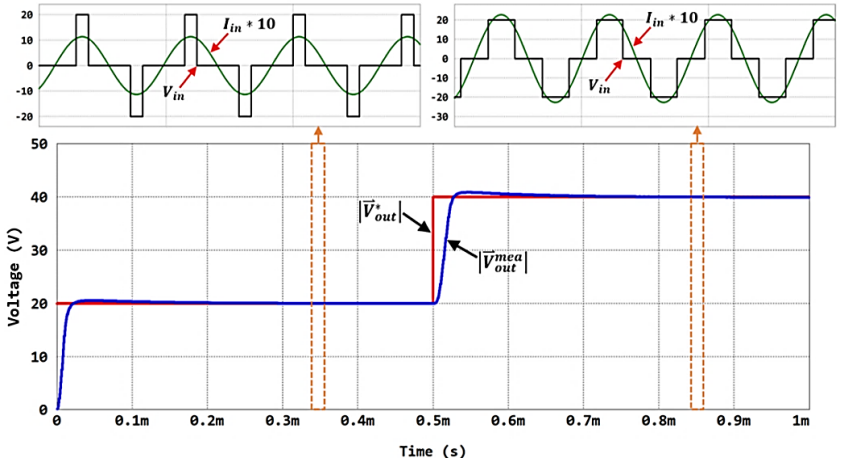

Figure 8. Simulation result of the output voltage step response

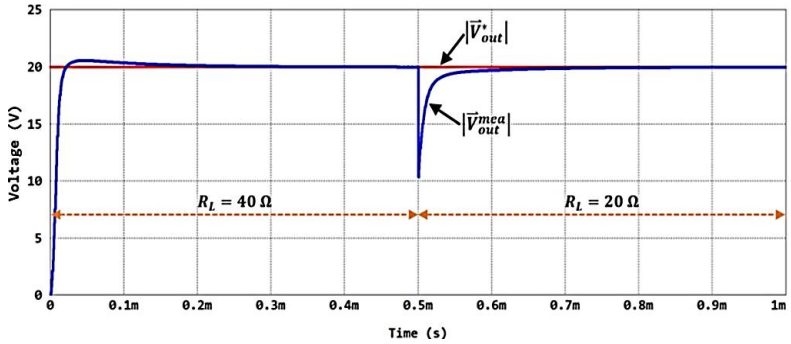

Figure 9. Simulation result of the output voltage regulation against load variation

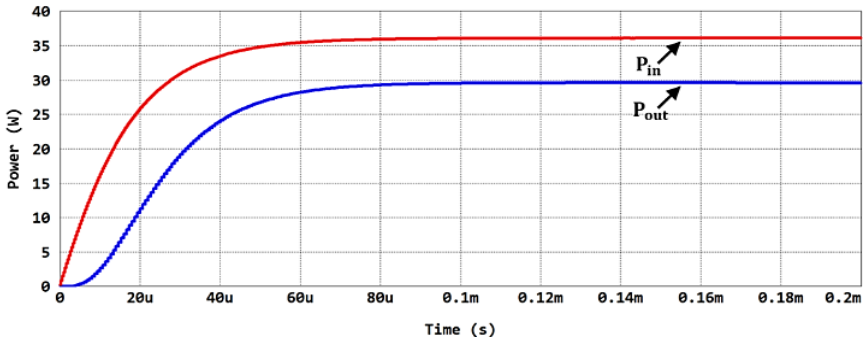

Figure 10. Simulation result of the input and output power

5. CONCLUSION

A method to regulate the output voltage of capacitive power transfer (CPT) system based on primary side control technique is presented in this paper. Additional components and wireless feedback are not required in the proposed control technique. Only a voltage sensor is required in the primary circuit. This reduces the component counts, cost, and complexity of CPT system. Instead of directly measuring the output voltage on secondary side, it is estimated through the measured capacitor voltage on primary side. This estimated value is used as the feedback signal for the controller. The output voltage is controlled to follow the desired (reference) value by adjusting duty cycle of the inverter switch. This is achieved by using the modified sine wave control of full-bridge inverter. The simulation results indicate that the output voltage can be regulated against the step change in desired value and load resistance. This validates the proposed control technique.

ACKNOWLEDGEMENTS

This research project is supported by Thailand Science Research and Innovation (TSRI). Basic Research Fund: Fiscal year 2023 under project number FRB660073/0164.

REFERENCES

[1] Z. Wang, Y. Zhang, X. He, B. Luo, and R. Mai, "Research and Application of Capacitive Power Transfer System: A Review," *Electronics (Switzerland)*, vol. 11, no. 7, 2022, doi: 10.3390/electronics11071158.

[2] H. Mahdi, R. Hattori, B. Hoff, A. Uezu, and K. Akiyoshi, "Design Considerations of Capacitive Power Transfer Systems," *IEEE Access*, vol. 11, pp. 57806–57818, 2023, doi: 10.1109/ACCESS.2023.3283908.

[3] M. Z. Erel, K. C. Bayindir, M. T. Aydemir, S. K. Chaudhary, and J. M. Guerrero, "A Comprehensive Review on Wireless Capacitive Power Transfer Technology: Fundamentals and Applications," *IEEE Access*, vol. 10, pp. 3116–3143, 2022, doi: 10.1109/ACCESS.2021.3139761.

[4] R. Sedehi *et al.*, "A Wireless Power Method for Deeply Implanted Biomedical Devices via Capacitively Coupled Conductive Power Transfer," *IEEE Transactions on Power Electronics*, vol. 36, no. 2, pp. 1870–1882, Feb. 2021, doi: 10.1109/TPEL.2020.3009048.

[5] A. N. M. S. Hossain, R. Erfani, P. Mohseni, and H. M. Lavasani, "On the Non-idealities of a Capacitive Link for Wireless Power Transfer to Biomedical Implants," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 15, no. 2, pp. 314–325, 2021, doi: 10.1109/TBCAS.2021.3069842.

[6] M. Z. Bin Mustapa, S. Saat, Y. Yusof, and M. M. Shaari, "Capacitive power transfer in biomedical implantable device: a review," *International Journal of Power Electronics and Drive Systems*, vol. 10, no. 2, pp. 935–942, 2019, doi: 10.11591/ijpeds.v10.i2.pp935-942.

[7] J. Q. Zhu *et al.*, "A Novel Capacitive Coupler Array with Free-Positioning Feature for Mobile Tablet Applications," *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 6014–6019, 2019, doi: 10.1109/TPEL.2018.2888623.

[8] K. K. Hasan, S. Saat, Y. Yusop, M. A. Majid, and M. S. Ramli, "Analysis and design of class e-lccl compensation circuit topology circuit topology for capacitive power transfer system," *International Journal of Power Electronics and Drive Systems*, vol. 12, no. 2, pp. 1265–1274, 2021, doi: 10.11591/ijpeds.v12.i2.pp1265-1274.

[9] M. B. Lillholm, Y. Dou, X. Chen, and Z. Zhang, "Analysis and Design of 10-MHz Capacitive Power Transfer With Multiple Independent Outputs for Low-Power Portable Devices," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 1, pp. 149–159, 2022, doi: 10.1109/JESTPE.2020.3035493.

[10] J. Dai and D. C. Ludois, "Capacitive Power Transfer Through a Conformal Bumper for Electric Vehicle Charging," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 1015–1025, 2016, doi: 10.1109/JESTPE.2015.2505622.

[11] S. Kodeeswaran and M. Nandhini Gayathri, "Performance investigation of capacitive wireless charging topologies for electric vehicles," *2021 International Conference on Innovative Trends in Information Technology, ICITIIT 2021*, 2021, doi: 10.1109/ICITIIT51526.2021.9399608.

[12] V. B. Vu, M. Dahidah, V. Pickert, and V. T. Phan, "An Improved LCL-L Compensation Topology for Capacitive Power Transfer in Electric Vehicle Charging," *IEEE Access*, vol. 8, pp. 27757–27768, 2020, doi: 10.1109/ACCESS.2020.2971961.

[13] C. Li, X. Zhao, C. Liao, and L. Wang, "A graphical analysis on compensation designs of large-gap CPT systems for EV charging applications," *CES Transactions on Electrical Machines and Systems*, vol. 2, no. 2, pp. 232–242, 2018, doi: 10.30941/cestems.2018.00029.

[14] A. Muharam, T. M. Mostafa, and R. Hattori, "Design of power receiving side in wireless charging system for UAV application," *Proceeding - ICSEEA 2017 International Conference on Sustainable Energy Engineering and Application: "Continuous Improvement of Sustainable Energy for Eco-Mobility"*, vol. 2018-January, pp. 133–139, 2017, doi: 10.1109/ICSEEA.2017.8267698.
[15] T. M. Mostafa, A. Muharam, and R. Hattori, "Wireless battery charging system for drones via capacitive power transfer," *2017 IEEE PELS Workshop on Emerging Technologies: Wireless Power Transfer, WoW 2017*, 2017, doi: 10.1109/WoW.2017.7959357.
[16] C. Cai, X. Liu, S. Wu, X. Chen, W. Chai, and S. Yang, "A Misalignment Tolerance and Lightweight Wireless Charging System via Reconfigurable Capacitive Coupling for Unmanned Aerial Vehicle Applications," *IEEE Transactions on Power Electronics*, vol. 38, no. 1, pp. 22–26, 2023, doi: 10.1109/TPEL.2022.3198529.
[17] E. Rong, P. Sun, X. Zhang, G. Yang, and X. Wu, "3.3kW Underwater Capacitive Power Transfer System for Electric Ship Charging Application," *2023 IEEE International Conference on Power Science and Technology, ICPST 2023*, pp. 1052–1057, 2023, doi: 10.1109/ICPST56889.2023.10164993.
[18] L. Yang *et al.*, "Comparison Survey of Effects of Hull on AUVs for Underwater Capacitive Wireless Power Transfer System and Underwater Inductive Wireless Power Transfer System," *IEEE Access*, vol. 10, pp. 125401–125410, 2022, doi: 10.1109/ACCESS.2022.3225541.
[19] L. Yang, M. Ju, and B. Zhang, "Bidirectional Undersea Capacitive Wireless Power Transfer System," *IEEE Access*, vol. 7, pp. 121046–121054, 2019, doi: 10.1109/ACCESS.2019.2937888.
[20] D. C. Ludois, K. J. Frankforter, S. E. Behringer, and F. A. Roberts, "Double Layer Capacitive Power and Heat Transfer in Rotating Machinery," *IEEE Transactions on Industry Applications*, vol. 58, no. 5, pp. 6115–6124, 2022, doi: 10.1109/TIA.2022.3184666.
[21] C. D. Rouse, S. R. Cove, Y. Salami, P. Arsenault, and A. Bartlett, "Three-Phase Resonant Capacitive Power Transfer for Rotary Applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 1, pp. 160–169, 2022, doi: 10.1109/JESTPE.2020.3009316.
[22] N. Nabila, S. Saat, Y. Yusop, M. S. M. Isa, and A. A. Basari, "The design of auto-tuning capacitive power transfer for rotary applications using phased-locked-loop," *International Journal of Power Electronics and Drive Systems*, vol. 10, no. 1, pp. 307–318, 2019, doi: 10.11591/ijpeds.v10.i1.pp307-318.
[23] E. Abramov, A. Mindel, and M. M. Peretz, "Regulated power transfer using self-tuned networks for capacitive wireless systems," *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, vol. 2019-March, pp. 3092–3099, 2019, doi: 10.1109/APEC.2019.8721887.
[24] T. M. Mostafa, D. Bui, A. Muharam, A. P. Hu, and R. Hattori, "Load Effect Analysis and Maximum Power Transfer Tracking of CPT System," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 8, pp. 2836–2848, 2020, doi: 10.1109/TCSI.2020.2981195.
[25] L. Huang and A. P. Hu, "Power Flow Control of Capacitive Power Transfer by Soft Switching of Extra Capacitors in Class e Converter," *2018 IEEE 4th Southern Power Electronics Conference, SPEC 2018*, 2018, doi: 10.1109/SPEC.2018.8635634.
[26] K. Lu and S. K. Nguang, "LQG control of capacitive power transfer system," *2017 IEEE PELS Workshop on Emerging Technologies: Wireless Power Transfer, WoW 2017*, pp. 128–132, 2017, doi: 10.1109/WoW.2017.7959379.
[27] T. C. Tin, P. H. La, and S. J. Choi, "A Novel Asymmetric Half-Bridge Inverter for Capacitive Wireless Power Transfer," *Proceedings - 2019 International Symposium on Electrical and Electronics Engineering, ISEE 2019*, pp. 194–198, 2019, doi: 10.1109/ISEE2.2019.8921000.
[28] J. Lian and X. Qu, "An LCLC-LC-Compensated Capacitive Power Transferred Battery Charger with Near-Unity Power Factor and Configurable Charging Profile," *IEEE Transactions on Industry Applications*, vol. 58, no. 1, pp. 1053–1060, 2022, doi: 10.1109/TIA.2021.3089448.
[29] J. Dai, S. S. Hagen, and D. C. Ludois, "High-Efficiency Multiphase Capacitive Power Transfer in Sliding Carriages with Closed-Loop Burst-Mode Current Control," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 1388–1398, 2019, doi: 10.1109/JESTPE.2018.2845385.
[30] F. Lu, H. Zhang, H. Hofmann, and C. C. Mi, "A Double-Sided LC-Compensation Circuit for Loosely Coupled Capacitive Power Transfer," *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 1633–1643, 2018, doi: 10.1109/TPEL.2017.2674688.
[31] J. M. Burdío, L. A. Barragán, F. Monterde, D. Navarro, and J. Acero, "Asymmetrical voltage-cancellation control for full-bridge series resonant inverters," *IEEE Transactions on Power Electronics*, vol. 19, no. 2, pp. 461–469, 2004, doi: 10.1109/TPEL.2003.823250.
[32] D. N. Sankhe, R. R. Sawant, and Y. S. Rao, "FPGA-Based Hybrid Control Strategy for Resonant Inverter in Induction Heating Applications," *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, vol. 3, no. 1, pp. 156–165, 2021, doi: 10.1109/jestie.2021.3051584.
[33] Y. S. Hwang, J. S. Lee, S. H. Kang, M. J. Kwon, E. Jang, and B. K. Lee, "Phase Shifted Power Control Strategy for Efficiency Improvement at Medium Power Region in Induction Cooktops Using Full-Bridge Series-Resonant Inverters," *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, vol. 2023-March, pp. 1123–1127, 2023, doi: 10.1109/APEC43580.2023.10131576.

BIOGRAPHIES OF AUTHORS

Supapong Nutwong is a lecturer in Electrical Engineering Department, Faculty of Engineering, King Mongkut's University of Technology Thonburi (KMUTT), Bangkok, Thailand since 2020. He received the B.Eng. degree and M.Eng. degree in electrical engineering from the King Mongkut's University of Technology Thonburi in 2007 and 2011, respectively; and the D.Eng. degree in electrical and information engineering technology from the King Mongkut's University of Technology Thonburi in 2019. From 2013 to 2014, he was a researcher at the Educational Support Unit, KMUTT. Since 2022, he has been an assistant professor with the Department of Electrical Engineering, KMUTT. His research interests include the field of power electronics, inductive power transfer (IPT) systems, capacitive power transfer (CPT) systems, wireless charging applications, and induction heating systems. He can be contacted at email: supapong.nut@kmutt.ac.th.

Nattapong Hatchavanich is a lecturer in Electrical Engineering Department, Faculty of Engineering, King Mongkut's University of Technology Thonburi (KMUTT), Bangkok, Thailand since 2021. He received the B.Eng. degree in Electrical Engineering from the King Mongkut's University of Technology North Bangkok (KMUTNB) in 2012; received the M.Eng. degree in Electrical Engineering from the King Mongkut's University of Technology Thonburi in 2016 and the D.Eng. degree in Electrical and Information Engineering Technology from the King Mongkut's University of Technology Thonburi in 2020. His current research interests include the resonant inverter and control technique for wireless power transfer system (WPT) and induction heating applications. He can be contacted at email: nattapong.hat@kmutt.ac.th.

Anawach Sangswang is a lecturer in Electrical Engineering Department, Faculty of Engineering, King Mongkut's University of Technology Thonburi (KMUTT), Bangkok, Thailand. He received the B.Eng. degree in Electrical Engineering from the King Mongkut's University of Technology Thonburi in 1995; and the M.Sc. and Ph.D. degrees in Electrical Engineering from Drexel University, Philadelphia, PA, in 1999 and 2003, respectively. Since 2020, he has been an associate professor with the Department of Electrical Engineering, KMUTT. From 1999 to 2003, he was a research assistant with the Center for Electric Power Engineering, Drexel University. His research interests include induction heating, wireless power transfer, energy management systems, and power system stability. He can be contacted at email: anawach.san@kmutt.ac.th.

Ekkachai Mujjalinvimut is a lecturer in Electrical Engineering Department, Faculty of Engineering, King Mongkut's University of Technology Thonburi (KMUTT), Bangkok, Thailand since 2016. He received the B.Eng. degree and M.Eng. degree in Electrical Engineering from the King Mongkut's University of Technology Thonburi in 2007 and 2009, respectively and the D.Eng. degree in Electrical and Information Engineering Technology from the King Mongkut's University of Technology Thonburi in 2016. Since 2019, he has been an assistant professor with the Department of Electrical Engineering, KMUTT. His current research interests include switched mode power supplies, applications of nonlinear control theory, and digital control. He can be contacted at email: ekkachai.muj@kmutt.ac.th.

Mongkol Konghirun is a lecturer in Electrical Engineering Department, Faculty of Engineering, King Mongkut's University of Technology Thonburi (KMUTT), Bangkok, Thailand. He received the B.Eng. degree (first class honors) in Electrical Engineering from the King Mongkut's University of Technology Thonburi in 1995 and the M.Sc. and Ph.D. degrees in Electrical Engineering from The Ohio State University, Columbus, OH, USA, in 1999 and 2003, respectively. Presently, he is an associate professor with the Department of Electrical Engineering, King Mongkut's University of Technology Thonburi. His research interests include electric motor drives, power electronics, railway electrification, and renewable energy. He can be contacted at email: mongkol.kon@kmutt.ac.th.