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Performance analysis for induction motor fed by reduced switch symmetrical multilevel inverter topology

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ABSTRACT

Due to its capacity to supply more voltage levels than conventional 2-level inverters, multilevel inverters have attracted a lot of attention in recent years. Multilevel inverters may produce output waveforms that nearly approximate sinusoidal waveforms because to this characteristic, which also significantly lowers harmonic distortion. In many different power conversion systems, the introduction of reduced switch symmetrical multilevel inverter topologies has drawn significant interest. Numerous benefits, such as higher output voltage quality, reduced harmonic distortions, and increased power conversion efficiency, are provided by these novel topologies. The inclusion of these inverters in the feeding of induction motors is one of their many prominent uses. In this paper, a generalized topology is presented that generates nine levels using nine switching devices. To reduce complexity, switching pulses are generated using a low frequency pulse width modulation technique. MATLAB/Simulink is used to analyze the performance assessment of a unique three-phase symmetric cascaded multilevel inverter-based reduced switch symmetrical inverter fed induction motor drive, brushless DC (BLDC) motor and grid has been verified. According to the findings the total harmonic distortion (THD) is found to be 15% for a three-phase system and as the number of levels increases to 17 level the THD is 7.10%.

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1. INTRODUCTION

Multilevel inverters (MLIs) have attracted a lot of attention in recent years for their potential use in electrical and industrial systems, as well as their high efficiency, simplicity of operation, and lack of electromagnetic interference (EMI). Additionally, MLIs may be quickly connected to renewable energy sources, including photovoltaic solar panels and wind turbines [1]–[3]. Numerous MLI topologies have been suggested by scholars since the 1970s. The 2-level inverter, which is the prevalent kind of inverter, has some disadvantages, including high total harmonic distortion (THD), the need for bulky filters, high voltage ratings for switches, high switchingfrequencies, and electromagnetic interference. In addition, because of the high voltage specification and stresson switches, the 2-level inverter will only be utilized for low and medium voltage applications. MLI is created to enable DC/AC conversion with much better efficiency and less THD [4]–[6] in order to get beyond these restrictions.

Reduced switch MLIs (RSMLI) are a class of MLIs that aim to reduce number of switch count required togenerate the multilevel waveform, thereby reducing complexity and cost of the circuit [7]–[10]. Reduced switch MLIs achieve this by using different techniques to synthesize the multilevel waveform with

fewer switches. This is done by utilizing various techniques such as capacitor voltage balancing, the flying capacitortechnique, or the diode-clamped technique. Reduced switch MLIs are used in high power applications such as motor drives, renewable energy sources (RES), and power grid applications [11]–[13]. These applications require high power efficiency, low harmonic distortion, and improved power quality, which are all benefits of MLIs.

In general, reduced switch MLIs outperform traditional 2-level inverters and are increasingly used in contemporary power electronics applications [14]–[16]. New topologies and control schemes are being developed and put into practice, and they remain a focus of ongoing research and development in the field of power electronics [17]–[19]. In this approach, a number of topologies with symmetric and asymmetric configurations were suggested. While in the latter, the magnitudes are diverse, in the former, all DC sources have the same magnitude. Various three phase multilevel inverter topologies were as presented in [20], [21]. Symmetric and asymmetric cascaded H-bridge topology was proposed in Khosroshahi [22].

Another form of MLI that has two separate components is a hybrid multilevel inverter. The level generation, or first phase, creates a staircase voltage with unidirectional polarity. To do this, a certain combination of DC source switches is used to generate a range of voltage levels. Second component changes the polarity, producing both positive and negative voltage across the load. Typically, an H-bridge inverter is employed for this. Traditional cascaded H-bridge MLI structure is seen in Figure 1. The (1) provides the number of switches needed for a certain output voltage level. There are a total of switches in each leg:

$$NSW = 2(N - 1) \quad (1)$$

where N = Number of levels.

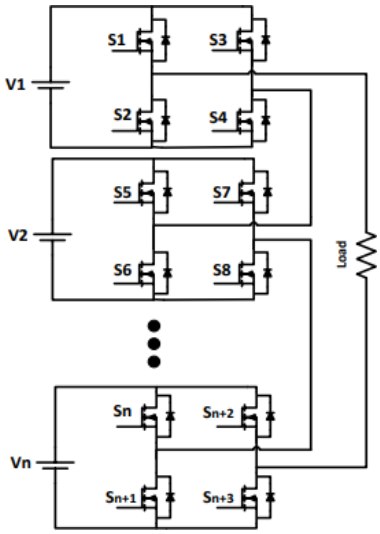

Figure 1. Conventional cascaded H-Bridge MLI

An enhanced topology based on cascaded H-bridge shown in Figure 2 was as introduced in previous researches [23]–[25].The number of switches and sources used can be determined using the equations provided which is given in (2) and (3) and the output voltage levels is dependent on the number of cells. Table 1 gives the comparison of the proposed system's switch requirements with those for the standard H-bridge at various levels. This topology significantly reduces the number of switches that are required when associated to the classical cascade H-bridge MLI. Comparing the switch count utilized in various MLI's with suggested MLI topologies is shown in Table 2.

$$N=2n+3 \quad (2)$$

$$K= N-2 \quad (3)$$

Where N = number of switches and n = number of sources.

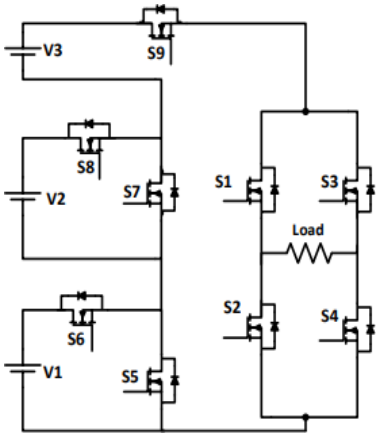

Figure 2. Hybrid cascaded H-bridge MLI

Table 1. Comparison of proposed system's switch requirements with those for the standard H-bridge at various levels

No. of levels	System	Switches required
7	Conventional H-Bridge	12
	Proposed MLI [12]	9
	Proposed MLI	8
9	Conventional H-Bridge	16
	Proposed MLI [12]	11
	Proposed MLI	9

2. PROPOSED REDUCED SWITCH COUNT MLI TOPOLOGY

The projected RSMLI fed induction motor drive strategy is depicted in Figure 3 and brushless DC (BLDC) motor load is shown in Figure 4 and grid connected shown in Figure 5. The Proposed RSMLI topology consists a typical H-bridge which is used as a polarity changing unit (PCU) to provide both +ve and -ve output voltage levels. The PCU is also in charge of producing a zero-voltage level at the output. This is done by turning on T2 and T4 at the same time for a certain amount of time. The switching states of the switches are listed in Table 2.

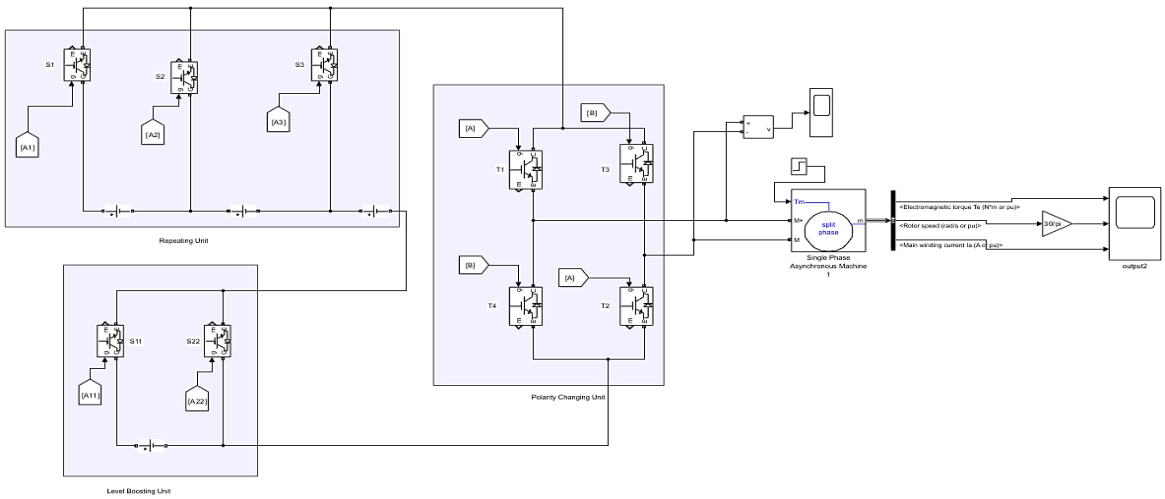

Figure 3. Single phase reduced switch MLI fed induction motor

For symmetrical arrangement, the suggested MLI is taken into consideration. The magnitude of the DC voltage sources determines the number of output voltage levels. The magnitude of each DC source, is chosen as V_{dc}. The current conduction path is shown in Figures 6-9. When switch S22 and S3 are turned ON voltage V1 appears. When switch S22 turned OFF and switch S11 turned ON along with switch S3 voltages

Va and V1 are connected in series and voltage 2 V_{dc} appears across the load. Now the switch S3 turned OFF and switch S2 ON along with switch S11 the voltages Va, V1 and V2 are in series and a total voltage of 3 V_{dc} appears across load. Switch S2 is turned OFF and switch S1 is turned ON along with switch S11 voltages Va, V1, V2 and V3 are in seriesso a total voltage of 4 V_{dc} appears across the load.

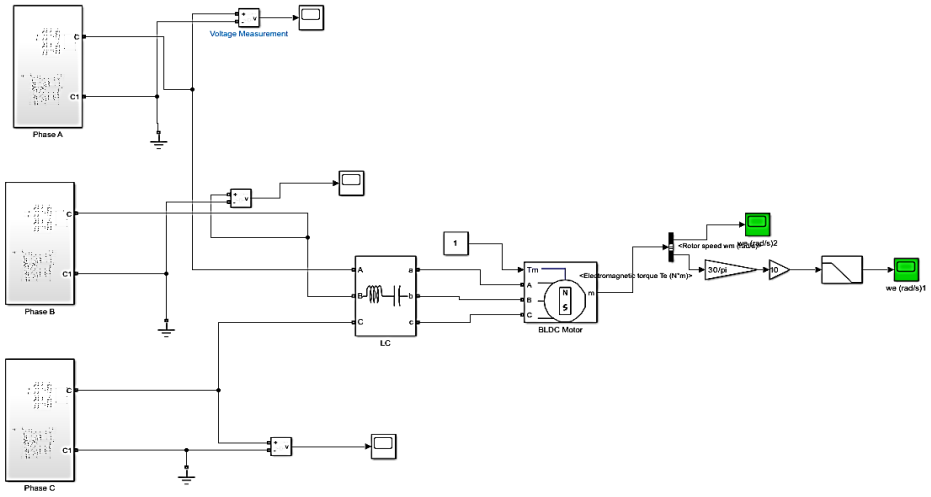

Figure 4. Three phase RSMLI fed BLDC motor

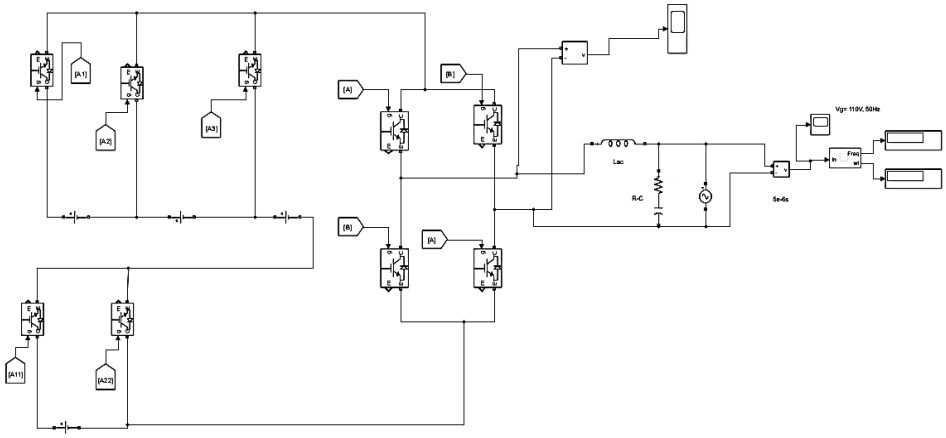

Figure 5. Grid connected single phase RSMLI

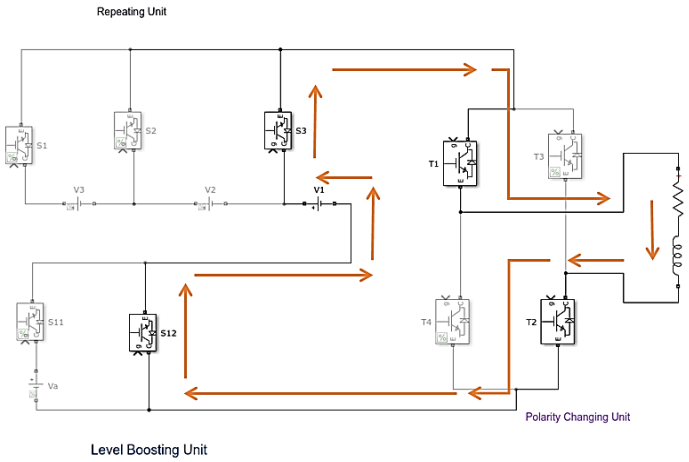

Figure 6. Current conduction path when Va Voltage is acting

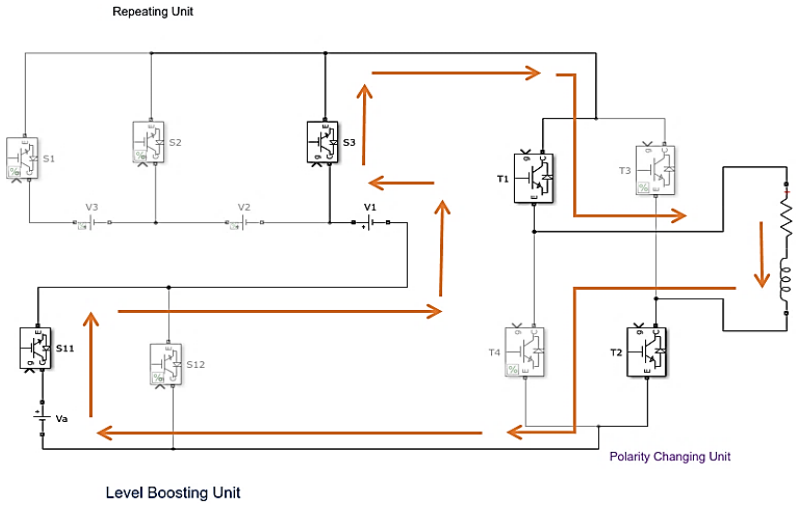

Figure 7. Current conduction path when V1 and Va Voltages are acting

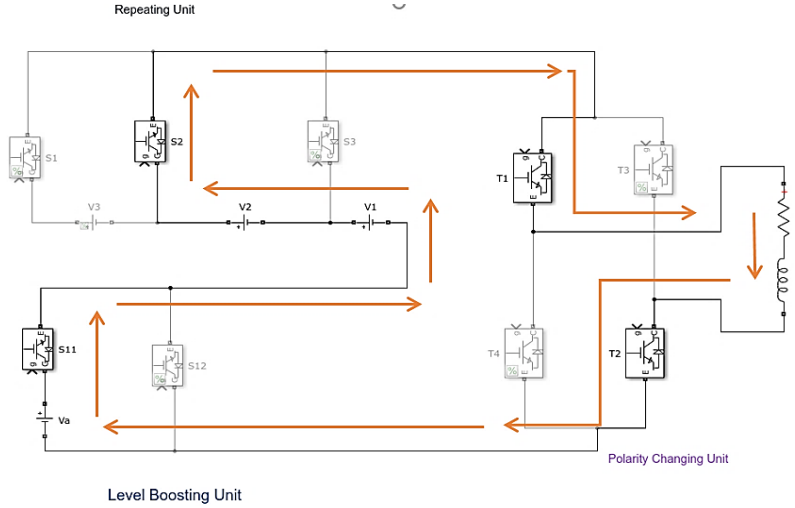

Figure 8. Current conduction path when V1, V2 and Va voltages are acting

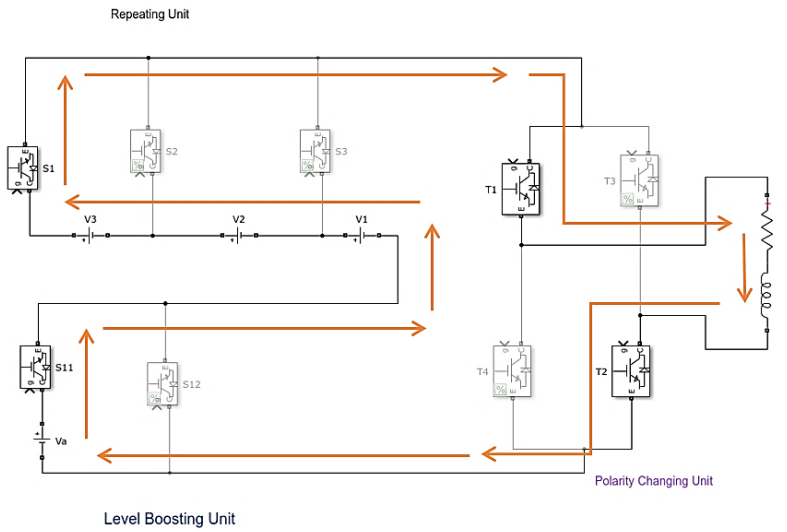

Figure 9. Current conduction path when V1, V2, V3 and Va voltages are acting

Table 2. Switching table with three repeating units

S1	S2	S3	S11	S12	T1	T2	T3	T4	V_0
0	0	1	0	1	1	1	0	0	+ V_{dc}
0	0	1	1	0	1	1	0	0	+2 V_{dc}
0	1	0	1	0	1	1	0	0	+3 V_{dc}
1	0	0	1	0	1	1	0	0	+4 V_{dc}
0	0	0	0	0	1	0	1	0	0
0	0	1	0	1	0	0	1	1	- V_{dc}
0	0	1	1	0	0	0	1	1	-2 V_{dc}
0	1	0	1	0	0	0	1	1	-3 V_{dc}
1	0	0	1	0	0	0	1	1	-4 V_{dc}

3. SIMULATION RESULTS

With a 10 ohm and 100 mH RL load, simulation is used to evaluate the performance of the proposed topology. The recommended topology is designed to work as 9-level single-phase and three-phase inverters. Figure 10 displays the simulation results for the proposed decreased switch count MLI architecture phase voltage for induction motor load, Figure 11 shows the output voltage for BLDC motor Load and Figure 12 depicts output voltage when RSMLI is grid connected and Figure 13 shows grid voltage. In the suggested design, pulse width modulation (PWM) pulses are produced using the multicarrier pulse width modulation technique (MCPWM) switching method with a carrier frequency of 1 kHz in order to achieve a 9-level output voltage. Figure 14 shows the %THD of the suggesteddecreased switch count MLI architecture for 9 levels. The% THD for various amplitude modulation indices isshown in Table 3.

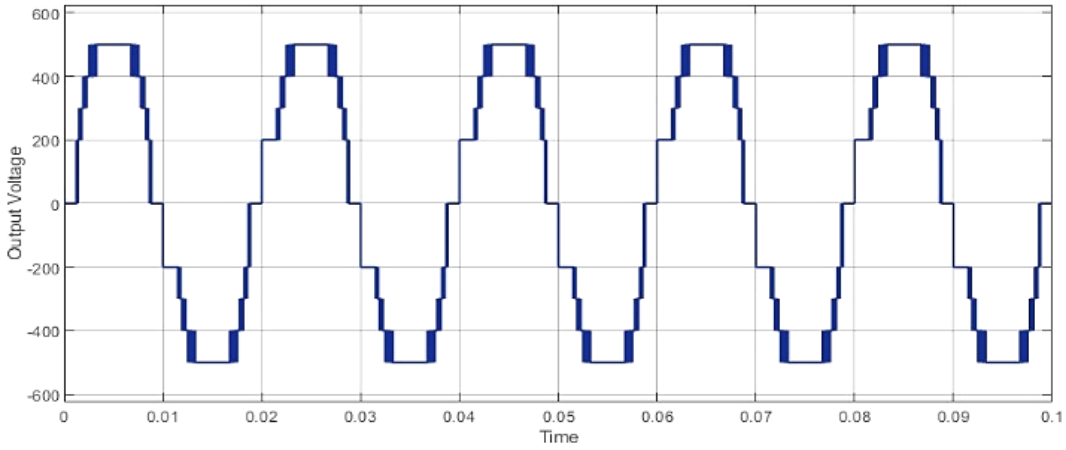

Figure 10. Output phase voltage waveform of the proposed topology with IM load

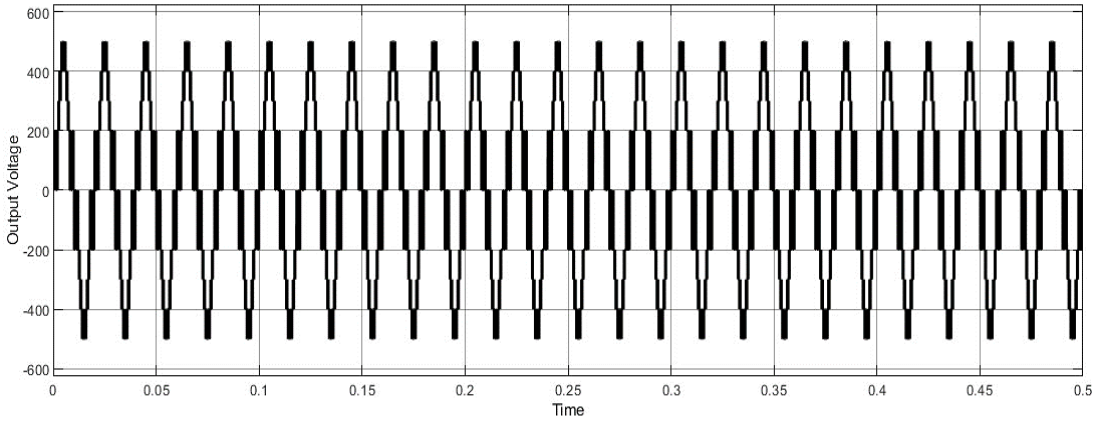

Figure 11. Output phase voltage waveform of RSMLI with BLDC motor load

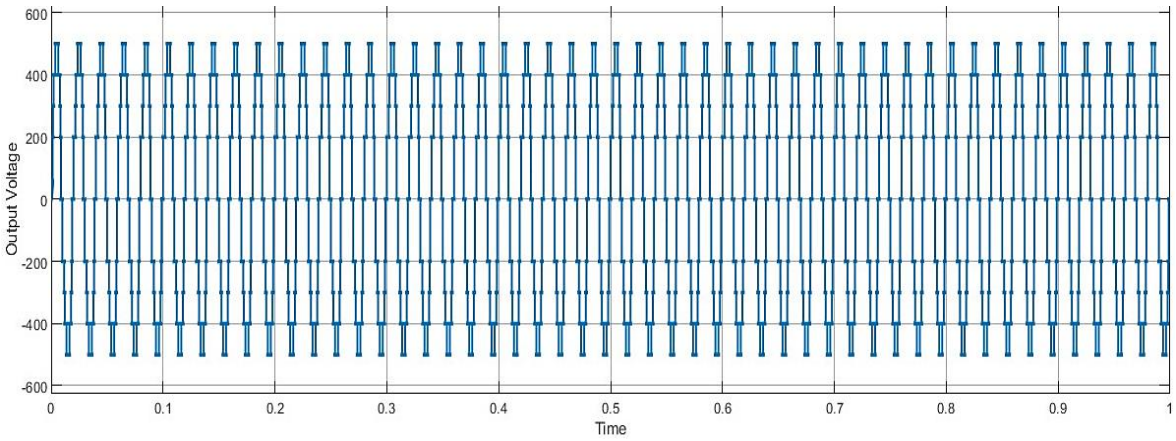

Figure 12. Output phase voltage waveform of RSMLI when grid connected

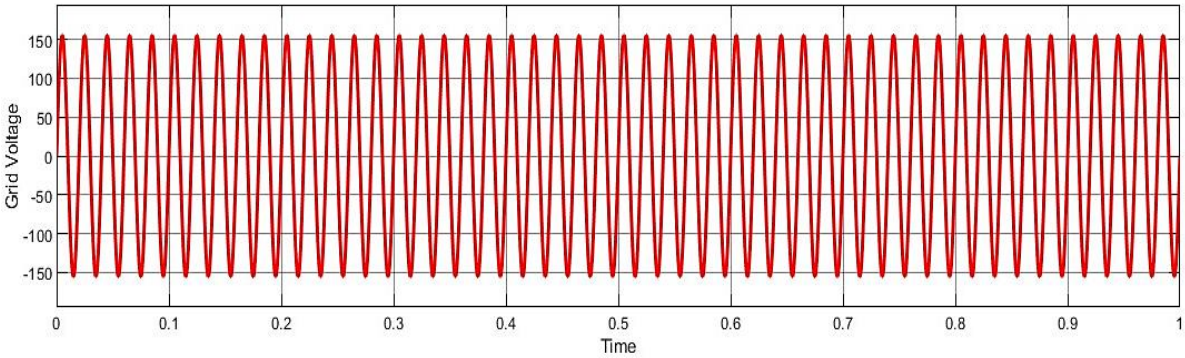

Figure 13. Grid voltage

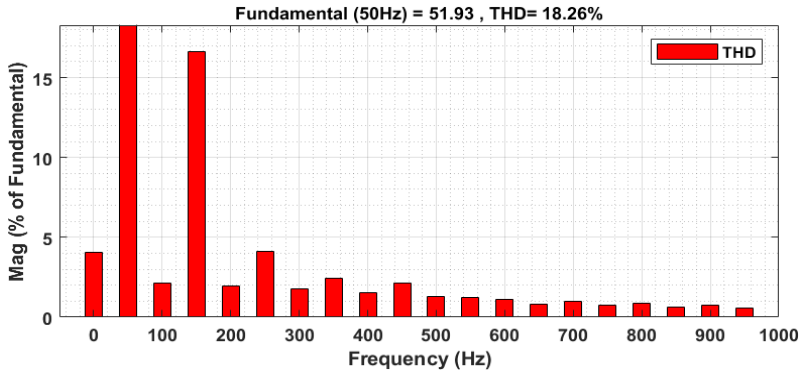

Figure 14. % THD for nine level RSMLI

The PWM generating strategy employed in the simulation investigation is shown in Figure 15. The PWM generating strategy is detailed for a single 9-level inverter that uses a single modulating waveform to produce positive and negative cycle pulses together with a 4-triangle carrier. To create the basic PWM pulses, the sine wave and every triangle component are evaluated and logically XORed. The switches in the suggested architecture are then given these base PWM pulses, which are used to synthesize each level of the output voltage. Figure 16. gives the simulation results of induction motor main winding current, auxiliary winding current, torque, and rotor speed. The graphs in Figures 17 and 18 compare the switch count to the number of levels for conventional and proposed topologies, respectively, and the number of levels to the percentage of THD.

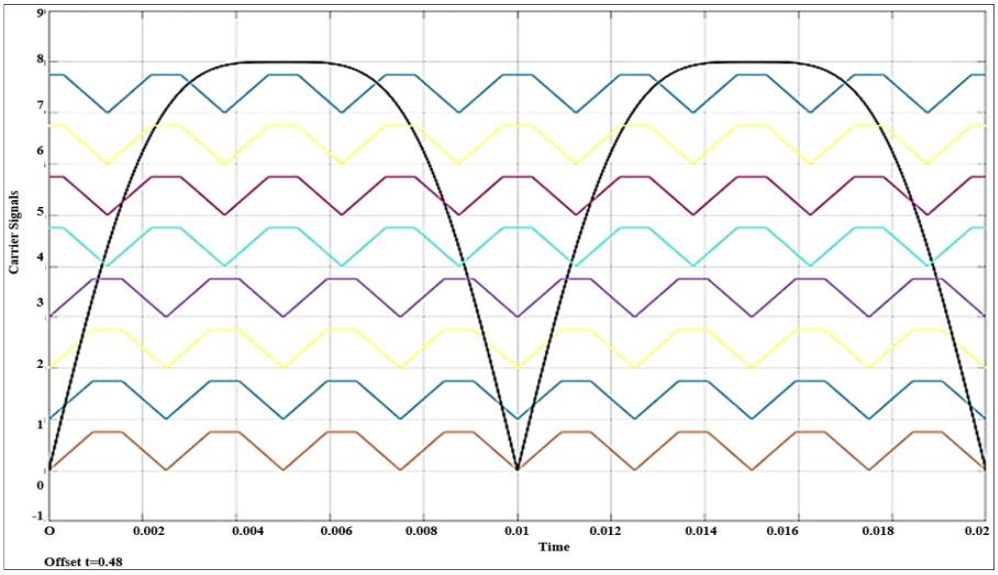

Figure 15. Phase disposition PWM with modified carrier

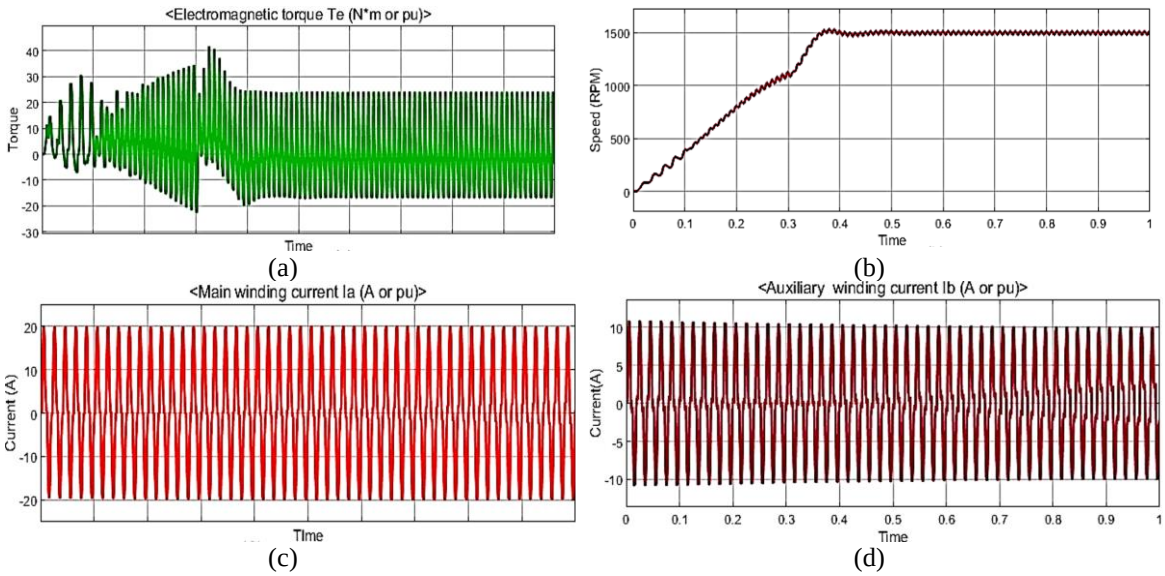

Figure 16. Simulation results of RSMLI fed induction motor drive (a) torque, (b) rotor speed, (c) main winding current, and (d) auxiliary winding current

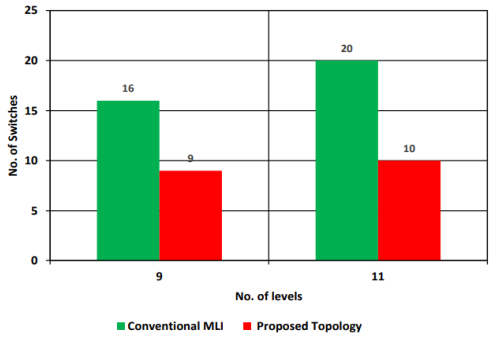

Figure 17. Graph showing no. of switches Vs no. of levels for conventional and proposed topology

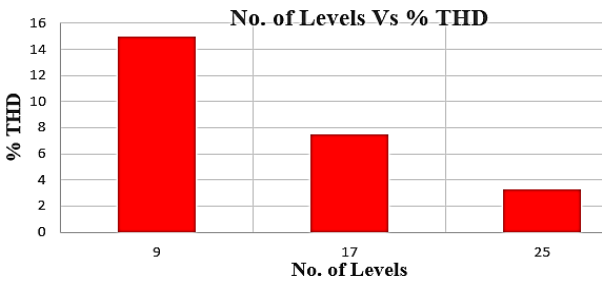

Figure 18. Graph showing no. of levels Vs %THD for proposed topology

4. CONCLUSION

To support high-power applications at medium voltage, a unique architecture has been developed. The reduction of the overall power components required for greater voltage levels for various loads is the major goal of this work. The multi-level inverter (MLI)'s revolutionary design makes use of four sources of direct current (dc). The present route of this design is intended to have fewer switches. In comparison to conventional topologies, the suggested architecture seeks to provide more voltage levels with fewer components. Along with the flow path,the operational modes necessary to produce nine tiers are thoroughly detailed. A single voltage source may beadded using just one switching device in the proposed topology, which reduces power loss by having fewer switches in the current conduction route.

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