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Solar PV based seventeen level reduced switch symmetrical multilevel inverter topology fed induction motor

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ABSTRACT

Multilevel inverters have received a lot of interest in recent years due to their ability to deliver more voltage levels than typical two-level inverters. Because of this property, multilevel inverters can produce output waveforms that closely resemble sinusoidal waveforms, lowering harmonic distortion dramatically. The emergence of reduced switch symmetrical multilevel inverter topologies has developed the curiosity of many different power conversion systems. These new topologies offer numerous advantages, including greater output voltage quality, fewer harmonic distortions, and increased power conversion efficiency. The inclusion of these inverters in the feeding of induction motors is one of their many prominent uses. A 17 levels of multi-level inverter (MLI) topology is presented with reduced switch count and harmonic reduction for power quality improvement. The inverter is fed by isolated equal photovoltaic panels which act as direct current or DC source. To reduce complexity, switching pulses are generated using hybrid pulse width modulation technique which is designed as controller. Through the use of MATLAB/Simulink, the performance assessment of a unique cascaded multilevel inverter-based reduced switch symmetrical inverter feeding an induction motor drive has been verified. The harmonic distortion with reduced switches obtained is 7.47% which is comparatively less than when compared with conventional cascaded H-bridge topology.

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1. INTRODUCTION

Multi-level inverter (MLI's) has received a lot of interest in recent years due to application potential in electrical and industrial systems, as well as their high efficiency, ease of operation, and lack of electromagnetic interference (EMI). MLIs can also be readily linked to a number of renewable energy sources, such as photovoltaic and wind turbines. Numerous MLI topologies and hybrid pulse width modulation techniques have been proposed since the 1970s [1]–[5]. Furthermore, due to the high voltage requirements and switch stress, the 2-level inverter will only be used for low and medium voltage applications. Multi-level inverter (MLI) was developed to enable DC/AC conversion with significantly higher efficiency and lower total harmonic distortion (THD) in order to overcome these limitations [6]–[8]. Reduced switch MLIs (RSMLI) are a type of MLI that aims to reduce the number of switching devices necessary to generate the multilevel waveform, lowering the circuit's cost and complexity. MLI's with fewer switches do this by employing various approaches to synthesize the multilevel waveform. This is accomplished by the use of several approaches such

as capacitor voltage balancing, the flying capacitor technique, and the diode-clamped technique. Reduced switch MLIs are commonly utilized in high power applications.

A hybrid DC link inverter with reduced power electronic switches and reduced THD is presented in [9], [10]. A cascaded converter based using hybrid cells and H-bridge structure were discussed in [11]. A new symmetric MLI topology with reduced switches were stated in [12], [13]. Novel modulation techniques to improve power quality were presented in [14], [15]. Harmonic analysis of wind driven system and PV system are given in [16], [17]. Authors [18]–[21] various three phase multilevel inverter topologies were presented. Symmetric and asymmetric cascaded H-bridge topology was proposed in [22]. Novel reduced switch topologies were presented in [23]–[25].

In this paper a new configuration is presented with reduced number of switches for solar photovoltaic (SPV) voltage source based 17 levels MLI. The proposed topology utilizes 18 switches which is less when compared to conventional cascaded H-bridge (CHB), neutral point clamped (NPC) and flying capacitor (FC) MLI topology. This generates 17 levels alternating current (AC) output voltage which not only reduces harmonics but also improves the power quality. Table 1 shows the comparison of the proposed topology over conventional for generating 9 levels output voltage.

Table 1. Comparison of the proposed system's switch requirements with those of conventional topologies

	NPC	FC	CHB	Proposed topology
No. of levels	9	9	9	9
Active switches	16	16	16	9
No. of sources	1	1	4	4
No. of diodes	12	--	--	--
DC bus capacitors	4	4	--	--
Balancing capacitors	--	6	--	--

2. PROPOSED REDUCED SWITCH COUNT MLI TOPOLOGY

The block diagram is shown in Figure 1. The proposed reduced switch multilevel inverter topology consists a typical H-bridge is used as a polarity changing unit (PCU) to provide both +ve and -ve voltage levels at the output. The PCU is also in charge of producing a zero-voltage level at the output. This is done by turning on T2 and T4 at the same time for a certain amount of time. The switching states of the switches are listed in Table 2.

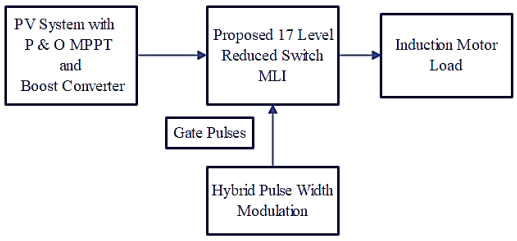

Figure 1. Block diagram of PV fed RSMLI fed induction motor

Table 2. 17 levels output voltage switching table

S1	S2	S3	S4	S5	S11	S22	S33	S44	S55	T1	T2	T3	T4	P1	P2	P3	P4	V0
0	0	0	0	1	0	0	0	0	0	1	1	0	0	1	0	1	0	+ V_{dc}
0	0	1	1	0	0	0	0	0	0	1	1	0	0	1	0	1	0	+ 2 V_{dc}
0	1	0	1	0	0	0	0	0	0	1	1	0	0	1	0	1	0	+ 3 V_{dc}
1	0	0	1	0	0	0	0	0	0	1	1	0	0	1	0	1	0	+ 4 V_{dc}
1	0	0	1	0	0	0	1	0	1	1	1	0	0	1	1	0	0	+ 5 V_{dc}
1	0	0	1	0	0	1	0	0	1	1	1	0	0	1	1	0	0	+ 6 V_{dc}
1	0	0	1	0	1	0	0	0	1	1	1	0	0	1	1	0	0	+ 7 V_{dc}
1	0	0	1	0	1	0	0	1	0	1	1	0	0	1	1	0	0	+ 8 V_{dc}
0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	0
0	0	0	0	1	0	0	0	0	0	0	0	1	1	0	1	0	1	- V_{dc}
0	0	1	1	0	0	0	0	0	0	0	0	1	1	0	0	1	0	- 2 V_{dc}
0	1	0	1	0	0	0	0	0	0	0	0	1	1	0	1	0	1	-3 V_{dc}
1	0	0	1	0	0	0	0	0	0	0	0	1	1	0	1	0	1	-4 V_{dc}
1	0	0	1	0	0	0	1	0	1	0	0	1	1	0	0	1	1	-5 V_{dc}
1	0	0	1	0	0	1	0	0	1	0	0	1	1	0	0	1	1	-6 V_{dc}
1	0	0	1	0	1	0	0	0	1	0	0	1	1	0	0	1	1	-7 V_{dc}
1	0	0	1	0	1	0	0	1	0	0	0	1	1	0	0	1	1	-8 V_{dc}

For symmetrical arrangement, the suggested MLI is taken into consideration. The magnitude of the DC voltage sources connected determines the number of output voltage levels. The magnitude of each DC source is chosen as volts direct current or V_{dc} in this mode and is taken from PV source which is shown in Figure 2.

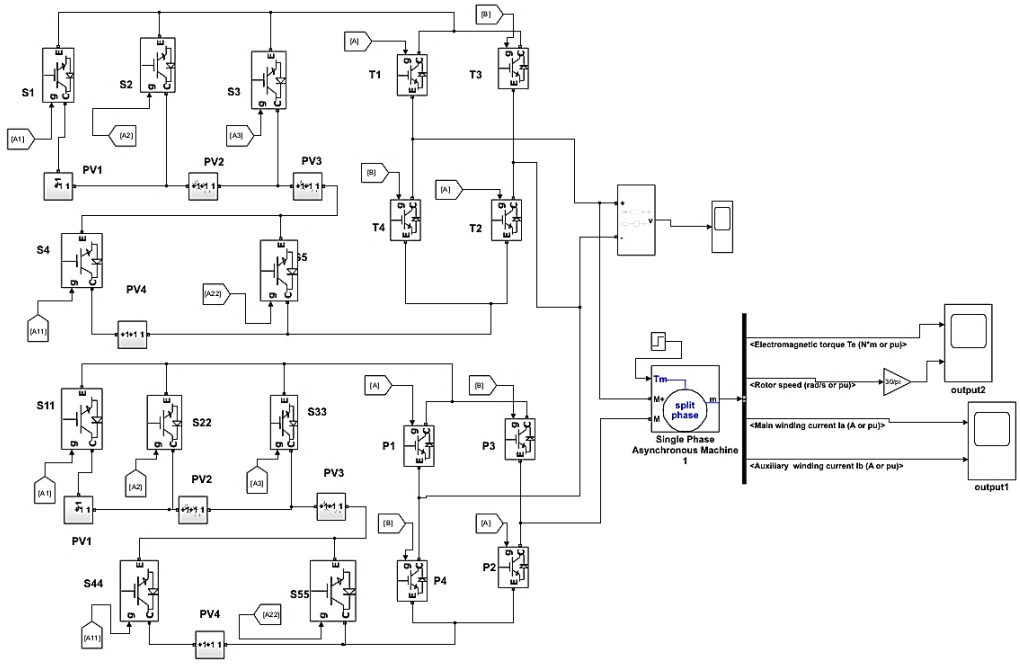

Figure 2. Block diagram of PV fed reduced switch MLI fed induction motor

3. PHOTOVOLTAIC SYSTEM

Photovoltaic (PV) systems have garnered significant attention due to their myriad advantages. These benefits encompass convenient allocation, extended lifespan, absence of noise pollution, swift installation, enhanced component portability and capability to generate power meeting peak load demands. As a result, PV systems find application across a broad spectrum of industrial uses. These include solar powered hybrid vehicles, battery charging setups, solar powered water pump, and more. Here a boost converter steps up the voltage that is obtained from PV which is shown in Figure 3. Perturb and observe is used to produce pulses for the boost converter. In Figure 4, the voltage and current characteristics, along with the voltage and power of PV1 are showcased. Figure 5 gives the output voltage of boost converter and it is found out to be 110 V.

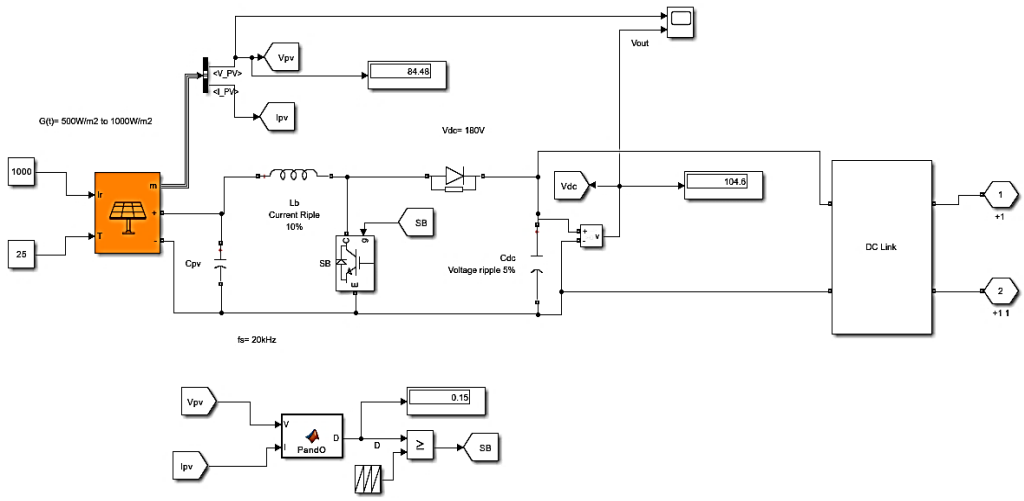

Figure 3. PV integration with boost converter

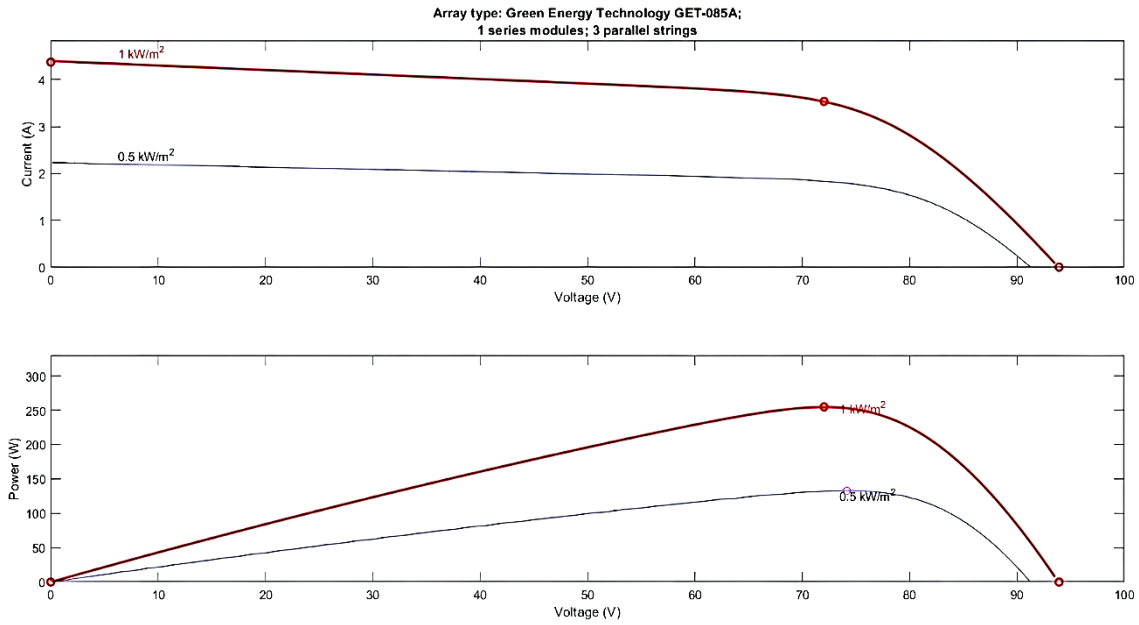

Figure 4. IV and PV characteristics of the system

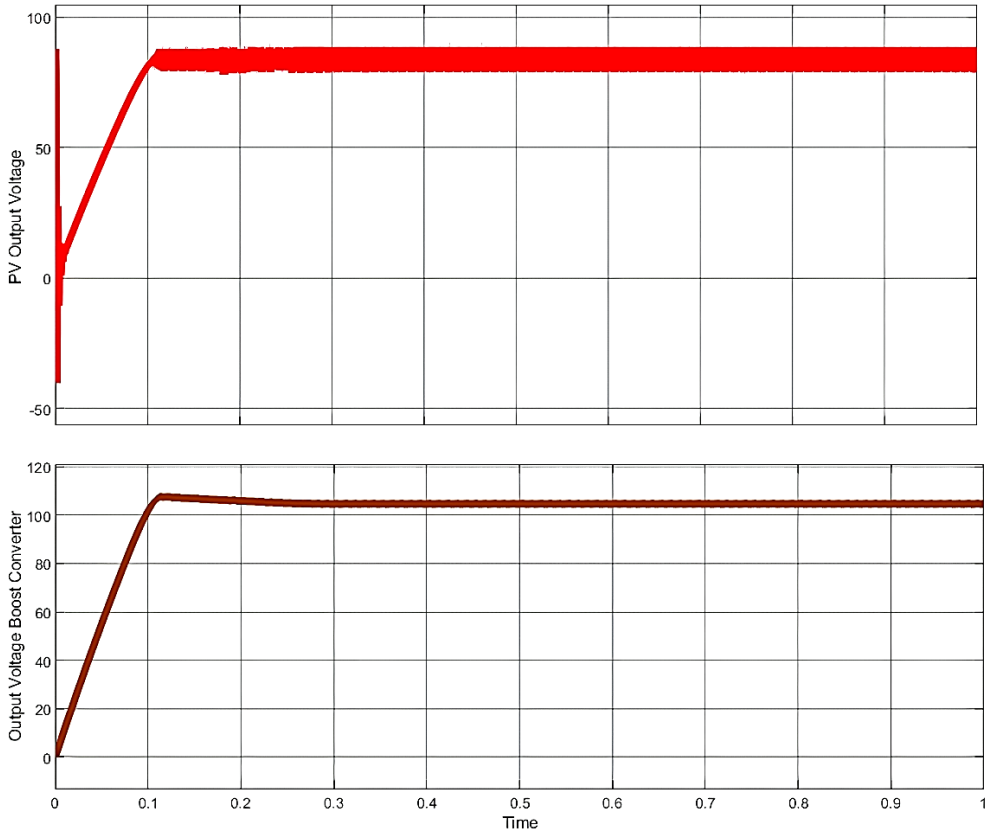

Figure 5. Output voltage of PV and boost converter

4. SIMULATION RESULTS

With a 10 ohm and 100 mH RL load, simulation is used to evaluate the performance of the proposed topology. The recommended topology is designed to work as 17 level single-phase and three-phase inverters. Figure 6 displays the simulation results for the proposed decreased switch count MLI architecture phase

voltage. In the suggested design, pulse-width modulated (PWM) pulses are produced using the multicarrier pulse width modulation (MCPWM) switching method with a carrier frequency of 1 kHz in order to achieve a 17 level output voltage. Figure 7 shows the %THD of the suggesteddecreased switch count MLI architecture for 17 levels. The %THD for various amplitude modulation indices isshown in Table 3.

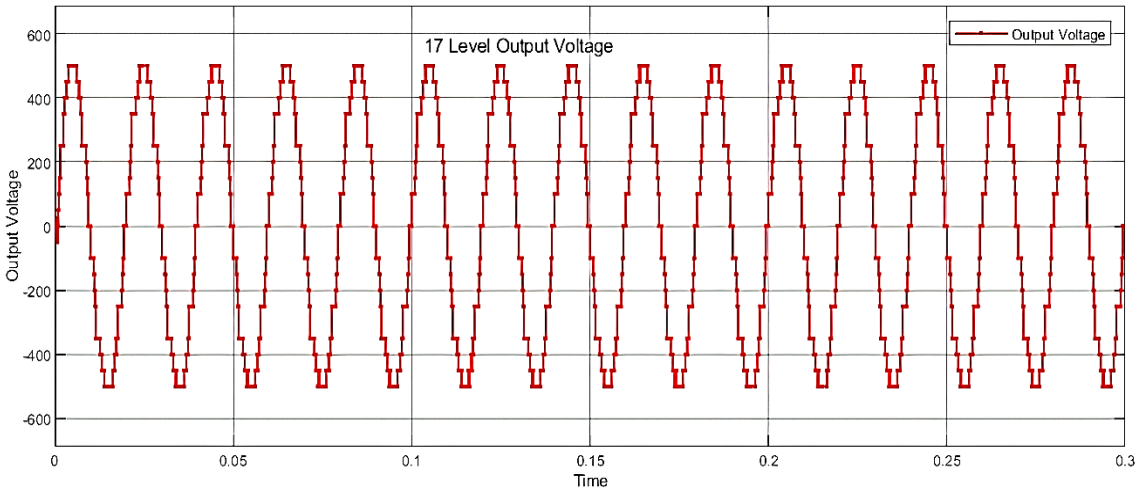

Figure 6. Output phase voltage waveform of the proposed topology

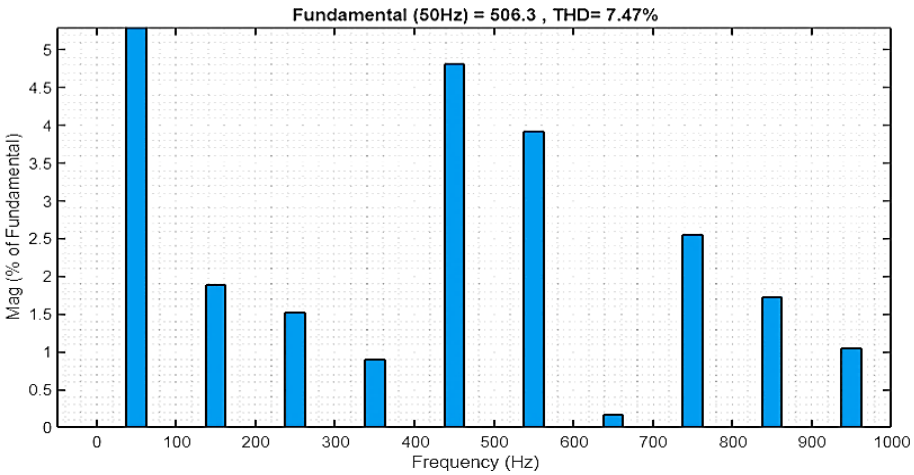

Figure 7. % THD for 17 levels output voltage of the proposed topology

Table 3. Output RMS voltage and % THD for various amplitude modulation index (m_a)

m_a	Vrms (v)	%THD
1	506.3	7.47
0.9	505.2	7.99
0.8	482.6	9.41
0.7	460	12.11

The PWM generating strategy employed in the simulation investigation is shown in Figure 8. The PWM generating strategy is detailed for a single 17 level inverter that uses a third harmonic single modulating waveform with 16-saturated triangle carrier waveforms. To create the basic PWM pulses, the sine wave and every triangle component are evaluated and logically XORed. The switches in the suggestedarchitecture are then given these base PWM pulses, which are used to synthesize each level of the output voltage. Figures 9(a) and 9(b) gives the electromagnetic torque speed of the induction motor. Figures 9(c) and 9(d) gives the main winding and auxiliary winding currents of the induction motor load.

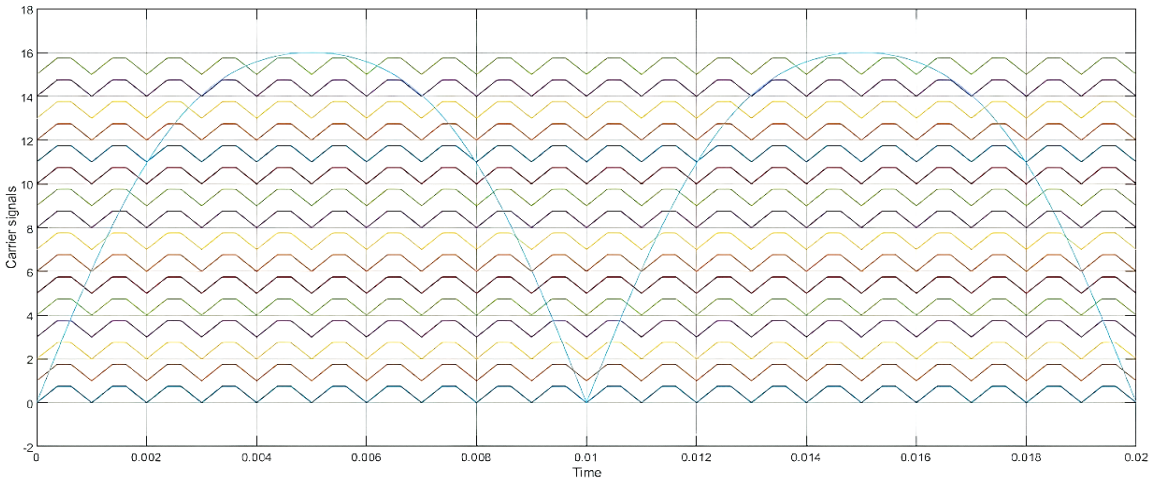

Figure 8. Phase disposition PWM with modified carrier

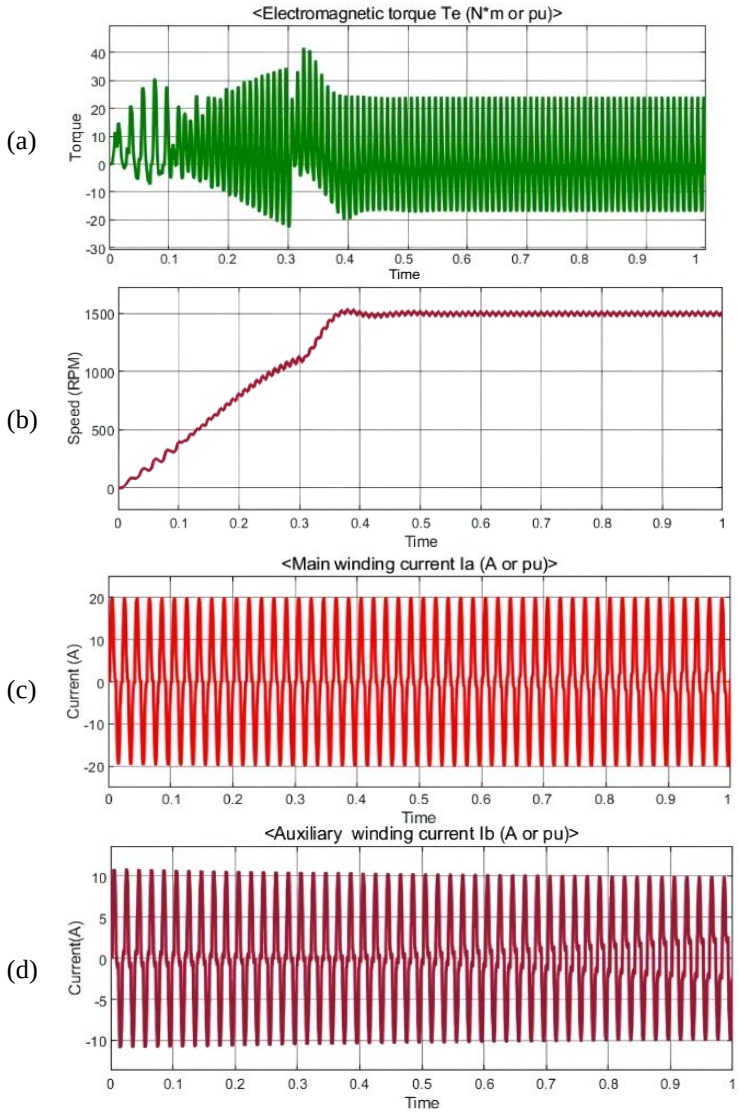

Figure 9. Simulation results of RSMLI fed induction motor drive: (a) torque, (b) rotor speed, (c) main winding current, and (d) auxiliary winding current

5. CONCLUSION

To support high-power applications at medium voltage, a unique architecture has been developed. The MLI's revolutionary design makes use of four sources of DC from PV. The reduction of the overall power components required for greater voltage levels and lesser THD is the major goal of this work. The THD obtained for the proposed topology is 7.47% whereas for cascaded H-bridge the total THD obtained is 9.10% with more number of switches. Along with the flow path, the operational modes necessary to produce seventeen tiers are thoroughly detailed.

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