International Journal of Power Electronics and Drive Systems (IJPEDS)
Vol. 15, No. 2, June 2024, pp. 993~1000
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v15.i2.pp993-1000

SHE PWM based 21 level inverters with hardware analysis

Annai Theresa Alphonse Arulappan[1], Malathi Selvaraj[2], Ambikapathy Aladian[3]
[1]Department of Electrical Engineering, Anna University, SRM Valliammai Engineering College, Chennai, India
[2]Department of Electrical and Electronic Engineering, SRM Valliammai Engineering College, Chennai, India
[3]Department of Electrical and Electronics Engineering, Galgotias College of Engineering and Technology, Greater Noida, India

Article Info

Article history:

Received Aug 22, 2023
Revised Nov 30, 2023
Accepted Dec 14, 2023

Keywords:

21 levels
Cascaded asymmetrical DC voltage source based MLI
Multilevel inverters
Selective harmonic elimination
Total harmonic distortion

ABSTRACT

Recently, the advancement of multilevel inverters (MLI) has been a crucial factor in high power and medium voltage applications. This MLI has multiple topologies and has been used in a variety of applications. Cascaded MLI is preferred over other forms of multilevel inverter topologies. Nonetheless, significant obstacles are encountered when implementing these topologies. They necessitate an increased number of switches, DC sources, capacitors, and diodes. Increased losses and total harmonic distortion (THD) will be present in the system. In addition, the MLI is more expensive. The better construction of a multilevel inverter results in more output levels with fewer switches, sources, and driver circuits, as well as low THD. A new single-phase cascaded asymmetrical DC voltage sources based multilevel inverter design and the selective harmonic elimination (SHE) approach are used to attain these goals. After confirming in MATLAB/Simulink, the hardware implementation of the multilevel inverter in 21 levels was completed in this article.

Corresponding Author:

Annai Theresa Alphonse Arulappan
Department of Electrical Engineering, Anna University, SRM Valliammai Engineering College
Chennai, Tamil Nadu, India
Email: srtheresasat@gmail.com

1. INTRODUCTION

The three-level converter [1] sparked the growth of the multilevel inverter. High-power industries have recently expressed a strong interest in multilevel inverters (MLI) [2], [3], [4]. In the absence of transformers or switches connected in series, large voltages with low harmonics can be produced through the careful arrangement of different voltage sources [5]. The three major multilevel inverter assemblies available in applications in industries with different DC sources are: i) diode clamped; ii) flying capacitor; and iii) cascaded H-bridge inverter [1], [6], [7]. The first topology was the series H-bridge design, however for the same topology, various other arrangements have been accomplished in [8], [9] and [2], [4] and [8]-[11]. Because the power conversion cells are arranged in series, measurements of the output voltage and power levels are simple. This design's obvious drawback is the substantial number of different voltage sources needed to supply each cell. The diode-clamped converter used the H-bridge architecture but added a series capacitor bank [12]. The capacitor-clamped switching cells in the flying capacitor multilevel architecture are connected in series [13]-[16]. When compared to the diode-clamped inverter, this architecture has several distinguishing and eye-catching characteristics. One benefit is the lack of a need for extra clamping diodes. Since the flying capacitor inverter provides switching redundancy inside the phase that may be used to balance the flying capacitors, just one DC supply is necessary as well. Another multilevel approach parallels the inverter phases using interphase reactors [13]. The semiconductors block the entire DC voltage in this configuration, but the load current is shared. In addition, a plethora of combinational designs have emerged, some of which include

the cascaded arrangement of fundamental topologies [17]-[19]. Due to the increasing effect of the level count, these designs could achieve a higher power quality than the fundamental topologies depending on the quantity of semiconductor switches. Some new designs were also proposed in [20]-[25] to reduce the number of discrete DC sources for high-voltage, high-power applications.

Unfortunately, multilevel inverters have some flaws. The requirement for a significant number of power switches is one peculiar difficulty. A multilevel converter still needs the associated gate driver and protection circuitry for each switch even when low-voltage rate switches are employed. As a result, the converter becomes more expensive and sophisticated. An effort was made to offer an innovative multilevel inverter topology that reduced the number of power switches and DC voltage sources in comparison to standard multilevel inverters [26]-[30]. These inverters required a large number of bidirectional switches to produce the output voltage with constant step levels.

After examining the drawbacks of the current arrangements, this study suggests a unique configuration for multilevel inverters with a large number of step levels associated with a small number of power switches. The newly proposed topology is comprised of four direct current sources, twelve switches, and twelve driving circuits. The suggested selective harmonic elimination (SHE) technique [19], [31], [32] is effective in eliminating the lowest order harmonics and producing a higher quality sinewave output waveform with an enhanced harmonic profile.

2. MULTILEVEL INVERTER

The MLI is a type of inverter circuit that raises the competence of the inverter setup, reduces the total harmonic distortion (THD) value of the inverter design, and reduces losses. The development of multilevel inverter technology began with the need to reduce the harmonic content present at the inverter output. As a result, it was practically carried out to meet the criteria of recognizing the inverters aimed at high voltage DC buses. However, either the switching devices were overly stressed or there was a lack of suitable voltage ratings to accommodate high voltage and high power inverters. Stress on switching devices could be justifiably decreased by incorporating cutting-edge technology into multilevel architectures. As a result, a high DC voltage level can be handled without the need for large, lossless step-up/down transformers [33]. By arranging the power semiconductor devices and the number of voltage sources, multilevel inverters can provide output voltages with multiple levels in the waveforms. The proposed work offers a new single-phase cascaded asymmetrical DC voltage sources based multilevel inverter design that may achieve a greater number of output levels while utilizing fewer switches, driver circuits, and DC voltage sources.

3. TWENTY-ONE LEVEL INVERTER PROPOSED

In recent years, electrical engineering experts have been very careful in constructing MLIs to obtain highly graded and reliable power for a variety of industrial applications. This paper explores a MLI based on a single-phase cascaded asymmetrical switched DC voltage source. A revolutionary multilevel inverter with the fewest switches is recommended here, and the output voltage level is enhanced up to 21 levels with low THD. Because we use fewer switches, the switching losses are also reduced. For a 21-level inverter, the recommended cascaded asymmetrical DC source-based multilevel inverter configuration has 12 power switches and 4 independent DC sources. The output voltage is divided into two components. The level creation portion on the left side is responsible for producing levels in both positive and negative polarities. The polarity production section on the right side is responsible for producing the polarity (+ or -) of the generated output voltage. The suggested innovative inverter connects the left and right portions to produce a multilevel output voltage waveform. The main goal of the proposed ACMLI configuration is to reduce electromagnetic interference, lower THD with the SHE method, and reduce switches compared to typical MLI. A classic one-phase 21-level inverter has forty switches, whereas the newly recommended method has only 12 switches that work on the same basis. The asymmetrical (4 separate DC voltage sources) cascaded H- bridge inverter is utilized here to achieve larger output levels. The PIC16F877A microcontroller is used to produce switch gate pulses. The SHE approach is employed in this proposed strategy to eliminate lower order harmonics while also increasing the efficiency of the MLI.

3.1. Operation of the topology proposed

Figure 1 depicts the proposed one-phase asymmetrical cascaded 21-level inverter topology. This inverter topology achieves 21 levels (0, +10, -10 levels) of output voltage as a stepped waveform. For achieving different voltage levels, the different switching states (i.e., ON, OFF states) of different switches are computed as shown in Table 1.

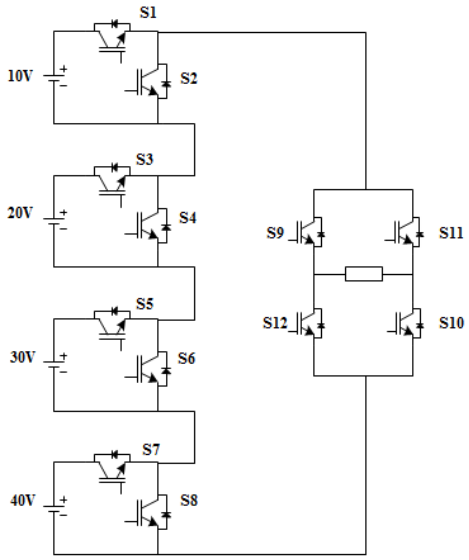

Figure 1. The 21-level single-phase asymmetrical cascade inverter that is being proposed

Table 1. Triggering states of proposed scheme

Output voltage level	Triggering states												Output voltage
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	
+10	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	ON	OFF	OFF	+100
+9	OFF	ON	ON	OFF	ON	OFF	ON	OFF	ON	ON	OFF	OFF	+90
+8	ON	OFF	OFF	ON	ON	OFF	ON	OFF	ON	ON	OFF	OFF	+80
+7	OFF	ON	OFF	ON	ON	OFF	ON	OFF	ON	ON	OFF	OFF	+70
+6	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	+60
+5	ON	OFF	OFF	ON	OFF	ON	ON	OFF	ON	ON	OFF	OFF	+50
+4	OFF	ON	OFF	ON	OFF	ON	ON	OFF	ON	ON	OFF	OFF	+40
+3	ON	OFF	ON	OFF	OFF	ON	OFF	ON	ON	ON	OFF	OFF	+30
+2	OFF	ON	ON	OFF	OFF	ON	OFF	ON	ON	ON	OFF	OFF	+20
+1	ON	OFF	OFF	ON	OFF	ON	OFF	ON	ON	ON	OFF	OFF	+10
0	OFF	ON	OFF	ON	OFF	ON	OFF	ON	ON	ON	OFF	OFF	0
-1	ON	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	ON	ON	-10
-2	OFF	ON	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	ON	-20
-3	ON	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	ON	-30
-4	OFF	ON	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	ON	ON	-40
-5	ON	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	ON	ON	-50
-6	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	-60
-7	OFF	ON	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	ON	ON	-70
-8	ON	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	ON	ON	-80
-9	OFF	ON	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	ON	-90
-10	ON	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	ON	-100

The standard method's output voltage levels are determined by: m = 2Ns + 1, where m represents the output voltage levels and Ns represents the individual inverter legs. The number of switches (l) required to complete m levels is known by: l = 2(m-1) for the execution of 21-level CMLI, and hence the total number of switches required in the usual technique is 40. The proposed design for a 21-level inverter shown here includes 12 switches and four separate DC sources. As an example, an old one-phase, 21-level inverter has 40 switches, whereas the newly proposed architecture has only 12 switches with the same logic. There are fewer gate driver circuits because there are fewer switches. As a result, the suggested design uses fewer components and less THD to convert the DC voltage to stepped wave AC.

3.2. Operation of the 21 level inverter hardware set up

A basic block diagram, which is shown in Figure 2, is used to show the hardware setup of the 21-level inverter. It consists of a power supply circuit, a main inverter circuit, a 12 V power supply, a control circuit, a driver circuit, and a load. The four asymmetrical DC voltages are connected at the inverter circuit's input. Using a regulated power supply, the four asymmetrical voltages (5 V, 10 V, 15 V, and 20 V DC) are extracted. A 230/12 V stepdown transformer converts the single- phase 230 V AC supply power to 12 V AC

voltage. A diode rectifier converts 12 V AC electricity to 12 V DC. The regulator IC 7805 achieves the 5 V controlled DC voltage. This 5 V DC power feeds into the control circuit, where the peripheral interface controller (PIC) microcontroller IC PIC16F877A generates switching signals using the selective harmonic elimination (SHE) approach. The driving circuit receives these triggering signals. A 230/12 V stepdown transformer converts the single phase 230 V AC supply power to 12 V AC voltage. A diode rectifier converts 12 V AC electricity to 12 V DC. The regulator IC 7805 achieves the 5 V controlled DC voltage.

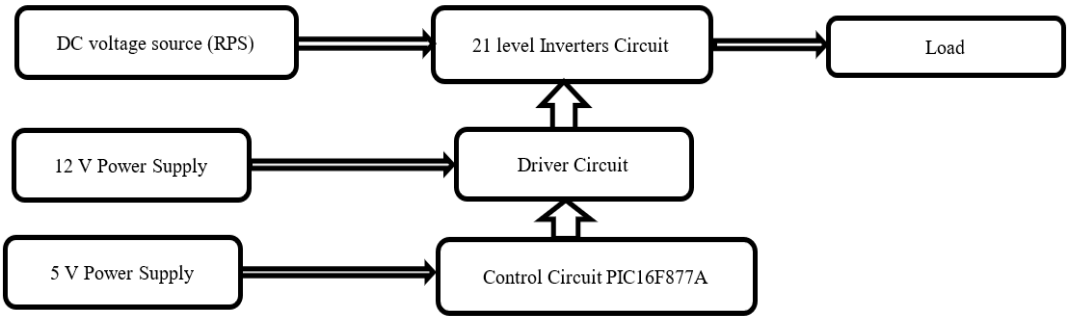

Figure 2. Block diagram of the proposed 21-level inverter

The primary multilevel inverter circuit's MOSFETs are turned ON and OFF in response to the triggering pulses received from the driver circuit, allowing the desired multilevel output to be achieved. A single-phase cascaded asymmetrical switched DC voltage source- based MLI is constructed with 8 MOSFETs and a 10 level DC voltage output. The main circuit also includes an H- bridge with four more MOSFETs, and its output is a 21-level AC output voltage because the H- bridge works as a polarity shifter, causing the voltage level to be positive (+) or negative (-). As a result, we receive the main inverter circuit's 21-level AC output voltage. The load receives the resulting 21-level AC output voltage. The 750 Ω rheostat is employed as the load in this case.

4. RESULT ANALYSIS

In MATLAB/Simulink, the circuit for a 21-level inverter is simulated and its outputs (such as load voltage and current) are acquired. There are just 12 switches and 4 DC sources employed in this innovative method. With just four DC sources, the output voltage level is higher when asymmetrical DC sources are used. The circuit solves its complexity by avoiding the use of capacitors and diodes. Because the SHE approach is employed, the THD% is decreased because the lower order harmonics are significantly reduced. Thus, we are able to achieve our goal of designing a unique inverter with fewer components and lower THD. The simulation circuit, the gate pulses that must be given to the MOSFETs, and the output voltage and current for the R load are all displayed in the following section. The outputs obtained through simulation are additionally validated using a hardware implementation.

4.1. Simulation results

The circuit used to mimic the suggested inverter, gating pulses, and output voltage and current are shown in Figures 3, 4, 5, and 6. The SHE technique is used to generate the gate pulses for the eight MOSFETs. In the H-bridge (polarity generator), two MOSFET switches from separate arms (S9, S10 or S11, S12) can operate simultaneously. The MATLAB subsystem contains the digital switching sequences. The output voltage and current are in phase since the circuit is simulated for an R load. The output voltage obtained is 100 V and current is 1 A. The suggested 21-level inverter's THD, shown in Figure 7, is 12.64%.

4.2. Hardware results

The experimental setup depicted in Figure 8 validates the output at level 21 of the suggested level 21 inverter. DC voltage sources are in the ratio 1:2:3:4 (i.e) with 5 V, 10 V, 15 V, and 20 V, correspondingly. The regulated power supplies are used here as DC sources. The switching pulses generated by SHE technique and the 21-level output voltage waveform in CRO are shown in Figure 9. A 750 Ω rheostat is connected as a resistive load.

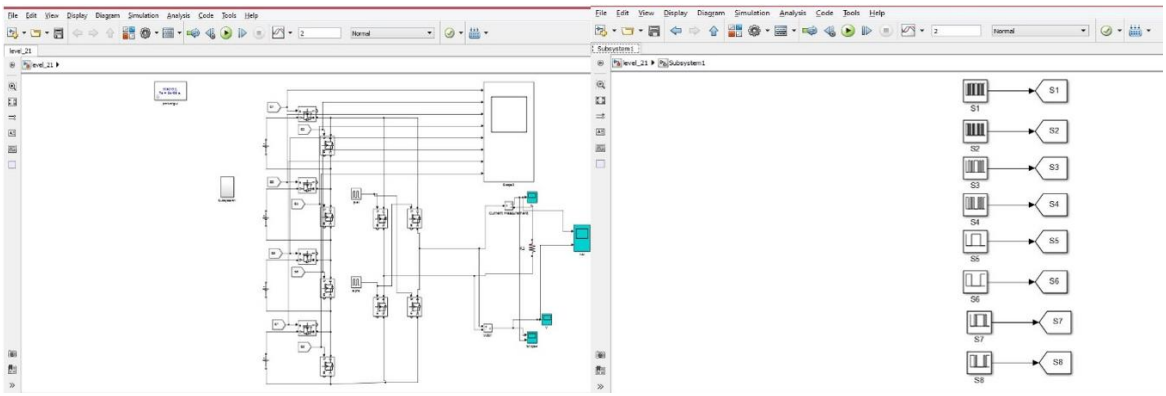

Figure 3. Simulation circuit of the recommended 21 level inverters with the subsystem

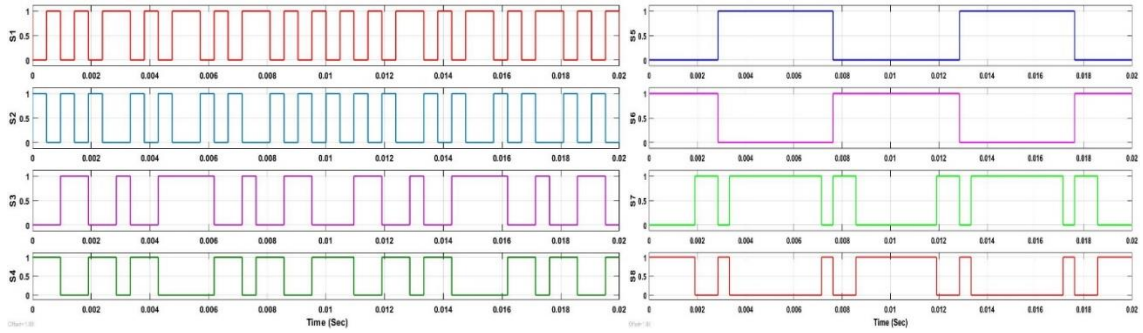

Figure 4. Gate pulses for the eight MOSFET switches

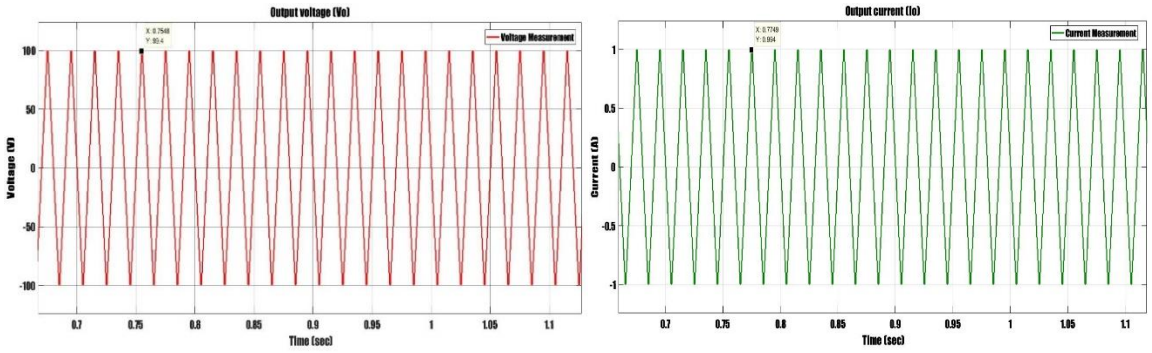

Figure 5. The unique output voltage and current of 21-level inverter at 21 levels

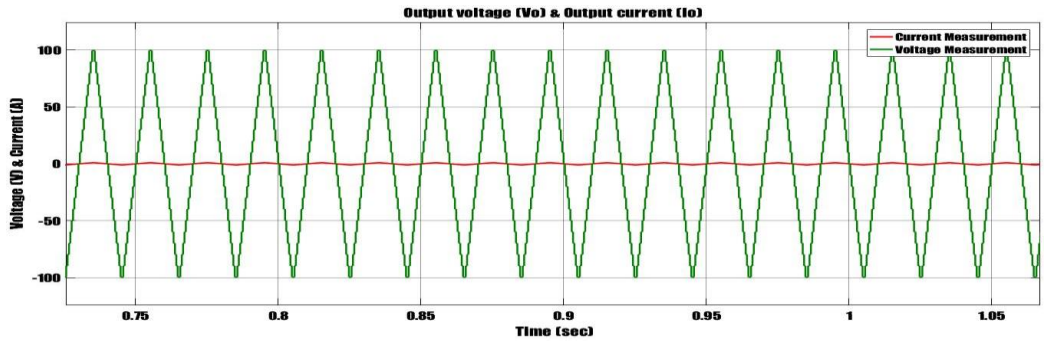

Figure 6. The output voltage and current of a unique 21-level inverter displayed in a single scope

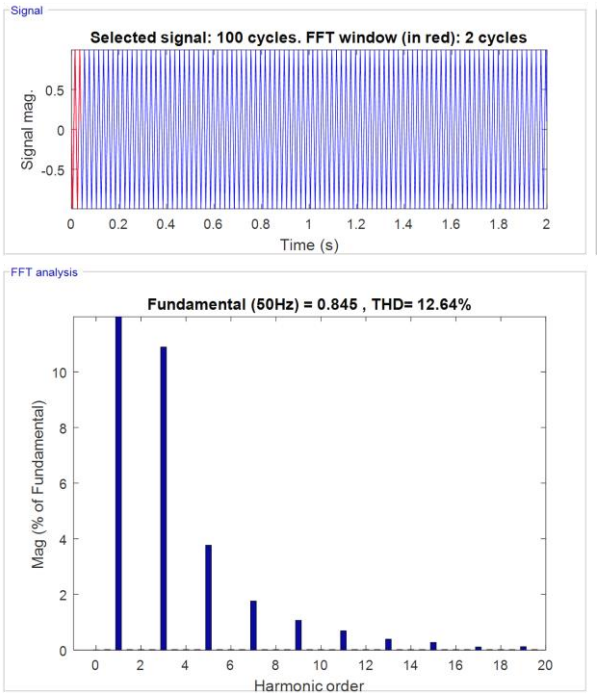

Figure 7. THD of the suggested 21 level inverters

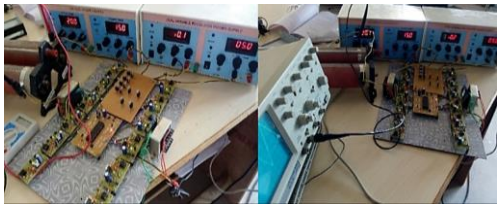

Figure 8. Experimental hardware setup of the projected 21 level inverters

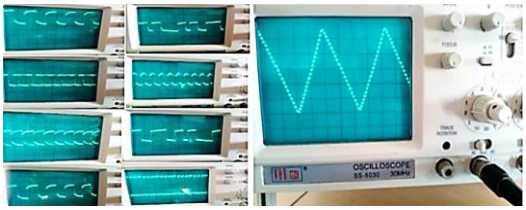

Figure 9. Gate pulses and the 21-level output voltage of the experimental setup

4.3. Hardware specifications

The hardware components used for building the 21 level inverter is given in Table 2. The experimental setup's affordability and simplicity are demonstrated by the provided specifications. The following parts are primarily needed for the main circuit, control circuit, and driver circuit of the suggested 21-level inverter.

Table 2. Components specifications

S. No	Component	Specifications
1	MOSFET	IRF 540 N
2	Diode	IN4007
3	Opto-coupler	6N137
4	Transformer	230/12 V, Step down
5	Capacitor	25 V, 1000 µF
6	Voltage regulator	7812, 7805
7	PIC Microcontroller	PIC16F877A
8	Crystal Oscillator	KDS 20.000 MHz

5. CONCLUSION

A novel MLI topology with a 21-level output voltage is displayed in this document. To provide the high- level voltage output, an asymmetric DC source configuration was used. The configuration used in this paper is made to allow the suggested architecture to produce a full cycle of AC voltage with both negative and

positive half cycles. The conventional polarity changer circuit is thus no longer necessary. In addition, switching losses have decreased due to the reduction from 40 to 12 switches, which lowers the cost of the devices. Additionally, there are a lot less DC sources and gate driver circuits. Additionally, the SHE PWM strategy has made THD reduction effective. Harmonic analysis was performed using the software MATLAB/Simulink. The method was successfully put into practice, and the result was verified using the hardware setup.

REFERENCES

[1] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724–738, Aug. 2002, doi: 10.1109/TIE.2002.801052.

[2] V. F. Pires, A. Cordeiro, D. Foito, J. F. Silva, and E. Romero-Cadaval, "Cascaded multilevel structure with three-phase and single-phase H-bridges for open-end winding induction motor drive," *IEEE Open Journal of the Industrial Electronics Society*, vol. 4, pp. 346–361, 2023, doi: 10.1109/OJIES.2023.3309652.

[3] E. Robles, M. Fernandez, J. Zaragoza, I. Aretxabaleta, I. M. De Alegria, and J. Andreu, "Common-mode voltage elimination in multilevel power inverter-based motor drive applications," *IEEE Access*, vol. 10, pp. 2117–2139, 2022, doi: 10.1109/ACCESS.2021.3137892.

[4] C. I. Odeh, A. Lewicki, and M. Morawiec, "A single-carrier-based pulse-width modulation template for cascaded H-bridge multilevel inverters," *IEEE Access*, vol. 9, pp. 42182–42191, 2021, doi: 10.1109/ACCESS.2021.3065743.

[5] A. A. Theresa, K. Kalpana, and M. Nirmala, "A novel 31 level cascaded H-bridge inverter," in *2021 International Conference on Advance Computing and Innovative Technologies in Engineering, ICACITE 2021*, IEEE, Mar. 2021, pp. 228–233. doi: 10.1109/ICACITE51222.2021.9404703.

[6] R. Raushan, B. Mahato, and K. C. Jana, "Optimum structure of a generalized three-phase reduced switch multilevel inverter," *Electric Power Systems Research*, vol. 157, pp. 10–19, Apr. 2018, doi: 10.1016/j.epsr.2017.11.017.

[7] K. K. Gupta and S. Jain, "A novel multilevel inverter based on switched dc sources," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 7, pp. 3269–3278, Jul. 2014, doi: 10.1109/TIE.2013.2282606.

[8] A. Lewicki, C. Odeh, and M. Morawiec, "Space vector pulsewidth modulation strategy for multilevel cascaded H-bridge inverter with DC-link voltage balancing ability," *IEEE Transactions on Industrial Electronics*, vol. 70, no. 2, pp. 1161–1170, Feb. 2023, doi: 10.1109/TIE.2022.3158005.

[9] S. Shuvo, E. Hossain, T. Islam, A. Akib, S. Padmanaban, and M. Z. R. Khan, "Design and hardware implementation considerations of modified multilevel cascaded H-bridge inverter for photovoltaic system," *IEEE Access*, vol. 7, pp. 16504–16524, 2019, doi: 10.1109/ACCESS.2019.2894757.

[10] A. Poorfakhraei, M. Narimani, and A. Emadi, "A review of multilevel inverter topologies in electric vehicles: Current status and future trends," *IEEE Open Journal of Power Electronics*, vol. 2, pp. 155–170, 2021, doi: 10.1109/OJPEL.2021.3063550.

[11] M. D. Siddique, A. Iqbal, M. A. Memon, and S. Mekhilef, "A new configurable topology for multilevel inverter with reduced switching components," *IEEE Access*, vol. 8, pp. 188726–188741, 2020, doi: 10.1109/ACCESS.2020.3030951.

[12] Y. He, Y. Liu, C. Lei, and J. Liu, "Equivalent space vector output of diode clamped multilevel inverters through modulation wave decomposition under carrier-based PWM strategy," *IEEE Access*, vol. 8, pp. 104918–104932, 2020, doi: 10.1109/ACCESS.2020.2999879.

[13] R. Sun, X. Wang, and Y. Ye, "Seventeen-level inverter based on switched-capacitor and flying-capacitor-fed T-type unit," *IEEE Access*, vol. 10, pp. 33561–33570, 2022, doi: 10.1109/ACCESS.2022.3161949.

[14] G. Kampitsis, E. I. Batzelis, P. D. Mitcheson, and B. C. Pal, "A clamping-circuit-based voltage measurement system for high-frequency flying capacitor multilevel inverters," *IEEE Trans Power Electron*, vol. 37, no. 10, pp. 12301–12315, Oct. 2022, doi: 10.1109/TPEL.2022.3174062.

[15] G. Kampitsis, E. I. Batzelis, A. Kolokasis, E. Matioli, and B. C. Pal, "A generalized phase-shift PWM extension for improved natural and active balancing of flying capacitor multilevel inverters," *IEEE Open Journal of Power Electronics*, vol. 3, pp. 621–634, 2022, doi: 10.1109/OJPEL.2022.3209540.

[16] C. Garcia *et al.*, "FCS-MPC based pre-filtering stage for computational efficiency in a flying capacitor converter," *IEEE Access*, vol. 9, pp. 111039–111049, 2021, doi: 10.1109/ACCESS.2021.3103070.

[17] G. Zhang and J. Yu, "Open-circuit fault diagnosis for cascaded H-bridge multilevel inverter based on LS-PWM technique," *CPSS Transactions on Power Electronics and Applications*, vol. 6, no. 3, pp. 201–208, Sep. 2021, doi: 10.24295/CPSSTPEA.2021.00018.

[18] S. S. Lee, "Single-stage switched-capacitor module (S 3 CM) topology for cascaded multilevel inverter," *IEEE Trans Power Electron*, vol. 33, no. 10, pp. 8204–8207, Oct. 2018, doi: 10.1109/TPEL.2018.2805685.

[19] U. T. Shami *et al.*, "Selective harmonic elimination notch angle calculation using THD and ZHF benchmarks for cascaded multilevel inverters," *IEEE Access*, vol. 11, pp. 116497–116510, 2023, doi: 10.1109/ACCESS.2023.3324557.

[20] P. Omer, J. Kumar, and B. S. Surjan, "A review on reduced switch count multilevel inverter topologies," *IEEE Access*, vol. 8, pp. 22281–22302, 2020, doi: 10.1109/ACCESS.2020.2969551.

[21] P. R. Bana, K. P. Panda, R. T. Naayagi, P. Siano, and G. Panda, "Recently developed reduced switch multilevel inverter for renewable energy integration and drives application: topologies, comprehensive analysis and comparative evaluation," *IEEE Access*, vol. 7, pp. 54888–54909, 2019, doi: 10.1109/ACCESS.2019.2913447.

[22] M. A. Rezaei, M. Nayeripour, J. Hu, S. S. Band, A. Mosavi, and M. H. Khooban, "A new hybrid cascaded switched-capacitor reduced switch multilevel inverter for renewable sources and domestic loads," *IEEE Access*, vol. 10, pp. 14157–14183, 2022, doi: 10.1109/ACCESS.2022.3146256.

[23] M. D. Siddique, S. Mekhilef, N. M. Shah, A. Sarwar, A. Iqbal, and M. A. Memon, "A new multilevel inverter topology with reduce switch count," *IEEE Access*, vol. 7, pp. 58584–58594, 2019, doi: 10.1109/ACCESS.2019.2914430.

[24] S. Kakar, S. B. M. Ayob, A. Iqbal, N. M. Nordin, M. Saad Bin Arif, and S. Gore, "New asymmetrical modular multilevel inverter topology with reduced number of switches," *IEEE Access*, vol. 9, pp. 27627–27637, 2021, doi: 10.1109/ACCESS.2021.3057554.

[25] M. D. Siddique, S. Mekhilef, N. M. Shah, and M. A. Memon, "Optimal design of a new cascaded multilevel inverter topology with reduced switch count," *IEEE Access*, vol. 7, pp. 24498–24510, 2019, doi: 10.1109/ACCESS.2019.2890872.

[26] M. A. Hosseinzadeh, M. Sarebanzadeh, C. F. Garcia, E. Babaei, and J. Rodriguez, "An asymmetric switched-capacitor multicell inverter with low number of DC source and voltage stress for renewable energy sources," *IEEE Access*, vol. 10, pp. 30513–30525, 2022, doi: 10.1109/ACCESS.2022.3140786.

[27] M. D. Siddique *et al.*, "A single DC source nine-level switched-capacitor boost inverter topology with reduced switch count," *IEEE Access*, vol. 8, pp. 5840–5851, 2020, doi: 10.1109/ACCESS.2019.2962706.
[28] Y. Wang, K. Wang, G. Li, F. Wu, K. Wang, and J. Liang, "A generalized switched-capacitor step-up multilevel inverter employing single DC source," *CSEE Journal of Power and Energy Systems*, vol. 8, no. 2, pp. 439–451, 2022, doi: 10.17775/CSEEJPES.2020.06280.
[29] K. Panda, P. Bana, O. Kiselychnyk, J. Wang, and G. Panda, "A single-source switched-capacitor-based step-up multilevel inverter with reduced components," *IEEE Trans Ind Appl*, vol. 57, no. 4, pp. 3801–3811, Jul. 2021, doi: 10.1109/TIA.2021.3068076.
[30] M. Trabelsi, H. Vahedi, and H. Abu-Rub, "Review on single-DC-source multilevel inverters: topologies, challenges, industrial applications, and recommendations," *IEEE Open Journal of the Industrial Electronics Society*, vol. 2, pp. 112–127, 2021, doi: 10.1109/OJIES.2021.3054666.
[31] G. Schettino, C. Nevoloso, R. Miceli, A. O. Di Tommaso, and F. Viola, "Impact evaluation of innovative selective harmonic mitigation algorithm for cascaded H-bridge inverter on IPMSM drive application," *IEEE Open Journal of Industry Applications*, vol. 2, pp. 347–365, 2021, doi: 10.1109/OJIA.2021.3130288.
[32] M. Tariq, D. Upadhyay, S. A. Khan, W. Alhosaini, P. Peltoniemi, and A. Sarwar, "Novel integrated NLC-SHE control applied in cascaded nine-level H-bridge multilevel inverter and its experimental validation," *IEEE Access*, vol. 11, pp. 22209–22220, 2023, doi: 10.1109/ACCESS.2023.3244215.
[33] G. K. Srinivasan, M. Rivera, V. Loganathan, D. Ravikumar, and B. Mohan, "Trends and challenges in multi-level inverter with reduced switches," *Electronics (Switzerland)*, vol. 10, no. 4, pp. 1–23, Feb. 2021, doi: 10.3390/electronics10040368.

BIOGRAPHIES OF AUTHORS

Annai Theresa Alphonse Arulappan is a full-time research scholar in Electrical Engineering, Anna University, SRM Valliammai Engineering College, Chennai, Tamil Nadu, India. She received her B.E. in electrical and electronics engineering in 2010 from V.R.S College of Engineering and Technology, Tamil Nadu, India, she pursued her M. Tech. in power electronics and drives in 2015 from SRM University, Chennai, Tamil Nadu, India. She is the silver medalist in both her UG and PG degrees. She also has done diploma in philosophy in the Institute Mater Dei, Goa connected with JDV, Pune. She has experience of 13 years in teaching. She has published international journals and filed patent. She also has a granted patent. Her research interests include the field of power electronics, power electronic converters, motor drives, industrial applications. She can be contacted at email: srtheresasat@gmail.com.

Malathi Selvaraj is an associate professor in the Department of Electrical and Electronics Engineering at SRM Valliammai Engineering College, Kattangulathur, Kanchipuram, India. She received her B.E in instrumentation and control engineering in 2000 from University of Madras. She pursued her both M.E. in power electronics and drives in 2007 and Ph.D. in electrical engineering in 2017 from College of Engineering, Guindy, Anna university, Chennai. She has experience of 21 years in teaching. She published research papers in various reputed international journals (Scopus and SCI) and conferences. Her research interests include design of controllers for DC-DC converters, renewable energy systems and smart grid. She can be contacted at email: malathis.eee@srmvalliammai.ac.in.

Ambikapathy Aladian is an associate professor and head of Department of Electrical and Electronics Engineering and head of IPR cell at Galgotias College of Engineering and Technology. She has 17 years of teaching experience. She has authored 9 engineering books; she has filed 8 patents, published 30 research papers in various reputed international journals (Scopus and SCI) and conferences. She is involved in various funded projects from government organizations such as MSME and Dr. Abdul Kalam Technical University, Lucknow. She also delivers expert lecture on various topics such as awareness on IPR, motivational way to inspire students and implementation of solar micro-plant at distribution side. She is reviewer of many reputed international journals. During her service as a head of department she made MOU with different industries and through which she has organized many events. She has also filed patent through collaborative research. Her research interests include power electronics, renewable energy, and micro grid. She can be contacted at email: ami.ise.boo@gmail.com.