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Impedance network-based ultra sparse matrix converter with enhanced voltage gain

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ABSTRACT

The matrix converter is devised to achieve sinusoidal input current and output voltage, and high power density. The typical matrix converter gives voltage gain less than unity using a significantly large number of switches. To reduce the number of switches an ultra sparse matrix converter (USMC) is introduced whose voltage gain is still less than unity. Researchers also introduced many modified versions of these matrix converters including quasi-Z-source, series Z-source, switched inductor, and switched capacitor USMCs. Although all of these matrix converters have their relative advantages and disadvantages in terms of the number of switches and passive elements, the voltage gain is still marginal. This paper focused on achieving higher voltage gain using minimal switches and passive elements. We proposed a doubler boost impedance network based ultra sparse matrix converter (DB-USMC). The doubler boost impedance network consists of a boost stage and doubler stage where the boost stage enhances the voltage and the doubler stage makes it double. The voltage gain of the proposed DB-USMC converter is 4.00 at a 50% duty cycle. The obtained results of the proposed DB-USMC converter show a path to get superior voltage gain using minimal switches and passive elements in a cost-effective manner.

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1. INTRODUCTION

High voltage gain is an essential requirement in power systems and renewable energy systems. The generated base voltages are not enough for effective power transmission due to the i^2R losses which cause low power efficiency. Currently, a step-up transformer with high voltage alternating current (HVAC) transmission solves this issue. However, the transformer is not always suitable because of its bulkier size, large space requirement, and high cost. Also, the transformer cannot vary the frequency to meet the grid requirement. Besides, high-voltage direct current (HVDC) transmission is more advantageous compared to the HVAC [1]. So if we substitute the transformer with the power converters then we get two benefits. Firstly, we can use the high direct current (DC) voltage in HVDC transmission. Secondly, make the output voltage and frequency of renewable energy systems suitable for the grid system. We can also convert the output of the renewable energy systems at a suitable voltage and frequency to direct use in industry and households with minimum cost.

The matrix converters [2], a class of power converters, have attracted much attention due to their abil-

ity to convert poly-phase alternating current (AC) to poly-phase AC at variable voltage and frequency with aiming to achieve higher voltage gain. It has sinusoidal input and output with a unity power factor, regenerative capability, and less harmonic distortion [2]-[4] that makes it suitable for various applications. Although matrix converters have many applications, the major drawback is the necessity of a large number of switches and low voltage gain [5], [6]. For example, a typical sparse matrix converter is designed by using fifteen or twelve switches [7], [8] with voltage gain less than unity. The ultra sparse matrix converter (USMC) is designed by modifying the sparse matrix converter to reduce the number of switches. The typical USMC requires nine switches [9], [10] which is still higher in number. On the other hand, the USMC does not have any intermediate topologies and therefore charge storage is not possible since there have no passive elements. Therefore, the voltage gain of USMC is very low which is 0.866. The USMC is currently used in renewable energy and photovoltaic (PV) applications [11], [12], wind energy integration in microgrids [13], feeding permanent magnet synchronous motors (PMSMs) in applications with field-oriented control (FOC) [14], [15] and as a power-transferring device [16]. But the low voltage gain reduces their efficiency and also limits applicability in industries. The voltage gain can be improved by using a step-up transformer, but this is costly and require more space.

To overcome the limitations of conventional sparse matrix converters researchers proposed the Z-source matrix converter by introducing the Z-source impedance network [17]. The Z-source matrix converter aims to enhance voltage gain using four passive elements (two capacitors and two inductors) [18]. The Z-source impedance network is integrated with an ultra sparse matrix converter and the resulting matrix converter is called ZS-USMC [19]. The ZS-USMC gives a voltage gain of 1.5 employing the same number of switches as USMC and four passive elements, which is still low. Besides, this converter has no common ground in the impedance network [20]. To circumvent this drawback series Z-source ultra sparse matrix converter (SZS-USMC) is introduced [21], [22]. The advantage of SZS-USMC is that it has common ground, with all elements the same as ZS-USMC, but it requires additional diode [23], and voltage gain drops to 0.5. On the other hand, the SZS-USMC produces discontinuous rectifier output current which is a serious issue that increases the ripple.

To address these limitations, a quasi-Z-source impedance network is integrated into USMC (QZ-USMC) [24], [25]. The QZ-USMC has a voltage gain of 1.5 using the same number of switches and passive elements as ZS-USMC. In QZ-USMC, common mode voltage, the same voltage present at two or more nodes of a circuit with respect to a reference point, is also increased which can increase the leakage current that may damage the insulation. Finally, although the Z-source impedance network integrated USMCs has relative advantages and disadvantages the noticeable point is that the voltage gain is still low. To overcome the limitations of the Z-source impedance network integrated USMCs and improve voltage gain, an active zero-state switched network is integrated with ZS-USMC [26]. One version of it is switched capacitor ZS-USMC (SCZ-USMC) [27], [28] that requires seven passive elements and ten switches. It has a voltage gain of 3.0, which is marginal, and a wide load range regarding power factor. The limitation of SCZ-USMC is the limited voltage conversion ratio due to using capacitors to transfer energy between different voltage levels. To transcend this barrier, switched inductor ZS-USMC (SIZ-USMC) is reported in [29], [30]. The SIZ-USMC has the same voltage gain of 3.0 using six passive elements and nine switches which are slightly lower than the SCZ-USMC. It also has higher voltage stress [31] which is the amount of voltage that is applied across the switching devices in the converter, which can cause them to break down or fail due to excessive voltage. Both SCZ-USMC and SIZ-USMC have the same voltage gain but require a large number of passive elements which is costly. To reduce the number of passive elements the switched boost USMC (SB-USMC) is introduced [32]. In SB-USMC, only two passive elements are required and it has lower inductor current stress. The required number of diodes is also reduced but the voltage gain drops to 2.0. On the other hand, it has higher voltage stress.

All existing matrix converters have their relative advantages and disadvantages but the most noticeable drawback of all matrix converters is that the voltage gain is low and marginal. Therefore, we need more voltage gain to meet the requirements of power systems and renewable energy systems. However, the question arises, how we can achieve higher voltage gain using a small number of switches and passive elements?

To answer this question, we proposed a doubler boost ultra sparse matrix converter (DB-USMC) by integrating a novel 'doubler boost impedance network' into the ultra sparse matrix converter. The proposed DB-USMC uses the doubler boost concept that comes from the voltage doubler circuit and boost converter. The doubler boost impedance network has two stages that are boost and doubler stages. We simulated the proposed DB-USMC using matlab simulink software. Finally, the results show that the proposed DB-USMC

converter has a voltage gain of 4.00 at 50% duty ratio. It also requires only three passive elements which are less than the other reported converters except for SB-USMC. The obtained results show a path to design a matrix converter to meet the requirements of power systems and renewable systems with superior voltage gain using minimal passive elements that reduce cost.

We organized the paper as follow: i) Section 2, we described the proposed DB-USMC topology with an elaborate description of the doubler boost network which is the heart of the proposed DB-USMC topology, formulation of the mathematical background, and development of the employed switching pattern; ii) Section 3, we included the methodology of how the proposed DB-USMC topology has been tested and validated with a summary of the used value of all parameters; iii) Section 4, we summarized the findings, with the aim of meeting the demand for high voltage gain, including a comparative analysis; and iv) Section 5, we concluded with the future directions.

2. PROPOSED TOPOLOGY

The proposed DB-USMC topology, as shown in Figure 1, is consist of three stages: the rectifier stage on the left, the doubler boost stage in the middle, and the inverter stage on the right. The main function of the rectifier stage is to convert AC-DC. Three-phase AC-DC rectifier act as a boost rectifier where output rectified voltage is 1.5 times the input AC voltage [33]. This stage consists of three unidirectional switches that are S_X, S_Y, and S_Z, and twelve power diodes that are connected to the 3-phase supply. Three phase supply sources are connected in X, Y, and Z points where each line contains an inductor and a capacitor that constitute a filter. The output of the rectifier stage is DC denoted by V_{ro} that is directly coupled to the doubler boost stage. The main function of the doubler booster stage is to boost the input DC that is shown separately in Figure 2. The doubler booster stage is divided into two substages; booster stage and doubler stage. The booster stage consist of an inductor denoted by L and a switch denoted by S. On the other hand, the doubler stage consist of two capacitors denoted by C where both capacitors have the same value and two diodes denoted by D_1 and D_2.

The output of the doubler boost stage is also DC, denoted by V_{db} in Figure 1, which is directly connected to the input of the inverter stage, and the main function of this stage is to convert input DC into AC. The inverter stage consists of six switches that are denoted by S_{AX}, S_{AY}, S_{BX}, S_{BY}, S_{CX}, and S_{CY}. The outputs are taken as u_A, u_B, and u_C.

We evaluated the performance of the proposed DB-USMC topology, as described above, using matlab simulink software. Three important steps in evaluating the performance of the proposed DB-USMC topology are understanding the operation of the doubler booster impedance network, determining the appropriate switching strategy, and calculating the proper value of passive elements. We described all three steps in 2.1.

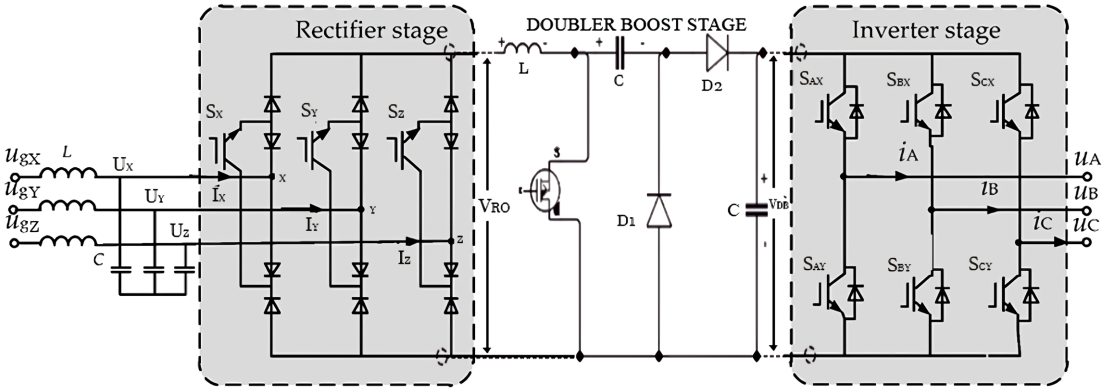

Figure 1. Proposed DB-USMC topology

2.1. Doubler boost impedance network

Doubler boost (DB) converter is a step-up converter and dynamic behavior of DB converter is similar to the boost converter that is addressed in [34]. The complete operation of the doubler boost converter can be described in two modes. The first is the shoot-through mode, and the second is the non-shoot-through mode.

For each cycle of pulses, it is high for a certain period of time and low for the remaining time. The converter run in shoot-through mode when the pulse is high and runs in non-shoot-through mode when the pulse is low. In the shoot-through state, switch S is ON, and diodes D_1 and D_2 are OFF which can visualized in Figures 1 and 2. The switch and diodes both can not be ON in together. So in this mode boost stage is ON and the doubler stage is OFF in Figure 2. Let apply KVL to the boost stage circuit, as in (1).

$$V_{ro} - V_L = 0 \tag{1}$$

In the non-shoot-through mode, switch S is OFF and diodes D_1 and D_2 are ON, as can be visualized in Figures 1 and 2. In this mode boost stage is OFF and the doubler stage is ON therefore current flows through the doubler circuit. The operation of the voltage doubler circuit is described in [35]. Let apply KVL in the doubler circuit, as in (2).

$$V_{ro} - V_L - V_{ro1} = 0 \tag{2}$$

V_{ro1} is the voltage that acts as the input voltage of the doubler circuit as shown in Figure 2, as in (3)-(6).

$$V_{ro} - V_L - \frac{V_{DB}}{2} = 0 \tag{3}$$

$$V_{ro1} = \frac{V_{DB}}{2} \tag{4}$$

$$V_L = V_{ro} - \frac{V_{DB}}{2} \tag{5}$$

$$\int_0^T V_L = 0 \tag{6}$$

By solving this equation, as in (7).

$$V_{DB} = \frac{2V_{ro}}{1-D} \tag{7}$$

The output voltage of the doubler boost represent in (7). It is also clear that the doubler boost impedance network boost the voltage level from V_{ro} to $2V_{ro}/(1-D)$. Now, the maximum phase output voltage of the rectifier stage is given by (8).

$$V_{abc} = \frac{m_f}{\sqrt{3}} V_{DB} \tag{8}$$

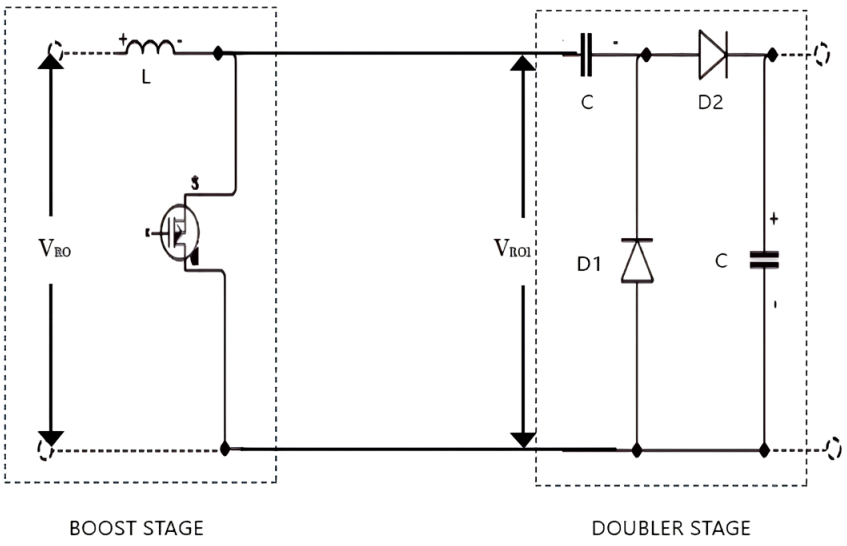

Figure 2. The doubler boost stage of the proposed DB-USMC topology

The final AC output voltage represent in (8). The overall gain of the proposed converter including the power factor is as in (9).

$$\frac{V_{abc}}{V_{xyz}} = \frac{\sqrt{3}m_f}{2} \times \frac{2}{1-D}\cos(\alpha) \tag{9}$$

Where α is the angle between voltage and current. Boosting factor (BF) of DB-USMC is represented by (10) and (11).

$$BF = \frac{\sqrt{3}m_f}{2} \times \frac{2}{1-D} = \frac{\sqrt{3}m_f}{1-D} \tag{10}$$

$$D = \frac{BF - \sqrt{3}m_f}{BF} \tag{11}$$

The (11), that represents the required duty ratio to obtain the desired voltage gain in terms of the boosting factor.

2.2. Switching strategy

The optimization of converter efficiency depends on the switching technique [36]. We use state vector pulse width modulation (SVPWM) [37] for generating the control signal to control the output current of the rectifier stage and the voltage of the inverter stage. The pulse width modulation signal is generated by comparing the reference voltage with a carrier signal, which has a fixed frequency and amplitude. In SVPWM, firstly each reference vector, such as I_X, I_Y, and I_Z, is converted into a set of three vectors, which is then used to generate a pulse width modulation (PWM) signal for each phase. In SVPWM, the duty cycle of the PWM signal is adjusted based on the position of the reference vector in the space vector diagram. In the rectifier stage, there have three reference vectors, I_X, I_Y, and I_Z, and corresponding nine vectors. Among nine vectors six are active vectors that are I_{xy}, I_{yz}, I_{zx}, I_{yx}, I_{zy}, and I_{xz} and three are zero vectors that are I_{xx}, I_{yy}, and I_{zz} where I_{xy}, I_{yz}, I_{zx}, I_{yx}, I_{zy}, and I_{xz} are the line current between the two corresponding lines and I_{xx}, I_{yy}, and I_{zz} are the line current of x, y, and z line, respectively. Similarly, in the inverter stage, there are six active vectors that are V_{001}, V_{010}, V_{011}, V_{100}, V_{101}, V_{110}, and two zero vectors that are V_{000} and V_{111} where V_{001} (001 is the binary number) means the voltage when S_X, S_y are OFF and S_z is ON and similarly switches are ON and OFF based on other vectors. On the other hand, two zero vectors V_{000} and V_{111} indicate the voltage when all switches are either ON or OFF. To implement SVPWM in the rectifier stage, reference input current I_{rf} is synthesized by two active vectors. Similar things will happen for the inverter stage. The reference voltage is synthesized by a combination of active and zero vectors.

In the DB-USMC control strategy, the duty ratio of SVPWM is continuously varying and also there have different duty ratios for the rectifier and inverter stages. The duty ratio DI_{xy} and DV_{001} for the rectifier and inverter stages, respectively, are defined by (12)-(14).

$$DI_{xy} = \frac{\sin(\frac{\pi}{3} - \gamma)}{\cos(\gamma)} \tag{12}$$

$$DV_{001} = m_f \sin(\frac{\pi}{3} - \partial) \tag{13}$$

$$DV_{001} = m_f \sin(\partial) \tag{14}$$

Here γ is the sector angle of the rectifier stage and ∂ is the vector angle of output voltage in the inverter stage. Similarly, we can define duty ratio for all other active vectors such as DI_{XZ} and DV_{010}. The overall duty ratio is defined as the multiplication of corresponding duty ratios in rectifier and inverter stages such as DI_{xy} and DV_{001}. All overall duty ratios for DB-USMC are given in (15)-(19).

$$D_a = DI_{xy} \times DV_{001} \tag{15}$$

$$D_b = DI_{xy} \times DV_{010} \tag{16}$$

$$D_c = DI_{xz} \times DV_{010} \tag{17}$$

$$D_d = DI_{xz} \times DV_{001} \tag{18}$$

$$D_0 = 1 - D_a - D_b - D_c - D_d - D \tag{19}$$

Here D is the duty ratio in the shoot mode for the doubler boost impedance network where shoot mode is one of two modes of operation that is described in 2.1. In the rectifier stage, the average output voltage is $1.5 \times V_{xyz}$ where V_{xyz} is the input phase voltage.

Finally, based on the above-mentioned duty ratios we defined the switching pattern. We have shown the switching pattern for the proposed DB-USMC in Table 1. The switching strategy of DB-USMC is designed to reduce switching losses. For I_{xy}, vectors of inverter stage V_{000}, V_{001}, and V_{010} are ON and the duty ratio at that time will be D_0/6, D_a/3, and D_b/1.5 to make sure that all vector of inverter stage are not ON all together. Similarly, For I_{xz} vector of the inverter stage V_{010}, V_{001}, V_{000}, V_{000}, V_{001}, and V_{010} are ON and the duty ratio at that time will be D_c/1.5 D_d/3, D_0/6, D_0/6, D_d/3, D_c/1.5. Again for I_{xy}, vectors of inverter stage V_{010}, V_{001}, and V_{000} are ON and the duty ratio at that time will be D_b/1.5, D_a/3, and D_0/6.

Table 1. The switching pattern for evaluating the proposed DB-USMC topology

Non shoot through		Shoot through	
V_{000}	$D_0/6$	V_{000}	$D_0/6$
V_{001}	$Da/3$	V_{001}	$D_d/3$
V_{010}	$D_b/1.5$	V_{010}	$D_c/1.5$
V_{010}	$D_c/1.5$	V_{010}	$D_b/1.5$
V_{001}	$D_d/3$	V_{001}	$D_a/3$
V_{000}	$D_0/6$	V_{000}	$D_0/6$

2.3. Passive elements

We calculate the value of passive components based on the ripple current across the inductor and the ripple voltage across the capacitor using the CCM mode. CCM is a continuous-current mode technique that is addressed [38]. We calculate the value of passive components based on the ripple current across the inductor and the ripple voltage across the capacitor, as in (20).

$$V_{ro} = V_L = L\frac{di}{dt} = L\frac{\Delta I_L}{\Delta t} \tag{20}$$

Now $\Delta t = DT$ where $T = 1/f$ is the time period, as in (21).

$$\Delta I_L = \frac{DTV_{ro}}{L} \tag{21}$$

From (7), we get (22).

$$\Delta I_L = \frac{D(1-D)V_{DB}}{2Lf} \tag{22}$$

According to the continuous conduction mode, we get (23) and (24).

$$I_L - \frac{1}{2}\Delta I_L = 0 \tag{23}$$

$$I_L = \frac{D(1-D)V_{DB}}{4Lf} \tag{24}$$

Now $P_0 = V_{DB}I_L$, as in (25) and (26).

$$L = \frac{D(1-D){V_{DB}}^2}{4fP_0} \tag{25}$$

$$L = \frac{D(1-D)V_{DB}^2\cos\alpha}{4f\%nP_o} \tag{26}$$

See (26), this gives the required value of L for $\%n$ ripple. On the other hand for capacitor, as in (27)-(31).

$$I_C = C\frac{\mathrm{d}V_c}{\mathrm{d}t} = C\frac{\Delta V_{DB}}{\Delta t} \tag{27}$$

$$C = \frac{\Delta t I_C}{\Delta V_{DB}} \tag{28}$$

$$C = \frac{DTI_C}{\Delta V_{DB}} \tag{29}$$

$$C = \frac{DTI_C \Delta V_{DB}}{\Delta V_{DB}^2} \tag{30}$$

$$C = \frac{DTP_0}{\Delta V_{DB}^2} \tag{31}$$

As V_C = V_{DB}, we found (32).

$$C = \frac{DTP_o}{\Delta V_{DB}^2 (1-D)\%z \cos\alpha} \tag{32}$$

See (32), that gives the required value of C for $\%z$ ripple.

3. METHODOLOGY

We tested and validated the proposed DB-USMC topology, as described in section 2, using MATLAB/simulink R2018a software as the literature suggested [32], [35]. At first, we designed and constructed the proposed DB-USMC topology in the MATLAB/Simulink software based on the diagram shown in Figure 1. After that, we assigned the value of all elements as indicated on the diagram from Table 2. In constructing Table 2, we calculated the value of two important passive elements, the inductor, and capacitor, as $L = 0.2198$µH and $C = 25$µF using (26) and (32), respectively, with taking 1.5625% and 0.3185% ripple factor, respectively. The value of all other elements is selected by reviewing existing literature [19], [24], [25], [27], [31]. In selecting the input AC supply we tried to keep it close to the North American power supply as shown in Figure 3 with a peak value of 100 V and root mean square (RMS) value of 70.7 V. We selected the duty ratio and switching frequency as 0.5 and 40 KHz, respectively based on the existing literature [39], [40]. Finally, we set the switching pattern based on Table 2 and simulate the proposed DB-USMC topology.

Table 2. The used value of parameters for three different stages of the proposed DB-USMC topology

Rectifier stage		Doubler boost stage		Inverter stage	
Parameter	Value	Parameter	Value	Parameter	Value
Switch rating	3000 V, 1000 A	Switch rating	3300 V, 1200 A	Switch rating	3000 V, 1000 A
Diode rating	1200 V, 30 A	Diode rating	1200 V, 30 A	Diode rating	1200 V, 30 A
Input filter (L_{in})	1 mH	Inductor	0.2198 µH	Output filter (L_{out})	1mH
Input filter (C_{in})	10 µF	Capacitor	25 µF	Output filter (C_{out})	1 µF

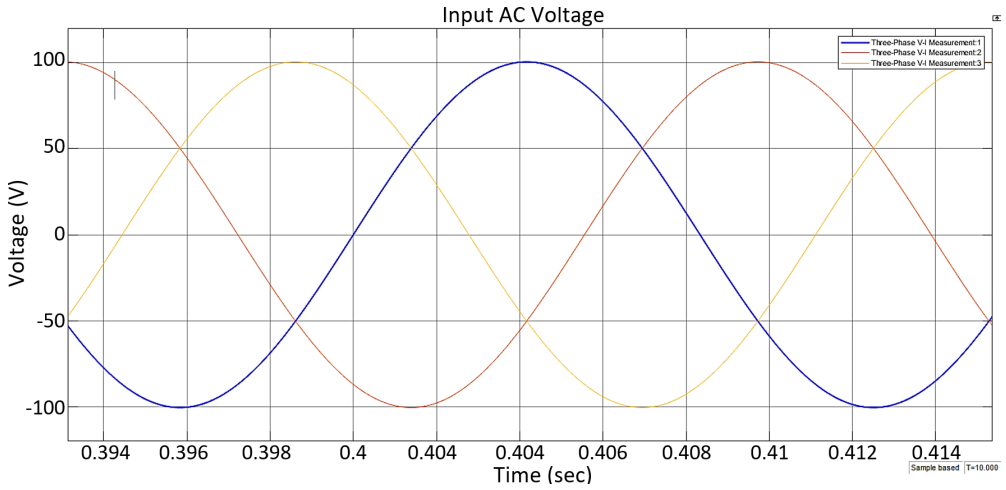

Figure 3. Input waveform to the rectifier stage of the proposed DB-USMC topology

4. RESULTS AND DISCUSSION

We evaluated the performance of the proposed DB-USMC topology in terms of voltage gain and the required elements to implement it. We obtained an end to end voltage gain of 4.00 with a minimal number of elements required to implement the proposed DB-USMC topology. The obtained high voltage gain takes us one step forward to answer the question of how we can achieve higher voltage gain to meet the requirements of power systems and renewable energy systems. Besides, the minimal number of elements required to implement the proposed DB-USMC topology enables to distribution of the solution at a reasonable cost. The 4.1 represents the output obtained at each stage of the proposed DB-USMC topology with an ultimate aim of high voltage gain and 4.2 represents a comparison of obtained results with the existing solutions for minimizing the cost.

4.1. Results

The output of the rectifier stage is 176V DC voltage (rectified) as shown in Figure 4 whereas the input AC supply to this stage, as well as for the proposed DB-USMC topology, has a peak value of 100V and an RMS value of 70.7V as shown in Figure 3. The rectified output voltage is slightly different from the theoretical value which is theoretically demonstrated as 150V in Section 2 This difference is due to the use of the filter circuits which also act as the storage elements. Therefore, a voltage gain of 2.49 with respect to the RMS value of the input AC supply is obtained in this stage. This voltage drives the doubler booster circuit.

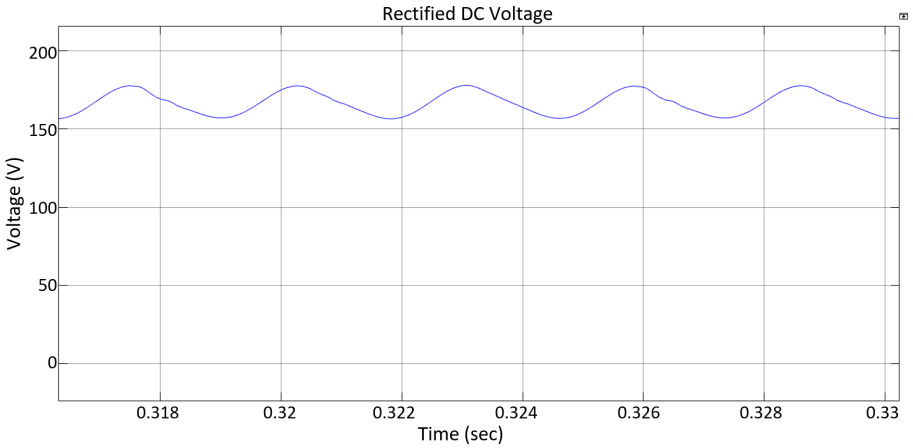

Figure 4. Output waveform of the rectifier stage

The rectified 176V DC acts as the input voltage to the doubler boost stage. The duty ratio of the doubler boost circuit is 0.5. In shoot-through mode, the switch acts as a short circuit, so the doubler circuit

is OFF and no voltage is produced in this mode. The current across the inductor is shown in Figure 5. In the non-shoot-through mode, the doubler stage is ON, and voltage stress across diodes (D_1 and D_2) is shown in Figure 6. In this mode, we get a maximum voltage that is 680V-690V, which is shown in Figure 7. So in the doubler boost stage, we get the voltage that is 4 times the input to this stage. So a high voltage gain of 3.92 with respect to the input to this stage and 9.76 with respect to the RMS value of the input AC supply is obtained in the doubler boost stage.

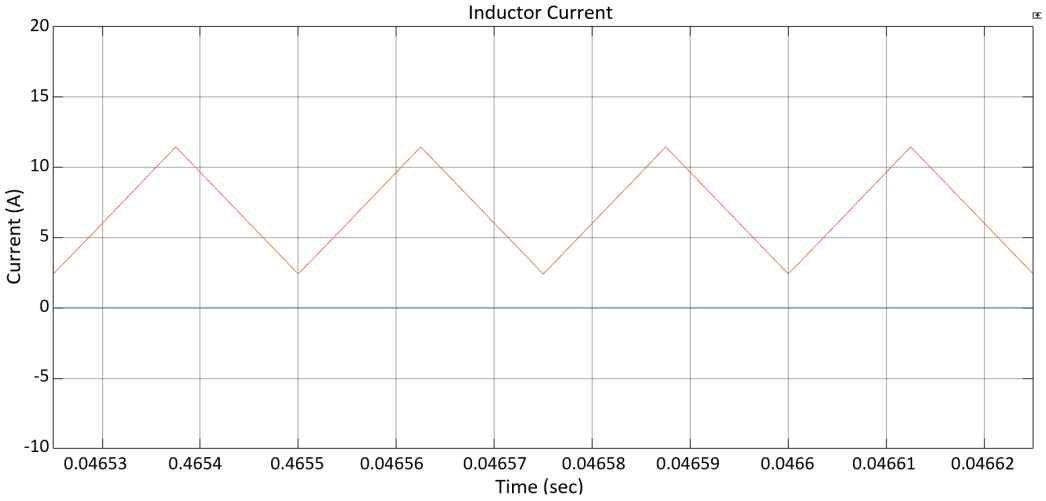

Figure 5. Waveform of the current across the inductor

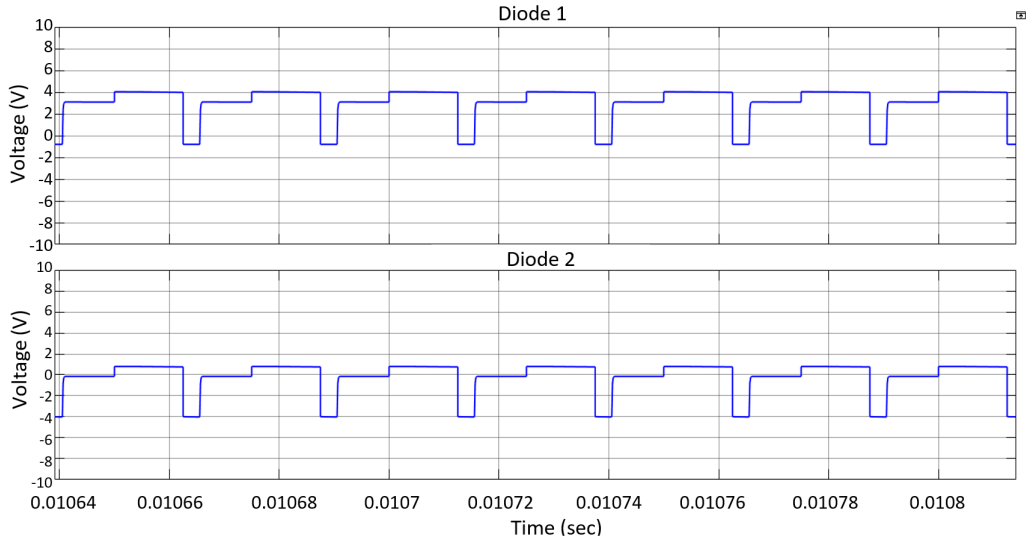

Figure 6. Waveform of the voltage across diodes (D_1 and D_2)

The boosted DC voltage acts as the input of the inverter stage. In the inverter stage, we get the output AC voltage with a peak value of 400V, which is shown in Figure 8. So the voltage at the output stage is 4 times the input AC supply. Therefore a high voltage gain of 4.00 with respect to the input AC supply and 0.41 with respect to the input to this stage is obtained.

The obtained results at different stages are summarized in Table 3. The obtained high gain at different stages meets the various requirements of the power systems and renewable energy systems. The doubler boost stage is the main stage to achieve this high voltage gain. By increasing the modulation index or duty cycle, higher voltage can be achieved where the limit is $M_f + D \leqslant 1$.

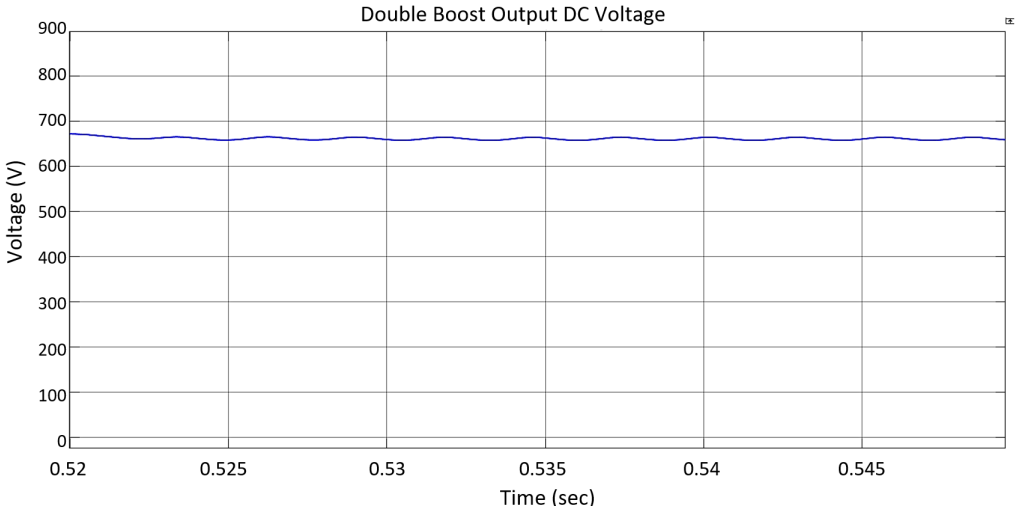

Figure 7. Output waveform of the doubler boost stage

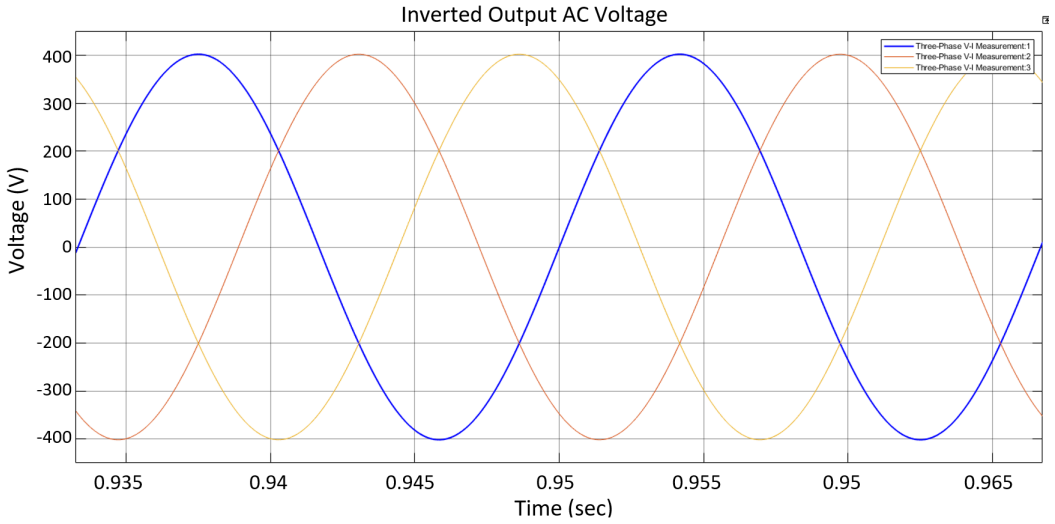

Figure 8. Output waveform of the inverter stage of the proposed DB-USMC topology

Table 3. Voltage gain of the proposed DB-USMC topology

Stage of the proposed DB-USMC topology	Output	Reference voltage	Obtained voltage gain	Applications
Rectifier stage	176 V	Input AC supply (100 V peak and 70.7 V RMS)	2.49	Boosted rectifier
Doubler boost stage	690 V	Input AC supply	9.76	HVDC transmission
		Input to this stage	3.92	Boosting DC
Inverter stage	400 V(peak) 283 V (RMS)	Input AC supply	4.00	HVAC transmission Direct industrial usages
		Input to this stage	0.41	–

4.2. Comparative analysis

We conducted a comparative analysis among the proposed DB-USMC and existing converters such as ZS-USMC, SZS-USMC, QZ-USMC, SIZ-USMC, and SB-USMC. We compared the proposed DB-USMC converter against existing converters considering parameters that are inductor current, capacitor voltage, the required number of passive elements, and the required number of diodes. The comparative analyses are summarized in Table 4.

The analysis shows that the required number of passive elements of the proposed DB-USMC is less than that of the ZS-USMC, SZS-USMC, QZ-USMC, SCZ-USMC, and SIZ-USMC. The required number of diodes is less than SIZ-USMC and SCZ-USMC but slightly greater than ZS-USMC, SZS-USMC, and QZ-USMC. The voltage gain is higher compared to all matrix converters. At duty cycle of 0.5, the proposed DB-USMC topology shows the voltage gain is 4.00, which is better than all other converters.

The proposed DB-USMC has a lower capacitor voltage rating than the SIZ-USMC. In DB-USMC, one extra switch is needed, and the voltage rating of this switch is the same as the voltage rating of the capacitor and the current rating of the inductor. Therefore, the proposed DB-USMC topology is able to meet the requirements of high voltage gain of power systems and renewable systems with minimal cost.

Table 4. Comparative analysis of different types of USMC. Here #PE, #D, #S and V_g represent the number of passive elements, number of diode, number of switches used and voltage gain for 50% duty cycle, respectively

Converter	Inductor current	Capacitor voltage	#PE	#D	#S	V_g
USMC	–	–	-	12	9	0.86
ZS-USMC	$I_L = \frac{\sqrt{3}M_f(1-D)I_{out}}{2(1-2D)}$	$V_{C1} = V_{C2} = \frac{(1-D)V_{ro}}{1-2D}$	4	13	9	1.5
SZS-USMC	$I_L = \frac{\sqrt{3}M_f(1-D)I_{out}}{2(1-2D)}$	$V_{C1} = V_{C2} = \frac{DV_{ro}}{1-2D}$	4	13	9	0.5
QZ-USMC	$I_L = \frac{\sqrt{3}M_f(1-D)I_{out}}{2(1-2D)}$	$V_{C1} = \frac{(1-D)V_{ro}}{1-2D}$ $V_{C2} = \frac{DV_{ro}}{1-2D}$	4	13	9	1.5
SCZ-USMC	$I_{L1} = I_{L2} = \frac{\sqrt{3}M_f I_{out}}{1-2D}$	$V_{C1} = V_{C2} = \frac{(1-D)V_{ro}}{3-2D}$	7	16	10	3.0
SIZ-USMC	$I_L = \frac{\sqrt{3}M_f(1-D)I_{out}}{2(1-3D)}$	$V_{C1} = V_{C2} = \frac{(1-D)V_{ro}}{1-3D}$	6	18	9	3.0
SB-USMC	$I_L = \frac{\sqrt{3}M_f(1-D)I_{out}}{2(1-2D)}$	$V_{C1} = V_{C2} = \frac{V_{ro}}{1-2D}$	2	14	10	2.0
DB-USMC	$I_L = \frac{2\sqrt{3}M_f I_{out}}{(1-D)}$	$V_{C1} = V_{C2} = \frac{2V_{RO}}{(1-D)}$	3	14	10	4.0

5. CONCLUSION

The matrix converters play an important role in different applications related to power where optimal voltage gain is a major concern. This paper introduces a novel approach, by proposing a USMC with integrated DB impedance network consisting of doubler and boost circuits. The proposed DB-USMC has three stages that are rectifier stage, doubler boost stage, and inverter stage. We simulated the proposed DB-USMC topology using matlab simulink R2018a software. The results show an end to end voltage gain of 4.00 which is an excellent enhancement in voltage gain. The obtained results indicate that the voltage gain of the proposed DB-USMC is higher than that of existing USMCs. The higher voltage gain is obtained by integrating the doubler boost impedance network. Moreover, the proposed DB-USMC brings out a reduction in the number and value of required passive elements, leading to cost minimization.

After all, there is a huge drop in voltage gain in the inverter stage. If we can achieve a good voltage gain or can maintain the same one in this stage then it is possible to obtain a very high the end to end voltage gain. This makes a future direction. Besides, although, the proposed DB-USMC has better capacitive voltage stress but, the inductive current stress is higher and can be improved in the future.

REFERENCES

[1] C. J. Chou, Y. K. Wu, G. Y. Han, and C. Y. Lee, "Comparative evaluation of the HVDC and HVAC links integrated in a large offshore wind farm-an actual case study in Taiwan," *IEEE Transactions on Industry Applications*, vol. 48, no. 5, pp. 1639-1648, Sept.-Oct. 2012, doi: 10.1109/TIA.2012.2209622.

[2] P. W. Wheeler, J. Rodriguez, J. C. Clare, L. Empringham, and A. Weinstein, "Matrix converters: a technology review," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 2, pp. 276-288, April 2002, doi: 10.1109/41.993260.

[3] L. Empringham, J. W. Kolar, J. Rodriguez, P. W. Wheeler, and J. C. Clare, "Technological issues and industrial application of matrix converters: A review," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 10, pp. 4260-4271, Oct. 2013, doi: 10.1109/TIE.2012.2216231.

[4] L. Huber and D. Borojevic, "Space vector modulated three-phase to three-phase matrix converter with input power factor correction," *IEEE Transactions on Industry Applications*, vol. 31, no. 6, pp. 1234-1246, Nov.-Dec. 1995, doi: 10.1109/28.475693.

[5] L. Wei, T. A. Lipo, and H. Chan, "Matrix converter topologies with reduced number of switches," *33rd Annual IEEE Power Electronics Specialists Conference Proceedings (Cat. No.02CH37289)*, Cairns, QLD, Australia, vol. 1, pp. 57-63, 2002, doi: 10.1109/PSEC.2002.1023847.
[6] O. Simon, J. Mahlein, M. N. Muenzer, and M. Bruckmarm, "Modern solutions for industrial matrix-converter applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 2, pp. 401-406, April 2002, doi: 10.1109/41.993273.
[7] J. W. Kolar, F. Schafmeister, S. D. Round, and H. Ertl, "Novel three-phase AC–AC sparse matrix converters," *IEEE Transactions on Power Electronics*, vol. 22, no. 5, pp. 1649-1661, Sept. 2007, doi: 10.1109/TPEL.2007.904178.
[8] J. W. Kolar, M. Baumann, F. Schafmeister, and H. Ertl, "Novel three-phase AC-DC-AC sparse matrix converter," *Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.02CH37335)*, Dallas, TX, USA, vol. 2, pp. 777-791, 2002, doi: 10.1109/APEC.2002.989333.
[9] S. Li, W. Chen, Y. Yan, T. Shi, and C. Xia, "A multimode space vector over modulation strategy for ultrasparse matrix converter with improved fundamental voltage transfer ratio," *IEEE Transactions on Power Electronics*, vol. 33, no. 8, pp. 6782-6793, Aug. 2018, doi: 10.1109/TPEL.2017.2752748.
[10] E. Lee, K. B. Lee, J. S. Lim, Y. Lee, and J. H. Song, "Predictive current control for a sparse matrix converter," *Proceedings of The 7th International Power Electronics and Motion Control Conference*, Harbin, China, pp. 36-40, 2012, doi: 10.1109/IPEMC.2012.6258840.
[11] P. Magesh and G. P. Ramesh, "Fuzzy logic control implementation of ultra sparse matrix converter for renewable energy applications," *2017 International Conference on Information Communication and Embedded Systems (ICICES)*, Chennai, India, pp. 1-3, 2017, doi: 10.1109/ICICES.2017.8070782.
[12] B. Ismail, B. Mohammed, O. Abdelkhalek, and S. Elhadj, "An experimental study of PV/T system using parabolic reflectors and heat exchanger," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 24, no. 3, pp. 1297-1306, Dec 2021, doi: 10.11591/ijeecs.v24.i3.pp1297-1306.
[13] O. Kuseso, T. Shishaye, W. Xiaohua, and H. Ali, "Unidirectional step-up ultra sparse matrix converter for integration of wind energy resources to microgrids," *AFRICON 2015*, Addis Ababa, Ethiopia, pp. 1-5, 2015, doi: 10.1109/AFRCON.2015.7331872.
[14] M. Bouazdia, M. Bouhamida, R. Taleb, and M. Denai, "Performance comparison of field oriented control based permanent magnet synchronous motor fed by matrix converter using pi and ip speed controllers," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 19, no. 3, pp. 1156–1168, 2020, doi: 10.11591/ijeecs.v19.i3.pp1156-1168.
[15] R. Majdoubi, L. Masmoudi, M. Bakhti, A. Elharif, and B. Jabri, "Parameters estimation of bldc motor based on physical approach and weighted recursive least square algorithm," *International Journal of Electrical and Computer Engineering*, vol. 11, no. 1, pp. 133–145, 2021, doi: 10.11591/ijece.v11i1.pp133-145.
[16] A. Dinakaran, J. Lydia, S. L. S. Vimalraj, B. B. Srinivas, M. Govarthanan, and C. D. R. Antony, "A high efficiency Z source sparse matrix converter for vehicle to home and grid to vehicle application," *2020 7th International Conference on Smart Structures and Systems (ICSSS)*, Chennai, India, pp. 1-4, 2020, doi: 10.1109/ICSSS49621.2020.9201977.
[17] O. Ellabban, H. Abu-Rub, and S. Bayhan, "Z-Source matrix converter: An overview," *IEEE Transactions on Power Electronics*, vol. 31, no. 11, pp. 7436-7450, Nov. 2016, doi: 10.1109/TPEL.2015.2471799.
[18] B. Ge, Q. Lei, W. Qian, and F. Z. Peng, "A family of Z-source matrix converters," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 1, pp. 35-46, Jan. 2012, doi: 10.1109/TIE.2011.2160512.
[19] A. M. Bozorgi, M. Farasat, and E. Karaman, "Novel modulation schemes and switching pattern for Z-source ultra-sparse matrix converter," *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, USA, pp. 4223-4229, 2017, doi: 10.1109/ECCE.2017.8096731.
[20] K. Park and K. B. Lee, "A novel sparse matrix converter with a Z-source network," *2009 35th Annual Conference of IEEE Industrial Electronics*, Porto, Portugal, pp. 4487-4492, 2009, doi: 10.1109/IECON.2009.5414882.
[21] E. Karaman, M. Farasat, and A. M. Trzynadlowski, "Matrix converter with a series Z-source," *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, Montreal, QC, Canada, pp. 6093-6098, 2012, doi: 10.1109/IECON.2012.6389085.
[22] A. M. Bozorgi, A. Hakemi, M. Farasat, and M. Monfared, "Modulation techniques for common-mode voltage reduction in the Z-source ultra sparse matrix converters," *IEEE Transactions on Power Electronics*, vol. 34, no. 1, pp. 958-970, Jan. 2019, doi: 10.1109/TPEL.2018.2820659.
[23] E. Karaman, M. Farasat, and A. M. Trzynadlowski, "A comparative study of series and cascaded Z-source matrix converters," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 10, pp. 5164-5173, Oct. 2014, doi: 10.1109/TIE.2014.2301766.
[24] E. Karaman, M. Farasat, and A. M. Trzynadlowski, "A $3\Phi - 3\Phi$ quasi Z-source matrix converter for residential wind energy systems," *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, Raleigh, NC, USA, 2012, pp. 240-246, doi: 10.1109/ECCE.2012.6342817.
[25] V. Siva, A. Singh, M. Raghuram, A. Kumar, and S. K. Singh, "Enhanced voltage gain of USMC by modified quasi Z-source impedance network," *2022 IEEE Industry Applications Society Annual Meeting (IAS)*, Detroit, MI, USA, pp. 1-6, 2022, doi: 10.1109/IAS54023.2022.9940027.
[26] V. Siva, A. Singh, S. K. Singh, and M. Raghuram, "Improved common mode voltage and modulation index range in ultra sparse matrix converters by adding active zero state switch network," *2022 IEEE 2nd International Conference on Sustainable Energy and Future Electric Transportation (SeFeT)*, Hyderabad, India, pp. 1-5, 2022, doi: 10.1109/SeFeT55524.2022.9909428.
[27] M. Raghuram, A. K. Chauhan, and S. K. Singh, "Extended range of ultra sparse matrix converter using integrated switched capacitor network," *IEEE Transactions on Industry Applications*, vol. 55, no. 5, pp. 5406-5415, Sept.-Oct. 2019, doi: 10.1109/TIA.2019.2928285.
[28] M. Raghuram, A. K. Chauhan, and S. K. Singh, "Switched capacitor impedance matrix converter," *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, USA, pp. 1071-1075, 2017, doi: 10.1109/ECCE.2017.8095906.
[29] E. Karaman, M. Farasat, and A. M. Trzynadlowski, "Indirect matrix converters as generator–grid interfaces for wind energy systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 4, pp. 776-783, Dec. 2014, doi: 10.1109/JESTPE.2014.2329920.
[30] M. Israyelu and S. Sashidhar, "Hybrid switched inductor step-up ultra-sparse matrix converter for wind generator applications," *IECON 2021 – 47th Annual Conference of the IEEE Industrial Electronics Society*, Toronto, Canada, pp. 1-6, 2021, doi:

10.1109/IECON48115.2021.9589687.
[31] E. Karaman, F. Niu, and A. M. Trzynadlowski, "Three-phase switched-inductor Z-source matrix converter," *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Orlando, FL, USA, pp. 1449-1454, 2012, doi: 10.1109/APEC.2012.6166011.
[32] V. Siva, A. Singh, S. K. Singh, and M. Raghuram, "Ultra sparse matrix converter with impedance network to enhance the voltage gain," *2022 IEEE 2nd International Conference on Sustainable Energy and Future Electric Transportation (SeFeT)*, Hyderabad, India, pp. 1-5, 2022, doi: 10.1109/SeFeT55524.2022.9909480.
[33] A. R. Borges and I. Barbi, "Three-phase single stage AC-DC buck-boost converter operating in buck and boost modes," *XI Brazilian Power Electronics Conference*, Natal, Brazil, pp. 176-182, 2011, doi: 10.1109/COBEP.2011.6085185.
[34] D. D. C. V. Perez, S. C. Trujillo, and F. E. H. Velasco, "On the dynamic behavior of the current in the condenser of a boost converter controlled with zad," *Telecommunication Computing Electronics and Control (TELKOMNIKA)*, vol. 18, no. 3, pp. 1678–1687, 2020, doi: 10.12928/telkomnika.v18i3.14109.
[35] L. S. Yang, T. J. Liang, H. C. Lee, and J. F. Chen, "Novel high step-up DC–DC converter with coupled-inductor and voltage-doubler circuits," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 9, pp. 4196-4206, Sept. 2011, doi: 10.1109/TIE.2010.2098360.
[36] N. H. Do, S. M. Ho, Q. T. Le, T. Hoang, T. M. Tran, and P. Vu, "Controlling matrix converter in flywheel energy storage system using afpm by processor-in-the-loop method," *Bulletin of Electrical Engineering and Informatics*, vol. 11, no. 4, pp. 1845–1854, 2022, doi: 10.11591/eei.v11i4.3813.
[37] A. M. Bozorgi, M. Monfared, and H. R. Mashhadi, "Optimum switching pattern of matrix converter space vector modulation," *2012 2nd International eConference on Computer and Knowledge Engineering (ICCKE)*, Mashhad, Iran, pp. 89-93, 2012, doi: 10.1109/ICCKE.2012.6395358.
[38] H. C. Sartori, F. Beltrame, H. H. Figueira, J. E. Baggio, and J. R. Pinheiro, "Power density comparative analysis concerning to three transistor technologies applied to a CCM PFC BOOST converter using optimization techniques," *2013 Brazilian Power Electronics Conference*, Gramado, Brazil, pp. 1317-1323, 2013, doi: 10.1109/COBEP.2013.6785286.
[39] M. Hayati, H. Abbasi, M. K. Kazimierczuk, and H. Sekiya, "Analysis and study of the duty ratio effects on the class-EM power amplifier including MOSFET nonlinear gate-to-drain and drain-to-source capacitances," *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10550-10562, Dec. 2018, doi: 10.1109/TPEL.2018.2810218.
[40] K. Kobravi, R. Iravani, and H. A. Kojori, "A new high switching-frequency MOSFET-based current-source-converter with bidirectional power-flow capability," *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Orlando, FL, USA, pp. 1179-1186, 2012, doi: 10.1109/APEC.2012.6165968.

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