International Journal of Power Electronics and Drive Systems (IJPEDS)
Vol. 15, No. 3, September 2024, pp. 1547~1563
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v15.i3.pp1547-1563

Efficiency enhancement in a switched capacitor cell interleaved buck converter using GaN-FETs

Puneet Kaur, Payal Jaswal, Aditi Gupta
Department of Electrical and Electronics Engineering, University Institute of Engineering and Technology, Panjab University, Chandigarh, India

Article Info

Article history:

Received Oct 11, 2023
Revised Mar 14, 2024
Accepted Mar 21, 2024

Keywords:

Electric vehicles
GaN-FET technology
Higher efficiency
Interleaved DC-DC converter
Performance analysis
Switched capacitors

ABSTRACT

In this paper, a switched capacitor cell buck converter, combining two-phase interleaved operation with gallium nitride or GaN-FET technology has been presented. These technologies make it suitable for wide range of applications where efficient power conversion is essential. To validate efficacy of the proposed converter with GaN-FET, its performance is examined in relation to a similar converter that utilizes metal-oxide semiconductor field-effect transistor (MOSFET) switches. The proposed converter offers a potential advantage over the DC-DC interleaved buck converter with MOSFET switches by allowing operation at higher frequencies, resulting in a smaller inductor value. The design parameters of the inductor have also been presented. The simulation results indicate that the converter exhibits better performance than MOSFET-based converter with regards to total power losses, input and output current ripple, output voltages and subsequently achieves higher efficiency at various duty cycles and different loads. Finally, experimental verification is done to validate the simulation results.

This is an open access article under the CC BY-SA license.

Corresponding Author:

Puneet Kaur
Department of Electrical and Electronics Engineering, University Institute of Engineering and Technology
Panjab University
Chandigarh, India
Email: puneetee@pu.ac.in

1. INTRODUCTION

With advances in the field of power converters, interleaved topologies have become increasingly popular and important due to their ability to reduce input and output ripple, increasing power density, improving reliability and scalability of power converters. At the same time, switched capacitor converters can efficiently step up or step-down voltage levels. These types of interleaved converters are therefore commonly used in high-power applications like electric vehicle or EV battery chargers, renewable energy systems, voltage regulators and data centres [1]–[3]. Efforts to continuously enhance the performance of interleaved converters are going on to maximize converter efficiency through various approaches. In this paper, a switched capacitor cell based interleaved buck converter has been explored, in which conventional switches has been substituted with gallium nitride or GaN-FETs, aiming to boost efficiency.

One of the primary benefits of interleaving is that it enhances the performance of power converters in terms of efficiency. Additionally, interleaving provides improved system reliability since the converters are connected in parallel, ensuring that the system will remain operational even in the event of a failure [4]–[6]. In a conventional interleaved buck converter (IBC), there are additional components such as an inductor, a power switch, and a diode which though improves its performance but tends to make the converter bulky. Moreover, in the traditional IBC design, all the switching devices are subjected to elevated voltage levels equivalent to

input voltage. As a result, voltage ratings of these devices are raised, giving rise to corresponding increase in the voltage drop, and consequently cost of converter increases. Another limitation of conventional IBC is that it requires a constricted pulse width to produce the lowered voltage level required for low voltage applications from the high input voltage. This complicates the design of the converter and limits the flexibility of the converter.

Several modifications/configurations have been proposed in IBC to improve its performance. Techniques utilizing turn-off snubbers and active clamp circuits to effectively reduce input current ripple, output current ripple and power losses have been discussed in [7]–[10]. The concept of coupled inductor and integrated inductor has been discussed along with improvement in voltage conversion ratio in the literature [11]–[15]. Further, different topologies have been exercised to extend the range of duty cycle for DC-DC converters [16]–[18]. Optimization of buck converters for typical step-down applications has been discussed in [19]–[21]. A two-phase interleaved buck converter that incorportes switched-cell capacitor technology for duty cycles above and below 50% has been proposed in [22]. Compared to conventional IBC, lowered voltage levels can be achieved by this converter at high duty cycles. The switched-cell capacitor also reduces the stresses on switches caused by voltage and current. All these interleaved converters discussed above use metal-oxide semiconductor field-effect transistor (MOSFET) as switches with high on-state resistance and the frequency of operation is also limited up to 100 kHz owing to the higher input and output capacitances of the MOSFET [23], [24].

For the improvement in the efficiency of DC-DC converters for potential applications like EVs [25], [26], research papers with DC-DC converters using GaN-FET switches have also been discussed in the literature [27]–[31]. The GaN-based devices offer several advantages such as the higher switching frequency owing to their low input and output capacitances, the reduction in the size of passive elements, the decrease in transition time results in lower switching losses, lower on-state resistance which results in reduced conduction losses, and higher power densities. The higher power densities allow the development of more compact power devices. The GaN-based transistors also have negative temperature coefficient of resistance, and high electron mobility. In previous studies [32], [33], a comparative analysis of the buck converter employing silicon (Si) based MOSFET, silicon carbide (SiC) based MOSFET and, GaN-based MOSFET indicates lower switching losses in SiC and GaN-based FETs than Si-based FETs and even high efficiency. A DC-DC converter has been developed utilizing GaN based E-HEMT in [34], [35]. These devices have faster switching speeds and it leads to reduction in losses arising from switching actions and subsequent enhancement in conversion efficiency [36]–[38].

The objective of this research paper is to propose a two-phase e-GaN-FET based interleaved buck converter based on switched-cell capacitor, thus exploring the advantages of both interleaved and GaN-FET technologies to boost the efficiency. Interleaved buck converter has been taken due to its ability to reduce ripples, to increase power density and to enhance reliability for electrical applications assisted by batteries. Switched capacitors facilitate the process of varying the duty cycles to achieve voltage levels as per requirement. Traditionally, interleaved buck converter often faces challenges such as increased bulkiness, elevated voltage stresses, input/output current ripple and compromised efficiency. The novelty of this research paper is to propose a converter using GaN-FET switches that has overcome all these challenges. Accordingly, the proposed converter has reduced overall size, reduced voltage stresses and improved efficiency at higher frequencies. The operation of proposed converter at higher frequencies (up to 500 kHz) is investigated for various values of duty cycles above and below 50%. A smaller size of inductor (below100 μH) has been incorporated which reduces the overall size and cost of design. The evaluation of other parameters viz. switching and total losses, voltage ripple, and current ripple have also been discussed and compared.

The paper is further organized as: i) sections 2 discuss the design and principle of operation of the proposed converter. It also includes steady- state analysis of the converter; ii) Section 3 presents the results and discussion on basis of simulation and its comparison with converter based on conventional power switches; and iii) Section 4 presents experimental verification of simulation results; and v) Followed by conclusion in section 5.

2. PROPOSED CONVERTER AND METHODOLOGY

The circuit configuration of proposed converter in this paper has been shown in Figure 1. It has three high-frequency GaN-FET switches Q_1, Q_2, Q_3 with crossly placed capacitors C_1 and C_2 having parasitic resistances as r_{c1} and r_{c2} respectively for interleaved phases. The inductance L_x is connected with the input voltage source and L_1 and L_2 are the inductances in the two interleaved stages. All the inductors (L_1, L_2, and L_x) have small parasitic resistances r_{L1}, r_{L2}, and r_{Lx} respectively. The capacitor C_o with parasitic r_{co} is the filter output capacitor of the converter and V_o is the generated voltage of the proposed converter.

The gate pulses for Q_1 and Q_2 are identical, while the gate pulses of Q_3 is 180° out of phase with respect to Q_1 and Q_2. When Q_1 and Q_2 conduct the diode associated with the same phase, D_1, will not conduct whereas D_2 will conduct. Similarly, when switch Q_3 is conducting, diode D_2 will not conduct whereas diode D_1 will conduct. The two capacitors C_1 and C_2 will be charged in series when switch Q_1 and Q_2 are not conducting and they will be discharged in parallel when both these switches are conducting. The work methodology for analysis of this converter has been developed for both below and above 0.5 duty cycle and for wide range of load resistances in order to highlight the potential of the proposed converter.

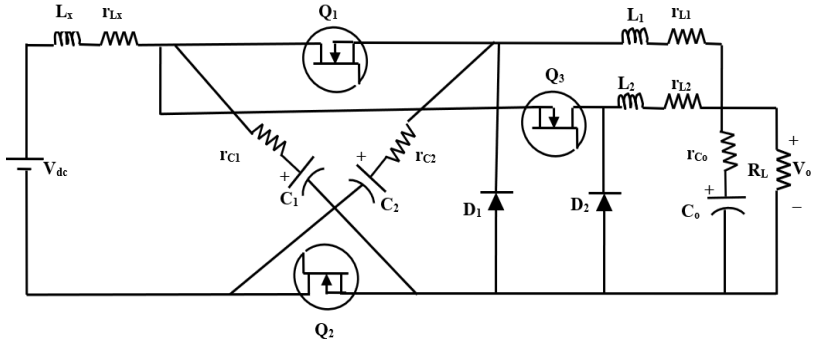

Figure 1. Proposed two-phase interleaved buck converter working on e-GaN FET

2.1. Operation of the converter with duty cycle ≤ 0.5

The switching pulses for switches Q_1, Q_2, and Q_3 for the proposed converter for duty cycle less than 0.5 have been shown in Figure 2. With $D \leq 0.5$ in continuous mode of conduction, the working of proposed converter can be divided into four modes [22]. For mode 1 (0-t_0), Figure 3 represents the circuit for this operating mode. Before this mode, none of the switches were conducting and the capacitors C_1=C_2 were getting charged through the input supply and the freewheeling diode D_1 and D_2 were conducting. During this mode, the switch Q_1 and Q_2 are conducting and the diode D_1 is reverse biased. The switch Q_3 is given complementary pulses to the Q_1 and Q_2 and it is not conducting whereas the diode D_2 is forward biased. The connection of the capacitors $C_1 = C_2$ will change from series to parallel in this mode of conduction and these capacitors will get discharged to the load. The current in the inductor L_1, L_x will increase in this mode and the inductor L_2 will discharge through the load. For mode 2 (t_0-t_1), Figure 4 shows the converter in this mode of operation. During this mode, all three switches that are Q_1, Q_2, and Q_3 are not conducting. L_1 and L_2, interleaved inductors, discharges through load whereas C_1, C_2 charges through path V_{dc}-Lx-C_1-D_1-C_2. In mode 3 (t_1-t_2), Figure 5 shows the converter in this mode of operation. During this mode of operation, switch Q_3 is conducting whereas switches Q_1 and Q_2 are given complementary pulses with respect to switch Q3. During this operating mode, input charges L_2, while L_1 discharges through load simultaneously. The two identical capacitors are still getting charged during this mode of operation. While in mode 4 (t_2-t_3), during this mode, no switch is in conduction and L_1 and L_2 discharges through load. During this mode, the converter operates similarly to that in mode 2.

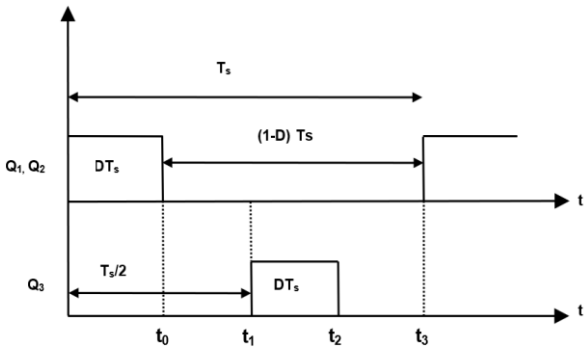

Figure 2. Proposed converter switching pulses for $D \leq 0.5$

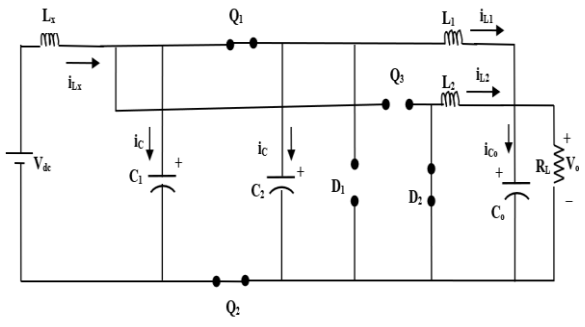

Figure 3. Operating mode 1 of proposed converter for $D \leq 0.5$

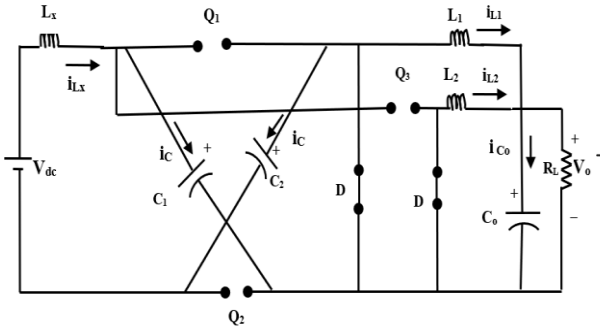

Figure 4. Operating mode 2 of proposed converter for D ≤ 0.5

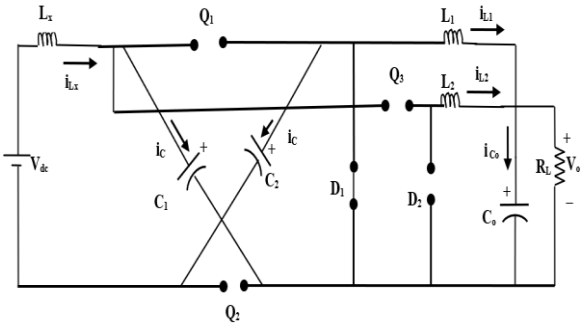

Figure 5. Operating mode 3 of proposed converter for D ≤ 0.5

2.2. Operation of the converter with duty cycle ≥ 0.5

The switching pulses for the converter for this range of duty cycle have been shown in Figure 6. With D ≥ 0.5 in continuous conduction mode, the working of proposed converter can be divided into four modes as:

- Mode I (0-t_0), during this mode, all three switches are in conduction. The current increases through L_1, L_2 and, L_x whereas, the identical capacitors are discharging in parallel. Figure 7 shows the proposed converter's operation in this mode.
- Mode II (t_1-t_2), during this mode, Q_1 and Q_2 conduct and the switch Q_3 does not conduct whereas the diode D_1 doesn't conduct and D_2 does conduct. The current through L_1 and L_x increases whereas current through L_2 decreases. The proposed converter's operation during this mode is akin to mode 2.
- Mode III (t_2-t_3), during this mode, Q_1, Q_2, and Q_3 are in conduction. The current through the L_1, L_2, and L_x is increasing in this mode of conduction whereas the identical capacitors are discharging in parallel. The proposed converter's operation is akin to mode 3.
- Mode IV (t_3-t_4), during this mode, Q_3 conducts and Q_1 and Q_2 do not conduct. The operation in this mode is akin to mode 4 of the proposed converter. D_1 and D_2, diodes, are biased in forward and reverse directions respectively.

2.3. DC analysis of proposed converter

The proposed converter is assumed to operate in steady state, assuming all the switches and diodes are ideal. Furthermore, the parasitic resistances associated with inductors as well as with capacitors are neglected. The two capacitors, C_1 and C_2, are considered to be identical that is they have same capacitance value C. The inductors connected on the load side are also considered to be identical. Additionally, the output capacitor C_o is presumed to be large enough capacitance to maintain the output voltage constant.

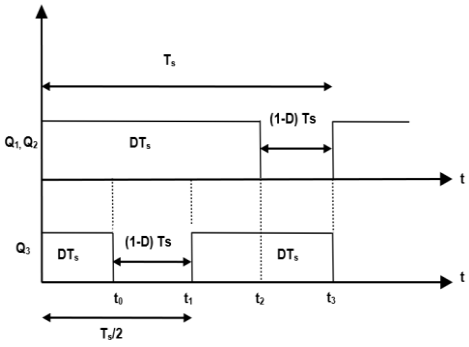

Figure 6. Proposed converter switching pulses for D ≥ 0.5

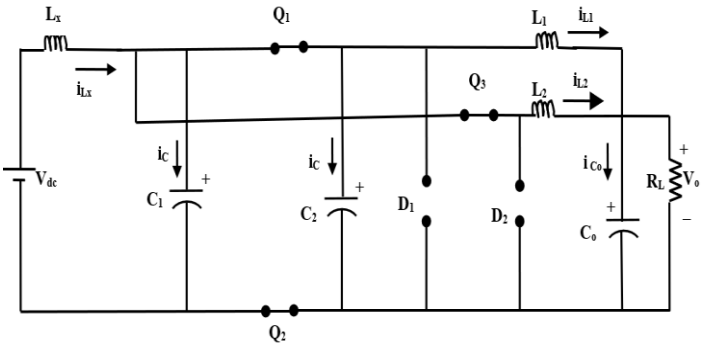

Figure 7. Operating mode I of proposed converter for D ≥ 0.5

2.3.1. Analysis of the converter with D ≤ 0.5

There are two identical capacitors C_1 and C_2,which will charge and discharge depending upon the sequence of turning on and turning off the switches Q_1, Q_2, and Q_3.The voltages of the identical capacitors are assumed to be same that is $V_{c1}=V_{c2}=V_c$. By using the volt-sec principle,(1)-(3) can be written for L_1, L_2, and L_x in mode 1 [22]:

$$V_{L_X} = V_{dc} - V_c \quad (1)$$

$$V_{L_X} = V_{dc} - V_c \quad (2)$$

$$V_{L_2} = -V_o \quad (3)$$

The voltage across the load can be written as (4):

$$V_o = V_{C_o} \quad (4)$$

By using the volt-sec principle (5)-(7) can be written for L_1, L_2, and L_x in mode 2:

$$V_{L_1} = -V_o \quad (5)$$

$$V_{L_2} = -V_o \quad (6)$$

$$V_{L_X} = V_{dc} - 2V_c \quad (7)$$

The voltage across the load can be written as (8):

$$V_o = V_{C_o} \quad (8)$$

Similarly, by using the volt-sec principle the (9)-(11) can be written for L_1, L_2, and L_x in mode 3:

$$V_{L_1} = -V_o \quad (9)$$

$$V_{L_2} = V_c - V_o \quad (10)$$

$$V_{L_X} = V_{dc} - 2V_c \quad (11)$$

The voltage across the load can be written as (12):

$$V_o = V_{C_o} \quad (12)$$

For mode 4, the voltage in (5)-(8) are used.

2.3.2. Analysis of the converter with D ≥ 0.5

There are two identical capacitors C_1 and C_2,which will charge and discharge depending upon the sequence of turning on and turning off the switches Q_1, Q_2 and Q_3.The voltages of the identical capacitors are assumed to be the same that is $V_{c1}=V_{c2}=V_c$. By using the volt-sec principle, the (13)-(15) can be written for L_1, L_2, and L_x in mode I [22]:

$$V_{L_X} = V_{dc} - V_c \quad (13)$$

$$V_{L_1} = V_c - V_o \quad (14)$$

$$V_{L_2} = -V_o \quad (15)$$

The voltage across the load can be written as (16):

$$V_o = V_{C_o} \quad (16)$$

By using the volt-sec principle (17)-(19) can be written for L_1, L_2, and L_x in mode II.

$$V_{L_X} = V_{dc} - V_c \quad (17)$$

$$V_{L_1} = V_c - V_o \quad (18)$$

$$V_{L_2} = -V_o \quad (19)$$

The voltage across the load can be written as (20):

$$V_o = V_{C_o} \quad (20)$$

The voltage equations of the mode III are akin to that of mode I and the voltage equations of the mode IV are akin to the mode 3 for D ≤ 0.5.

2.4. DC conversion ratio of voltage

The expression for the voltage conversion ratio provides valuable insights into the efficiency of the proposed converter. Utilizing appropriate equations, the voltage conversion ratio has been derived, taking into consideration duty cycles both above and below 0.5. This comprehensive approach ensures a thorough assessment of the converter's performance across various operational scenarios.

2.4.1. The voltage conversion ratio for duty cycle D ≤ 0.5

During the stable state, the average value of voltage is zero across inductor, which can be expressed utilizing volt-sec principle. For getting expression of Lx ,(21) is written using voltage-second balance as in [39]:

$$(V_{dc} - V_c)DT_s + (V_{dc} - 2V_c)(0.5 - D)T_s + (V_{dc} - 2V_c)DT_s + (V_{dc} - 2V_c)(0.5 - D)T_s = 0 \quad (21)$$

The expression for V_{dc} obtained from (21) is written as (22).

$$V_{dc} = V_c(2 - D) \quad (22)$$

Similarly, the expression obtained for the inductor L_1 by using the voltage second balance is given in (23).

$$(V_c - V_o)DT_s - V_o(0.5 - D)T_s - V_oDT_s + V_o(0.5 - D)T_s = 0 \quad (23)$$

The expression for V_o obtained from equation (23) is written as (24).

$$V_o = V_c * D \quad (24)$$

The (22) also provides the expression for V_c which can be substituted in (24) to obtain the ratio of voltage conversion, H, of the proposed converter. The expression for H is given as (25).

$$H = \frac{V_0}{V_{dc}} = \frac{D}{2-D} \quad (25)$$

2.4.2. The voltage conversion ratio for D ≥ 0.5

During the stable state, the average value of voltage is zero across inductor, which can be expressed utilizing volt-sec principle [22], [39]. For getting expression of Lx, (26) is written using voltage-second balance:

$$(V_{dc} - V_c)DT_s - (V_{dc} - 2V_c)(1 - D)T_s = 0 \quad (26)$$

The expression for V_{dc}obtained from equation (26) is written as (27).

$$V_{dc} = V_c(2 - D) \quad (27)$$

By applying the volt-sec principle to the inductor L_1, (28) is obtained:

$$(V_c - V_o)DT_s - V_0\,(0.5 - D)T_s = 0 \quad (28)$$

The expression for V_o obtained from equation (28) is written as (29).

$$V_0 = V_c * D \quad (29)$$

Substituting the value of V_c from (27) into (29), ratio of conversion of voltage (H′) is determined as (30).

$$H' = \frac{V_0}{V_{dc}} = \frac{D}{2-D} \quad (30)$$

2.5. Design value of inductor

As previously mentioned, the proposed converter allows for the selection of a smaller inductor value. Utilizing appropriate equations, the inductor value has been determined and is presented for two duty cycle scenarios, as detailed in references [22] and [39]. This design flexibility enables optimization for various operational conditions, enhancing the converter's performance and versatility.

2.5.1. For D ≤ 0.5

The ripple associated with inductor L_x is given in (31).

$$\Delta iL_x = \frac{V_o(1-D)T_s}{L_x} \quad (31)$$

The inductor current ripple of the inductors L_1 and L_2, which are assumed to be identical ($L_1 = L_2 = L$) is given in (32).

$$\Delta iL = \frac{V_o(1-D)T_s}{L} \quad (32)$$

With $D \leq 0.5$, the minimum values for the design of inductors L_1, L_2, and L_x can be evaluated with the average and ripple currents. The minimum value of the current for inductor L_x, L_1, and L_2 are given in (33)-(35).

$$I_{Lx_{min}} = I_{Lx_{avg}} - \left(\frac{\Delta i_{Lx}}{2}\right) \quad (33)$$

$$I_{L1_{min}} = I_{L1_{avg}} - \left(\frac{\Delta i_{L1}}{2}\right) \quad (34)$$

$$I_{L2_{min}} = I_{L2_{avg}} - \left(\frac{\Delta i_{L2}}{2}\right) \quad (35)$$

The minimum value of inductor current at the boundary condition is zero and written as (36)-(37).

$$0 = I_{Lx_{min}} \quad (36)$$

$$I_{Lx_{avg}} = \left(\frac{\Delta i_{Lx}}{2}\right) \quad (37)$$

The average inductor current, I_{Lx}, for the L_x is same as I_{in}, which is determined by equating average power supplied by the input with average power absorbed by the load, as (38).

$$P_0 = P_{in} \quad (38)$$

Where, output power is represented by P_o and input power by P_{in}.

From (39), I_{in} can be expressed in terms of the V_o, V_{dc}, and I_o as (40).

$$V_0 I_0 = V_{dc} I_{in} \quad (39)$$

$$I_{Lx_{avg}} = I_{in} = \frac{V_0 I_0}{V_{dc}} \quad (40)$$

By substituting (25) in (40) we get (41).

$$I_{Lx_{avg}} = \left(\frac{D}{2-D}\right) I_0 \quad (41)$$

Therefore, by substituting the (31) and (41) in (37), the boundary load (r_{LX}) for L_x is computed and given in (42).

$$R_{Lx} = \frac{2L_x D}{(1-D)(2-D)T_s} \quad (42)$$

Where, $L_{x_{min}}$ is the minimum value of inductance at this condition and given as (43).

$$L_{x_{min}} = \frac{(1-D)(2-D)R_{LB}T_s}{2D} \quad (43)$$

Therefore, the value of $L_{x_{min}}$ has been taken as 14.4 µH. Similarly, the minimum value of current at boundary for inductor L_1 and L_2 (L_1=L_2=L) is given in (44).

$$I_{L1_{min}} = I_{L2_{min}} = I_{L_{min}} = 0 \quad (44)$$

The average inductor current for L_1 and L_2 is given in (45).

$$I_{L_{avg}} = \frac{\Delta i_L}{2} \quad (45)$$

Each inductor carries the average value of current same as that of half of the load current as in (46).

$$\frac{I_{OB}}{2} = \frac{(1-D)T_S V_O}{L} \quad (46)$$

Where, I_{OB} is the boundary load current. The minimum value of the inductance required for continuous conduction mode can be computed from the (47).

$$L_{1_{min}} = L_{2_{min}} = L_{min} = R_{LB}(1-D)T_s \quad (47)$$

The values of $L_{1_{min}}$ and $L_{2_{min}}$ are computed as 3.2 µH.

2.5.2. For D ≥ 0.5

For duty cycles greater than 0.5, the analysis can be carried out for the design of the inductor values as well as for the value of ripple in inductor current in the similar way as presented in above section. In this case, the ripple in inductor current will be same as that of (31) and (32). The values of the minimum inductances for the consideration of design for D ≥ 0.5 are similar to that of the (43) and (47).

2.6. Power losses and efficiency

Table 1 shows various losses considered for the proposed converter. The losses resulting from conduction and switching are evaluated for all GaN-FET switches, assuming identical on-state resistance (r_{ds}) and output capacitance (Cr) of the switches respectively. The forward resistance of diodes is given as r_d and V_d is the forward voltage of diodes. The analysis is done including parasitic resistances of inductors and assuming all capacitors as ideal [39], [40]. The converter's efficiency can be computed as (48) and losses as (49),

$$\eta = \frac{P_0}{P_0 + P_{loss}} = \frac{1}{1+\frac{P_{loss}}{P_0}} \quad (48)$$

Where:

$$P_{loss} = P_{r_{ds}} + P_s + P_d + P_{fd} + P_{r_{Lx}} + P_{r_L} \quad (49)$$

Table 1. Power losses for the proposed converter

Losses	Expression	Losses	Expression
Conduction losses of switches (P_{rds})	$\left(\frac{3}{4}\right) r_{ds} \left(\frac{P_0}{R_L}\right) D$	Forward bias loss of diode (P_{fd})	$\frac{V_d(1-D)}{V_0}$
Switching losses (P_s)	$\frac{3C_r P_0 R_L}{D^2 T_s}$	Loss due to r_{Lx} (Pr_{Lx})	$rL_x \left(\frac{D}{2-D}\right)^2 \left(\frac{P_0}{R_L}\right)$
Conduction losses of diodes (P_d)	$\frac{P_0 r_d (1-D)}{2R_L}$	Loss due to r_{L1} and r_{L2} (Pr_L)	$\left(\frac{r_L}{2R_L}\right) P_0$

3. RESULTS AND DISCUSSION

The simulation-based model of the proposed converter with GaN-FET switches and the converter with MOSFET switches has been designed as shown in Figure 8, based on the parameters given in Table 2. The specifications of the switches have been given in Table 3. The operating duty ratio range of converter is set between 0.2 and 0.75, with a minimum load resistance of 2 Ω and a maximum of 24 Ω. From (43) and (47), the minimum possible values of the inductance L_{xmin} for the proposed converter with a chosen switching frequency of 500 kHz is calculated as 14.4 µH and the $L_{1min} = L_{2min} = 3.2$ µH.

3.1. Voltage output obtained from converter

The voltage output of proposed converter and the converter with MOSFET switches has been evaluated with a duty cycle of 0.4 and 0.7 by using the parameters in Tables 2 and 3. Figures 9 and 10 compare the output voltage of the proposed converter with GaN-FET and MOSFET-based converter. The results show that the output voltage of the proposed converter is 4.62 V and 10.46 V at a duty cycle of 0.4 and 0.7 respectively. The output voltage with MOSFET reaches 4.592 V and 10.29 V at a duty cycle of 0.4 and 0.7 respectively. Therefore, the proposed converter with GaN-FET leads to an increase in the output voltage as compared to MOSFET-based converter.

Furthermore, a comparison has been drawn between proposed converter with GaN-FET switches and existing converter with MOSFET switches over wide range of duty cycles considered from 0.3 and 0.7. The results shown in Figure 11, indicate that at 0.3 duty ratio, the proposed converter has output voltage of 3.2 V, while the converter with MOSFET switches has an output voltage of 3.1 V. At a duty ratio of 0.7, the proposed converter has an output voltage of 10.46 V, which is higher than 10.29 V output voltage achieved by

converter with MOSFET switches. Therefore, it can be comprehended that the proposed converter has a wider operating range with better output voltage performance. Table 4 shows the comparison of output voltage at different duty cycles.

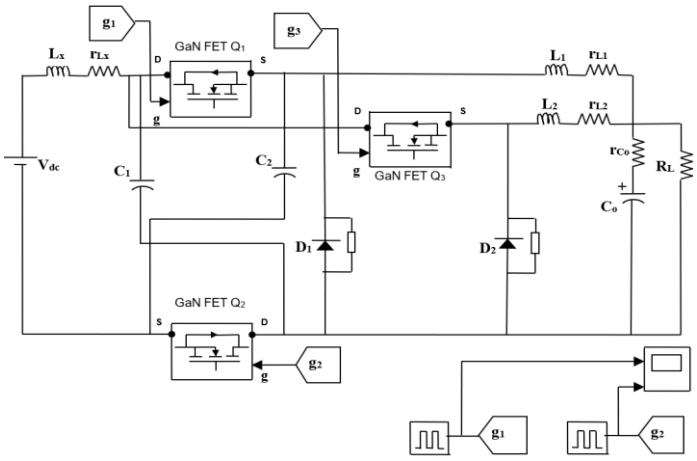

Figure 8. Simulink-based model of proposed converter

Table 2. Parameters for circuit simulation of converters using MOSFET and GaN-FET

Circuit variable	MOSFET	GaN-FET
Input voltage (V_{dc})	20 V	20 V
Switching Frequency (f_s)	50 kHz	500 kHz
Inductance	L_a, L_b, L_m = 180 µH	L_1, L_2, Lx = 75 µH
Parasitic resistance of inductor	r_{Lm}, r_{La}, r_{Lb} = 0.07 Ω	r_{Lx}, r_{L1}, r_{L2} = 0.02976 Ω
The capacitance of identical capacitors	220 µF	220 µF
The capacitance of the output capacitor (C_o)	330 µF	330 µF
Forward voltage drop of diode (V_d)	0.39 V	0.39 V
Forward resistance of diode (r_d)	0.078 Ω	0.078 Ω
Parasitic resistance of output capacitance(r_c)	0.22 Ω	0.22 Ω

Table 3. Electrical characteristics of power switches for simulation

GaN-FET	Si-MOSFET	
EPC	Infineon	Supplier
EPC2215	IRFP250NPbF	Part number
0.008 Ω	0.075 Ω	On-state resistance
390 pF	315 pF	Output capacitance
2 pF	83pF	Reverse transfer capacitance
200 V	200 V	Drain to source voltage
1356 pF	2159pF	Input capacitance

Table 4. Comparison of output voltage at different duty ratios

Duty ratio	Output voltage of converter with MOSFET (V)	Output voltage of proposed converter (V)
0.3	3.155	3.169
0.4	4.6	4.7
0.5	6.272	6.335
0.6	8.14	8.25
0.7	10.29	10.46

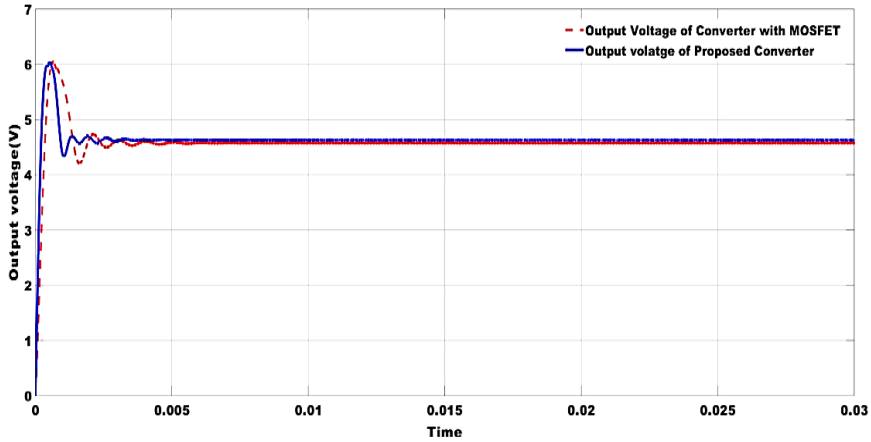

Figure 9. Output voltage at 0.4 duty cycle

3.2. Assessment of input and output current ripple

The output current ripple of proposed converter and converter based on MOSFET switches has been compared and the waveforms are shown in Figures 12 and 13 at a duty cycle of 0.4 and 0.7 respectively. At a duty cycle of 0.4, the proposed converter has the ripple of 0.027 A in output current, while the converter with MOSFET switches have a ripple of 0.114A in output current. Similarly, at duty cycle of 0.7, ripple of 0.05A appears in output current of proposed converter as compared to 0.21 A ripple in output current of a converter with MOSFET switches. Therefore, the proposed converter with GaN-FET has reduced the ripple content in the output current more efficiently than the MOSFET-based converter.

The input current ripple of proposed converter and MOSFET-based converter has been shown in the Figures 14 and 15 at a duty cycle of 0.4 and 0.7 respectively. The ripple in input current of the proposed converter is 0.0817 A and 0.089 A at a duty cycle of 0.4 and 0.7 respectively whereas input current ripple of the MOSFET based converter is 0.3396 A and 0.3647 A at a duty cycle of 0.4 and 0.7 respectively. Therefore, the proposed converter with GaN-FET exhibits better results in reducing the input current ripple as compared to the converter with MOSFET switches.

3.3. Assessment of output voltage ripple

The output voltage ripple of the proposed converter and the converter with MOSFET switches has been compared at a duty cycle of 0.4 and 0.7 respectively as shown in Figure 16 and Figure 17. The proposed converter exhibits a ripple of 0.005 V at 0.4 duty cycle, while the converter with MOSFET switches have a ripple of 0.04 V. Similarly, at 0.7 duty cycle, the proposed converter has ripple of 0.01 V whereas, converter with MOSFET switches has ripple of 0.024 V. Hence, the results indicate that the proposed converter with GaN-FET exhibits better performance in reducing the output voltage ripple.

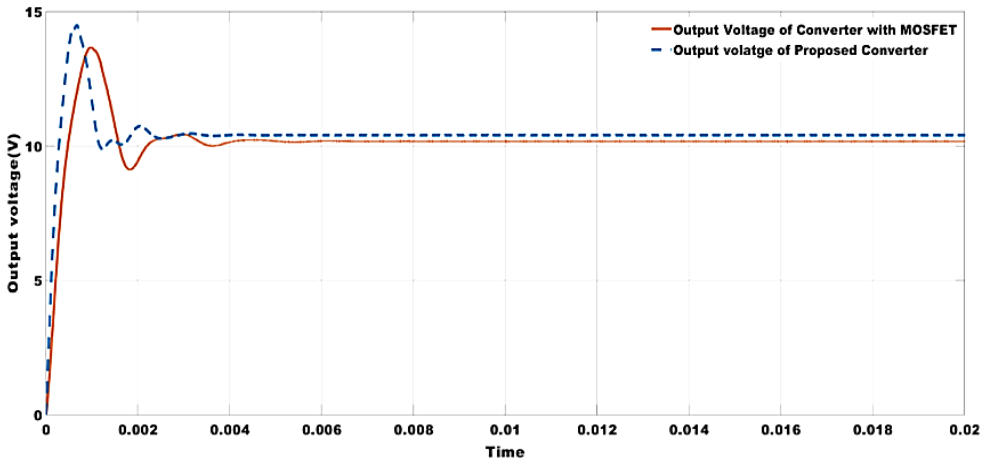

Figure 10. Output voltage at 0.7 duty cycle

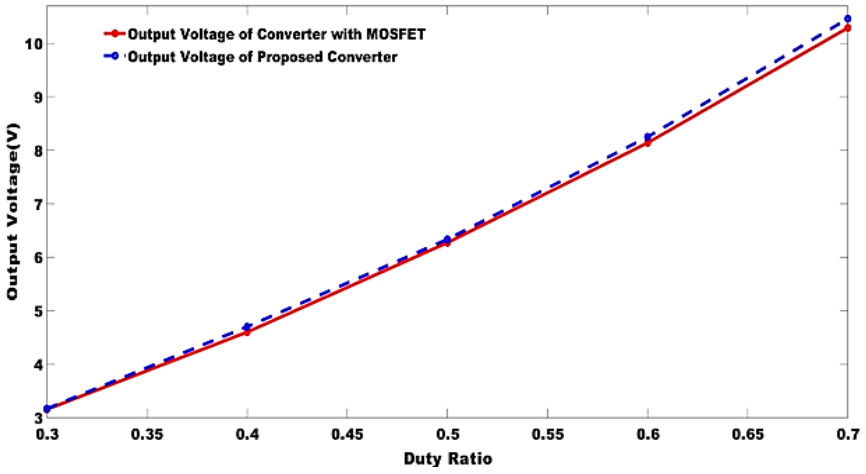

Figure 11. Output voltage for different duty ratios

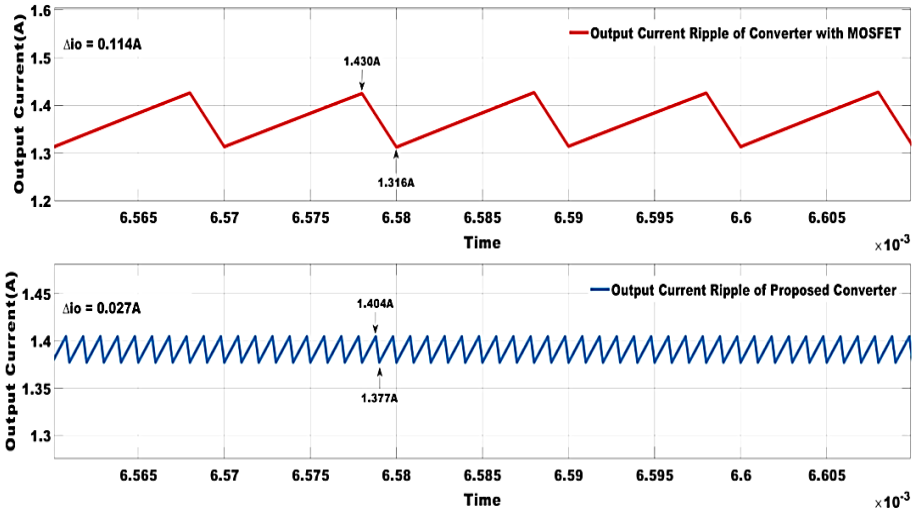

Figure 12. Comparison of output current ripple at duty cycle of 0.4

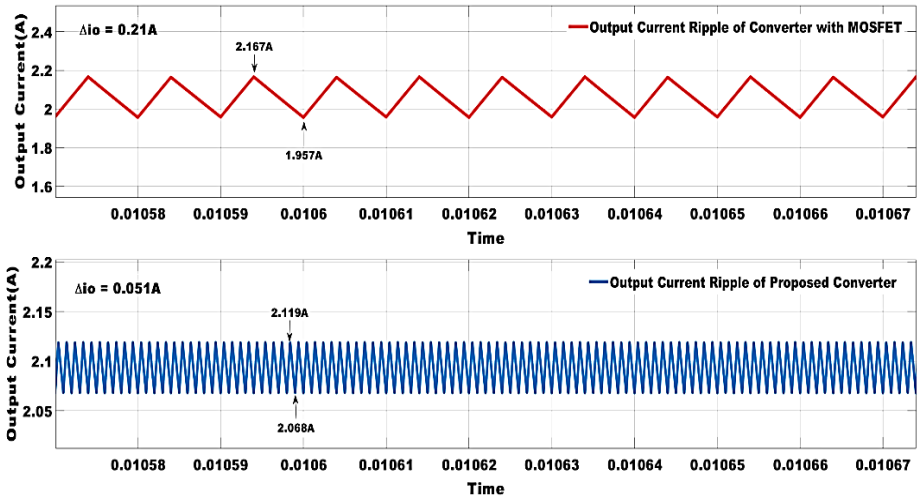

Figure 13. Comparison of output current ripple at duty cycle at 0.7

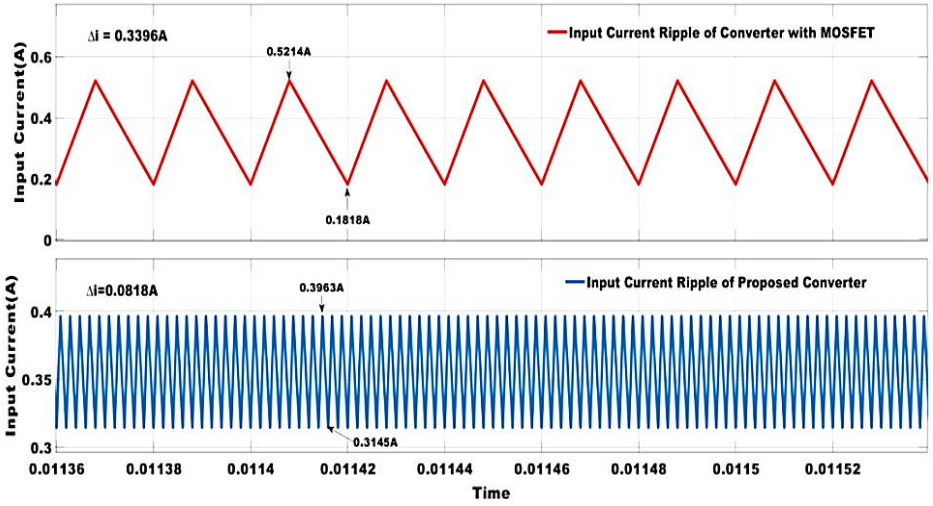

Figure 14. Comparison of input current ripple at duty cycle of 0.4

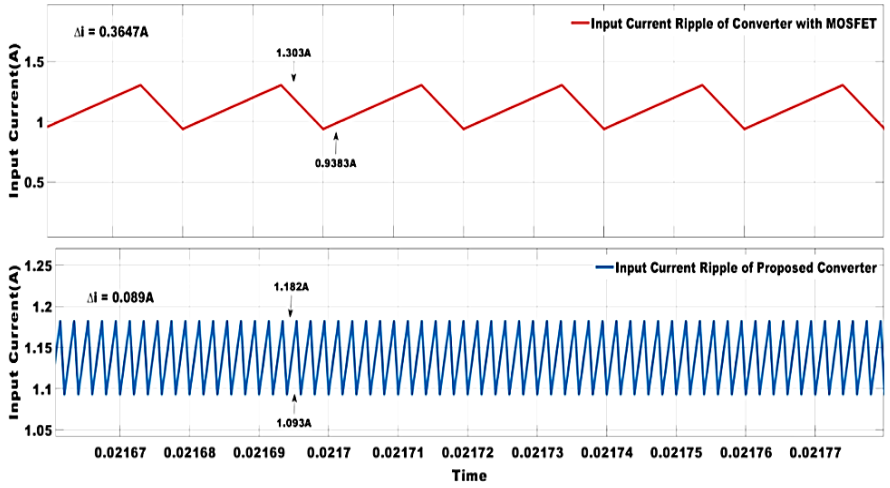

Figure 15. Comparison of input current ripple at duty cycle of 0.7

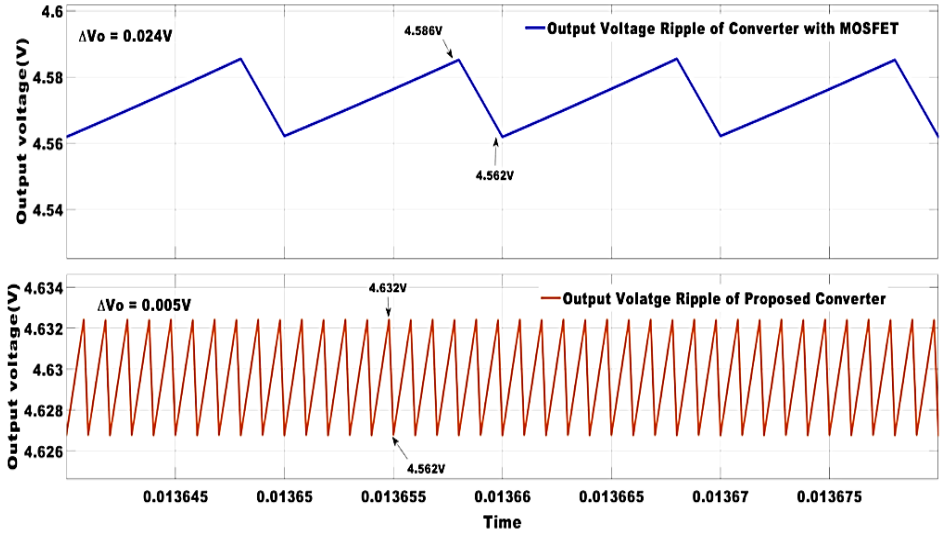

Figure 16. Comparison of output voltage ripple at duty cycle of 0.4

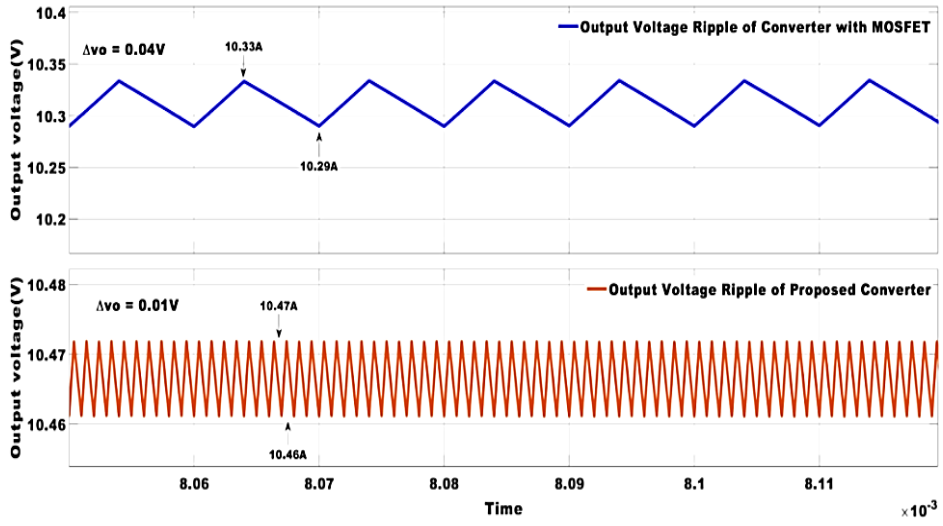

Figure 17. Comparison of output voltage ripple at duty cycle at 0.7

3.4. Assessment of efficiency

The proposed converter's efficiency has been evaluated at duty cycle ranging from 0.4 and 0.7 and the outcomes have been presented in Figure 18. The proposed converter achieves an efficiency of 90.55% at a 0.4 duty cycle and reaches to 96.31% at a duty cycle of 0.7. In comparison, the efficiency of converter with converter MOSFET switches is 89.39% at a duty cycle of 0.4 which increases to 94.86% at a duty cycle of 0.7. Hence, the efficiency has been optimized by the proposed converter with GaN-FET at all duty cycles under consideration.

Furthermore, the efficiency of the proposed converter is evaluated by increasing the load resistance, and the results have been compared with those of existing converter based on power MOSFET switches. Figure 19 depicts that the proposed converter with GaN-FET maintains higher efficiency at all load resistances considered than the existing converter. Table 5 shows the values of efficiency obtained with the two compared converters for different duty cycles. Table 6 shows the values of efficiency obtained with the two compared converters with the varying load resistance.

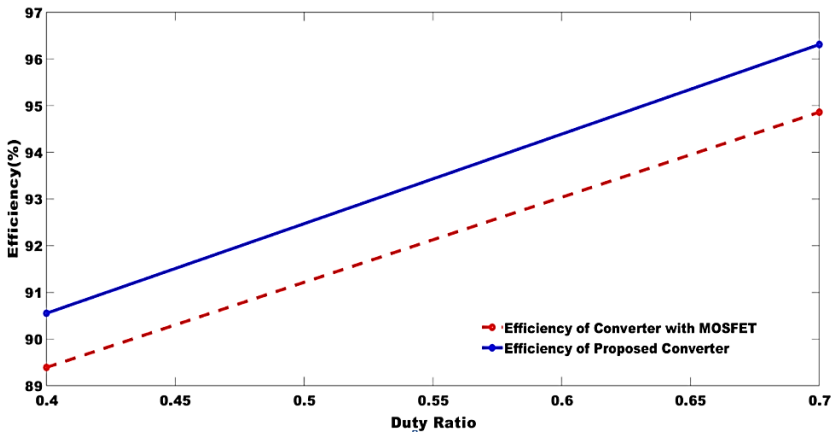

Figure 18. Efficiency evaluation of proposed converter at various duty ratios

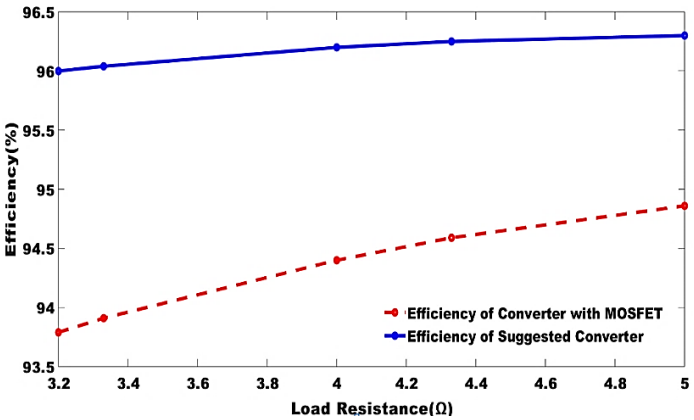

Figure 19. Efficiency evaluation of the proposed converter at various load resistances

Table 5. Comparison of η for different duty cycle

Duty cycle	Proposed converter η(%)	Converter with MOSFET switches η (%)
0.4	90.55	89.39
0.7	96.31	94.86

Table 6. Comparison of η with varying load resistance

Load resistance (Ω)	Proposed converter η (%)	Converter with MOSFET switches η (%)
3.2	96	93.79
3.33	96.04	93.91
4	96.2	94.4
4.33	96.25	94.59
5	96.3	94.86

3.5. Losses evaluation

The power losses of the proposed converter and the converter with MOSFETs have been evaluated at a duty cycle of 0.4 and 0.7 and the outcomes are depicted in Figure 20. The power losses of the converter with MOSFET switches are 0.218 W and 0.474 W at 0.4 and 0.7 duty cycle respectively whereas the power losses of the proposed converter are obtained as 0.026 W and 0.314 W at respective duty cycles. Therefore, as per the evaluated results, the power losses have decreased with proposed converter as compared to the existing converter with MOSFET switches. The reduction in power losses lead to increased efficiency, which leads to cost savings and improved performance in many applications.

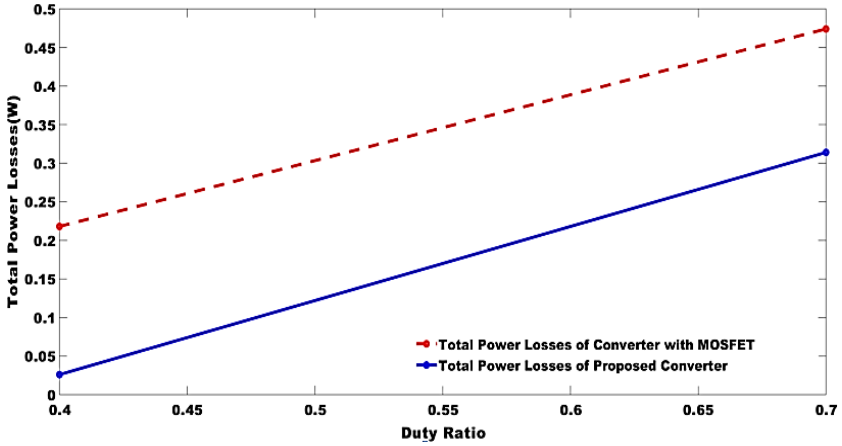

Figure 20. Comparison of total power losses of the proposed converter and existing converter at various duty ratios

4. EXPERIMENTAL VERIFICATION

A prototype of the topology is developed as shown in Figure 21 with specifications of GaN-FET switches as presented in Table 3. To assess the converter's performance in a real-time environment, an experimental setup is implemented with elevated operating values, as illustrated in Figure 22. The developed converter demonstrates an input voltage range, extending up to 50 V, and a rating of 800 W. This augmentation in scale provides a comprehensive evaluation of the converter's capabilities, allowing for a thorough examination of its behavior under conditions that closely resemble practical applications. The experimental setup consists of controlled DC power supply, programmable electronic load (current sink), series resistive shunts, heat sinks and cooling fan for DC-DC converter heat dissipation and measurement equipment.

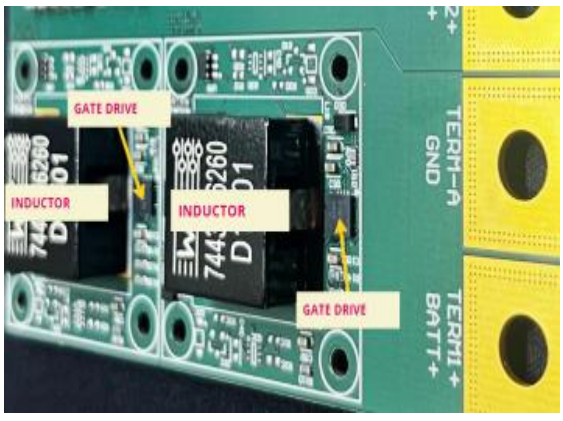

Figure 21. Developed prototype of the converter

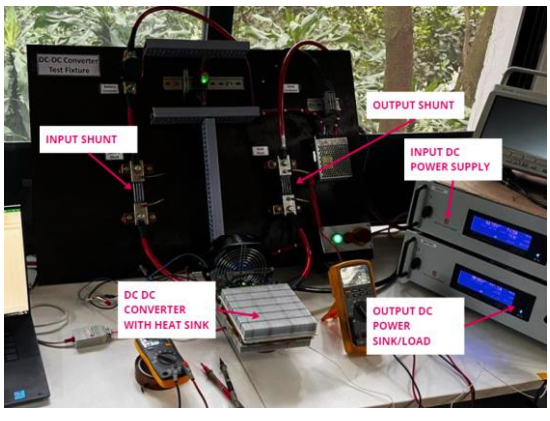

Figure 22. Experimental set-up of proposed IBC

While co-relating results of experimental set-up and simulation, it should be noted that experimental prototype has a higher rating in comparison to the values employed in the simulation model. This is done to assess the proposed converter's performance in a real-time environment. Scope shot in Figure 23 shows the

180° phase shifted gate pulses for GaN-FET drive in buck converter. One of the gate pulses is for Q_1, Q_2 and other for Q_3. Input and output voltage for the developed converter is shown in Figure 24. The output voltage in the Figure 24 is corresponding to a duty ratio of 0.8 and can be validated as per equations (24) and (29) given in section 2. Figure 25 shows the voltage and current waveforms of the developed converter when connected to an active load. Highlighted measurements are captured with a duty cycle of 0.6 (14 V/2.5 A), 0.7 (16 V/7.5 A) and 0.8 (18 V/12.5 A). Figure 26 shows the waveforms for inductor current (L_1/L_2) at duty cycle of 0.2 for the developed converter.

Table 7 summarizes the test results of the developed DC-DC converter. The developed converter is tested as a current controlled source for battery charging application. During testing, battery was charged with charging current ranging from 11.80 A to 25.30 A. The steady state heat sink temperature varies from 62.69 °C to 83.61 °C. As on-state resistance (r_{DSON}) of the GaN-FET increases with rise in temperature, there is increase in the conduction losses of GaN switches from 0.501 W to 2.688 W under the given testing conditions. These losses are only 2% to 10% of total losses. It is highlighted here that overall efficiency of the developed converter is maintained above 96% with output currents ranging from 10 A to 25 A approximately.

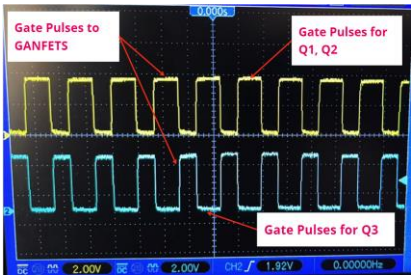

Figure 23. Gate pulses for Q_1,Q_2, and Q_3

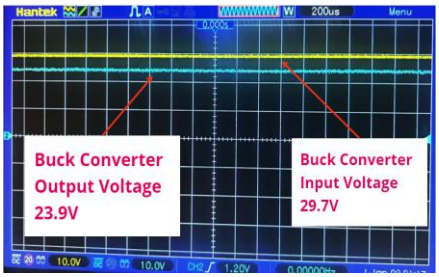

Figure 24. Output and input voltage waveforms

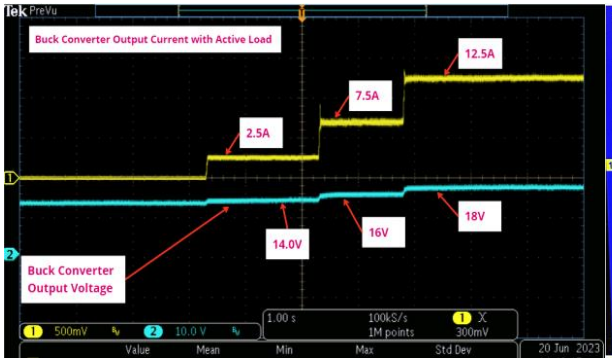

Figure 25. Output voltage and output current waveforms

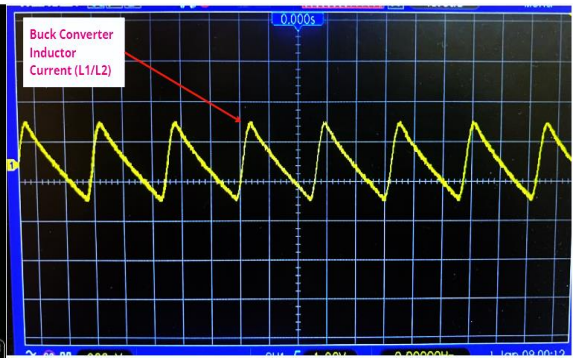

Figure 26. Inductor (L_1 /L_2) current

Table 7. Efficiency and losses

Input voltage (volts)	Output voltage (volts)	Temperature (heat sink) (°C)	Input shunt voltage (mV)	Input current (A)	Output shunt voltage (mV)	Output current (A)	P_{input} (W)	P_{output} (W)	Efficiency η (%)	Losses (W)	GaN-FET conduction losses (W)
43.91	36.14	62.69	10.10	10.10	11.80	11.80	443.49	426.45	96.158	17.04	0.501
43.87	36.22	75.11	15.10	15.10	17.70	17.70	662.44	641.09	96.778	21.34	1.222
43.83	34.37	83.61	20.40	20.40	25.30	25.30	894.13	869.56	97.252	24.57	2.688

5. CONCLUSION

In this paper, a switched capacitor cell based interleaved buck converter with GaN-FET switches has been explored, with the aim to achieve higher efficiency. To validate the potential of the proposed converter, its performance has been compared against conventional MOSFET-based converter. The evaluation considers various performance indices viz. efficiency, power losses, output voltage, input current ripple, output current ripple and output voltage ripple. The outcomes show reduced power losses, thus leading to higher efficiency at varying duty cycles and different loading conditions. Additionally, it supports the use of a small inductor (reduced size), high frequency operation and provides better output voltage regulation. Experimental results further validate the

simulation results of this research work. In future work, one potential path involves addition of a current control loop to control the output voltage in case of dynamic changes in input voltage. Also, the presented converter can be analysed for discontinuous conduction and the inductors can be replaced with the coupled inductors.

ACKNOWLEDGEMENTS

Authors thank University Institute of Engineering and Technology, Panjab University, Chandigarh, India for their support during this research work. Experimental verification has been supported by Brighten Controls LLP, Bangalore, India.

REFERENCES

[1] P. Nandankar and J. P. Rothe, "Design and implementation of efficient three-phase interleaved DC-DC converter," in *2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT)*, IEEE, Mar. 2016, pp. 1632–1637, doi: 10.1109/ICEEOT.2016.7754962.

[2] M. Esteki, B. Poorali, E. Adib, and H. Farzanehfard, "Interleaved buck converter with continuous input current, extremely low output current ripple, low switching losses, and improved step-down conversion ratio," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 8, pp. 4769–4776, Aug. 2015, doi: 10.1109/TIE.2015.2397881.

[3] M. Biswas, S. Majhi, and H. Nemade, "Performance of a coupled inductor for interleaved buck converter with improved step-down conversion ratio," *IET Power Electronics*, vol. 14, no. 2, pp. 239–256, Feb. 2021, doi: 10.1049/pel2.12029.

[4] A. Garg and M. Das, "High efficiency three phase interleaved buck converter for fast charging of EV," in *2021 1st International Conference on Power Electronics and Energy (ICPEE)*, IEEE, Jan. 2021, pp. 1–5, doi: 10.1109/ICPEE50452.2021.9358486.

[5] K. Murugappan, R. Seyezhai, G. K. Sabarish, N. Kaashyap, and J. Jason Ranjit, "Simulation and analysis of interleaved buck DC-DC converter for EV charging," 2020, pp. 369–380,. doi: 10.1007/978-981-15-7245-6_28.

[6] P. Alavi, E. Babaei, P. Mohseni, and V. Marzang, "Study and analysis of a DC–DC soft-switched buck converter," *IET Power Electronics*, vol. 13, no. 7, pp. 1456–1465, May 2020, doi: 10.1049/iet-pel.2019.0431.

[7] H. Li, H. Du, Y. Zeng, Z. Qiu, X. Jiang, and Z. Chen, "A modified interleaved capacitor clamped DC–DC converter with non-resonant soft switching," *IEEE Transactions on Power Electronics*, vol. 37, no. 10, pp. 12221–12236, Oct. 2022, doi: 10.1109/TPEL.2022.3163010.

[8] A. Algamluoli, X. Wu, H. M. Abdulhadi, Kitmo, and M. A. Khan, "Ultra high voltage gain non-isolated DC-DC converter based on new interleaved triple boosting technique," *Frontiers in Energy Research*, vol. 11, Sep. 2023, doi: 10.3389/fenrg.2023.1273155.

[9] Y.-M. Chen, S.-Y. Tseng, C.-T. Tsai, and T.-F. Wu, "Interleaved buck converters with a single-capacitor turn-off snubber," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 40, no. 3, pp. 954–967, Jul. 2004, doi: 10.1109/TAES.2004.1337467.

[10] C.-T. Tsai and C.-L. Shen, "Interleaved soft-switching coupled-buck converter with active-clamp circuits," in *2009 International Conference on Power Electronics and Drive Systems (PEDS)*, IEEE, Nov. 2009, pp. 1113–1118, doi: 10.1109/PEDS.2009.5385749.

[11] K. Yao, Y. Qiu, M. Xu, and F. C. Lee, "A novel winding-coupled buck converter for high-frequency, high-step-down DC–DC conversion," *IEEE Transactions on Power Electronics*, vol. 20, no. 5, pp. 1017–1024, Sep. 2005, doi: 10.1109/TPEL.2005.854022.

[12] C. Lin *et al.*, "Study on an interleaved buck power factor corrector with gallium nitride field effect transistor and integrated inductor," *IET Power Electronics*, vol. 7, no. 10, pp. 2506–2516, Oct. 2014, doi: 10.1049/iet-pel.2013.0642.

[13] M. Ilic and D. Maksimovic, "Interleaved zero-current-transition buck converter," *IEEE Transactions on Industry Applications*, vol. 43, no. 6, pp. 1619–1627, 2007, doi: 10.1109/TIA.2007.908175.

[14] D. Zhang *et al.*, "Optimal duty ratio assisted PFM control for vhf isolated class E DC-DC converter," *IEEE Transactions on Power Electronics*, vol. 38, no. 12, pp. 15467–15480, Dec. 2023, doi: 10.1109/TPEL.2023.3317910.

[15] J. S. R. Kumar, H. V. Du John, B. K. J. I.V, J. Ajayan, A. D. A, and D. Nirmal, "A comprehensive review of AlGaN/GaN High electron mobility transistors: Architectures and field plate techniques for high power/ high frequency applications," *Microelectronics Journal*, vol. 140, p. 105951, Oct. 2023, doi: 10.1016/j.mejo.2023.105951.

[16] F. Marvi, E. Adib, and H. Farzanehfard, "Zero voltage switching interleaved coupled inductor synchronous buck converter operating at boundary condition," *IET Power Electronics*, vol. 9, no. 1, pp. 126–131, Jan. 2016, doi: 10.1049/iet-pel.2014.0960.

[17] M. Esteki, B. Poorali, E. Adib, and H. Farzanehfard, "High step-down interleaved buck converter with low voltage stress," *IET Power Electronics*, vol. 8, no. 12, pp. 2352–2360, Dec. 2015, doi: 10.1049/iet-pel.2014.0976.

[18] T. Kahl, L. Wernicke, S. Dieckerhoff, C. Fromme, M. Tannhauser, and A. Siemens, "All-GaN bidirectional ANPC-based resonant DC-DC converter," in *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, IEEE, Sep. 2020, p. P.1-P.10, doi: 10.23919/EPE20ECCEEurope43536.2020.9215705.

[19] A. Zakaria, M. I. Marei, and H. M. Mashaly, "A hybrid interleaved DC-DC converter based on buck-boost topologies for medium voltage applications," *e-Prime - Advances in Electrical Engineering, Electronics and Energy*, vol. 6, p. 100301, Dec. 2023, doi: 10.1016/j.prime.2023.100301.

[20] D.-T. Do, H. Cha, B. L.-H. Nguyen, and H.-G. Kim, "Two-channel interleaved buck LED driver using current-balancing capacitor," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 3, pp. 1306–1313, Sep. 2018, doi: 10.1109/JESTPE.2018.2845858.

[21] M. G. Adivi and M. R. Yazdani, "A forward-integrated buck DC-DC converter with low voltage stress for high step-down applications," *Journal of Power Electronics*, vol. 18, no. 2, pp. 356–363, 2018, doi: 10.6113/JPE.2018.18.2.356.

[22] M. Biswas, S. Majhi, and H. Nemade, "Two-phase high efficiency interleaved buck converter with improved step-down conversion ratio and low voltage stress," *IET Power Electronics*, vol. 12, no. 15, pp. 3942–3952, Dec. 2019, doi: 10.1049/iet-pel.2019.0547.

[23] S. Khoshzaman and I. Hahn, "A performance comparison of GaN FET and silicon MOSFET," in *2021 22nd IEEE International Conference on Industrial Technology (ICIT)*, IEEE, Mar. 2021, pp. 127–133, doi: 10.1109/ICIT46573.2021.9453693.

[24] A. Letellier, M. R. Dubois, J. P. Trovao, and H. Maher, "Gallium nitride semiconductors in power electronics for electric vehicles: advantages and challenges," in *2015 IEEE Vehicle Power and Propulsion Conference (VPPC)*, IEEE, Oct. 2015, pp. 1–6, doi: 10.1109/VPPC.2015.7352955.

[25] P. Tarassodi, J. Adabi, and M. Rezanejad, "Energy management of an integrated PV/battery/electric vehicles energy system interfaced by a multi-port converter," *International Journal of Engineering*, vol. 36, no. 8, pp. 1520–1531, 2023, doi: 10.5829/IJE.2023.36.08B.12.

[26] P. Ramesh, P. Kumar Gouda, A. Rameshbabu, G. Ramanathan, and C. Bharatiraja, "An isolated multi-port bidirectional DC-DC converter for EV applications," *Materials Today: Proceedings*, vol. 68, pp. 1853–1859, 2022, doi: 10.1016/j.matpr.2022.08.047.

[27] S. Norouzi, H. Ghoreishy, A. A. Ahmad, and F. Tahami, "A new variable frequency zero voltage switching control method for boost converter operating in boundary conduction mode," *International Journal of Engineering*, vol. 33, no. 11, Nov. 2020, doi: 10.5829/ije.2020.33.11b.14.
[28] M. Kaufmann and B. Wicht, "A monolithic GaN-IC with integrated control loop for 400-V offline buck operation achieving 95.6% peak efficiency," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 12, pp. 3169–3178, Dec. 2020, doi: 10.1109/JSSC.2020.3018404.
[29] T. Mishima, R. Miyazaki, and C.-M. Lai, "GaN-HEMT MHz-driving current-fed snubberless ZCS high step-up dc-dc converter for fuel cell vehicles," in *2021 IEEE International Future Energy Electronics Conference (IFEEC)*, IEEE, Nov. 2021, pp. 1–6, doi: 10.1109/IFEEC53238.2021.9661902.
[30] M. Mosayebi, M. Gheisarnejad, H. Farsizadeh, B. Andresen, and M. H. Khooban, "Smart extreme fast portable charger for electric vehicles-based artificial intelligence," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 2, pp. 586–590, Feb. 2023, doi: 10.1109/TCSII.2022.3176863.
[31] V. M. Iyer, S. Gulur, G. Gohil, and S. Bhattacharya, "An approach towards extreme fast charging station power delivery for electric vehicles with partial power processing," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 10, pp. 8076–8087, Oct. 2020, doi: 10.1109/TIE.2019.2945264.
[32] A. M. S. Al-bayati, S. S. Alharbi, S. S. Alharbi, and M. Matin, "A comparative design and performance study of a non-isolated DC-DC buck converter based on Si-MOSFET/Si-Diode, SiC-JFET/SiC-schottky diode, and GaN-transistor/SiC-Schottky diode power devices," in *2017 North American Power Symposium (NAPS)*, IEEE, Sep. 2017, pp. 1–6, doi: 10.1109/NAPS.2017.8107192.
[33] Q. Tan, L. Mao, Y. Cai, B. Zhang, and Z. Ruan, "Comparative evaluation and analysis of GaN-based VSIs and CSIs," *Energy Reports*, vol. 9, pp. 568–576, Mar. 2023, doi: 10.1016/j.egyr.2022.11.082.
[34] A. M. S. Al-bayati and M. Matin, "A Highly efficient GAN E–HEMT/SIC Schottky diode power device based DC–DC zeta converter," in *2018 IEEE Conference on Technologies for Sustainability (SusTech)*, IEEE, Nov. 2018, pp. 1–5, doi: 10.1109/SusTech.2018.8671330.
[35] Y. Yang, Y. Liu, Y. Zhao, J. Liu, and B. Zhu, "High frequency and high power density bipolar DC–DC converter with GaN HEMT," *Energy Reports*, vol. 9, pp. 617–624, Sep. 2023, doi: 10.1016/j.egyr.2023.04.110.
[36] M. Orr, S. Finney, and D. Holliday, "Non-isolated resonant link DC–DC converter for use with GaN devices," *The Journal of Engineering*, vol. 2019, no. 17, pp. 4200–4204, Jun. 2019, doi: 10.1049/joe.2018.8066.
[37] E. B. Bulut, M. O. Gulbahce, and D. A. Kocabas, "Analysis of a GaN based PWM AC-AC converter with an improved switch loss model," *AEU - International Journal of Electronics and Communications*, vol. 131, p. 153578, Mar. 2021, doi: 10.1016/j.aeue.2020.153578.
[38] Z. Zheng, H. Xu, L. Zhang, and K. J. Chen, "On the operating speed and energy efficiency of GaN-based monolithic complementary logic circuits for integrated power conversion systems," *Fundamental Research*, vol. 1, no. 6, pp. 661–671, Nov. 2021, doi: 10.1016/j.fmre.2021.09.015.
[39] A. Ioinovici, *Power Electronics and Energy Conversion Systems: Fundamentals and Hard-switching Converters*. John Wiley & Sons, Ltd, 2013. doi: 10.1002/9781118443040.
[40] K.-C. Tseng and C.-C. Huang, "High step-up high-efficiency interleaved converter with voltage multiplier module for renewable energy system," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 3, pp. 1311–1319, Mar. 2014, doi: 10.1109/TIE.2013.2261036.

BIOGRAPHIES OF AUTHORS

Puneet Kaur is currently working as an assistant professor in the Department of Electrical and Electronics Engineering (EEE) at UIET, Panjab University, Chandigarh, India. Holding a Ph.D. in Power Electronics from Panjab University and M.E. in Power Systems from Punjab Engineering College, Chandigarh, she has interest in the applications of power electronics in power systems, electric drives, and DC-DC converters for efficient power transfer. Her research journey includes development of a DC motor performance analyzer for comprehensive data analysis and consultancy project on battery monitoring for electric vehicles. She can be contacted at email: puneetee@pu.ac.in.

Payal Jaswal is working as post graduate engineer at Jacobs Engineering Pvt. Ltd, India. She has done her masters in Power Systems from University Institute of Engineering and Technology, Panjab University, Chandigarh and Bachelor of Engineering from DAV Institute of Engineering and Technology, Jalandhar. She can be contacted at email: payaljaswal02@gmail.com.

Aditi Gupta is assistant professor in Electrical and Electronics Engineering Department, UIET, Panjab University, Chandigarh, India. She has completed her B.Tech. in Electrical Engineering from Kurukshetra University, India in 2002 with honours, M.E. in Electrical Engineering from PEC, Chandigarh, India in 2004 with distinction and Ph.D. from Panjab University, Chandigarh, India in 2019, in the area of ancillary services management including renewables. Her research interests include ancillary services management in deregulated power systems, load frequency control, reactive power management, congestion management, power electronics, and renewable energy resources. She has also authored a book, Automatic Control Engineering, Wiley India in the year 2015. She can be contacted at email: aditigupta@pu.ac.in.