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DSP implementation and discretization of phase locked loop methods in presence of grid imperfections

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ABSTRACT

The fluctuation of grid variables affects the performance of the phase-locked loop, considerably reducing the efficiency of grid energy injection or compensation currents generation during active filtering. The phase locked loop is the main tool for grid synchronization, offering continuous, real-time extraction of grid variables. As these techniques are implemented on digital computers, their discretization and analysis of resource requirements is an important step. This work represents a discretization and implementation on a digital signal processing (DSP) board of two distinct phase-locked loop (PLL) techniques as well as a comparative study of the latter. Our study covers various aspects, including the discretization of the PLLs to be studied, an assessment of the hardware resources required, their implementation on a DSP board, and their effectiveness in quickly identifying grid variables in the presence of imbalance and harmonics, which represent the most frequent grid imperfections.

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1. INTRODUCTION

An increasing number of power converters are currently being incorporated into the electrical grid as part of distributed generation systems [1]-[4] or active power filtering applications [5], [6]. Given the need for synchronization with the grid with the power converters [7], it becomes imperative to extract phase, amplitude and frequency of the grid voltage in order to control them properly as shown in Figure 1. In the field of grid synchronization, a multitude of approaches has been studied to meet various application requirements. Methods such as "zero crossing detection" and "discrete Fourier transform" have received considerable attention in the literature. The first is based on monitoring the points at which the grid voltage crosses the zero-amplitude axis, thus providing a fundamental indicator for synchronization, one of its primary advantages lies in its simplicity of implementation, but its accuracy can be sensitive to noise and non-ideal grid conditions. In parallel, to accurately detect zero crossings, a sufficiently high sampling rate is required. This can lead to increased resource requirements, resulting in an estimated time up to 300 ms [8]. Synchronization based on the discrete fourier transform (DFT) analyzes signals in the frequency domain, which has the advantage of being able to process signals with variable frequencies. On the other hand, its performance can be influenced by non-ideal grid conditions. In addition, the computational complexity of the discrete Fourier transform can introduce latency and resource requirements [9], resulting in an estimated time up to 185 ms [10], impacting real-time applications, which led researchers to develop other synchronization methods to overcome these problems. In

this context, the phase-locked loop (PLL) is employed to continuously and instantaneously extract the grid variables in the presence of the latter's imperfections.

Several phase-locked loop (PLL) structures are proposed in the literature [11]-[15]. The synchronous reference frame PLL (SRF-PLL), is designed using the Park transform, and is one of the first synchronization techniques introduced. It is simple to implement, and produces good results under disturbance-free grid conditions. However, when grid faults occur, this method gives less accurate results. Numerous studies have concentrated on enhancing its ability to reject disturbances. One study has introduced a decoupled double synchronous reference frame (DDSRF-PLL) architecture [16] that relies on decoupling cells to overcome the impact of grid imbalance. However, the PLLs efficiency are reduced by imperfections of grid (voltage sags [17], imbalance [18], [19], phase jump [20], frequency variations, and harmonics [21]). Hence the need for a PLL structure that ensures fast, accurate synchronization and detection of variations of grid variables. In the other hand, the various PLL structures are generally implemented on digital computers, which makes their discretization and the analysis of the hardware resources required for their implementation indispensable.

The objective of this research is to perform a discretization and an implementation of the SRF-PLL and the advanced DDSRF-PLL technique on a processor, as well as a comparative study between the latter in terms of the hardware resources required, and their speed of detection of grid parameters. The implemented PLLs will be tested in the next experimental step, which aims to evaluate PLL's performances in real-life scenarios, in the context of active power filtering and power injection into the electrical grid. These tests are a crucial step in guaranteeing the practical effectiveness of the PLLs implemented, for future deployment in diverse power system applications. This paper is divided into three sections: i) The first section presents the discretization step of the two PLL methods to be studied; ii) The second section deals with the part relating to the implementation of the techniques studied on a DSP board and the discussion of the test results obtained; and iii) The third and the final section is a conclusion summarizing the developed work.

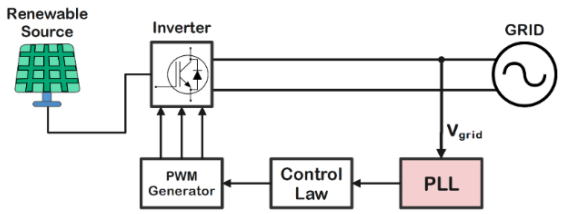

Figure 1. Overview of the studied system architecture

2. METHODS

The various PLL methods to be studied need to be discretized and implemented on a processor [22]. This discretization is typically accomplished through various methods, including the forward Euler method, the backward Euler method, and the trapezoidal method [23]. Both Euler methods produce a 2ω ripple in the estimated amplitude and frequency of the input signal, and influence the performance of the PLL techniques, which is why we have chosen to work with the trapezoidal method [23]. The trapezoidal method requires the transformation described on (1), where « T_s » is the sampling period.

$$s \rightarrow \frac{T_s}{2} \cdot \frac{1-z^{-1}}{1+z^{-1}} \quad (1)$$

2.1. Synchronous rotating frame PLL (SRF-PLL)

The prevalent method for achieving synchronization in three-phase systems is called synchronous reference frame PLL (SRF-PLL) [24]. This approach employs the Park transformation to convert the grid voltage from the conventional abc reference frame into the rotating dq frame, as described in the Figure 2.

In a scenario with ideal voltage conditions, the control of the angular position of the "dq" frame is managed by a feedback control loop, which continually aligns the q component to zero [25]. When an imbalance fault arises [26], [27], the PLL is unable to track the phase angle [25], this is explained by the presence of oscillations at twice the fundamental frequency, induced by the presence of the negative sequence component, resulting in a shift of V_d relative to the positive sequence amplitude $|V^+|$. According to Figure 2, the PI controller and the integrator must be discretized [28] in order to be implemented on the DSP board. The choice of the trapezoidal method leads to the difference equations for the PI controller (2) and integrator (3) respectively, K_P and T_i are chosen to adjust the loop's bandwidth and response time.

$$\text{PI controller: } y(n) = y(n-1) + 92{,}11 \times u(n) - 91{,}89 \times u(n-1) \quad (2)$$

$$\text{Integrator: } y(n) = y(n\text{-}1) + 2{,}5\cdot10^{-5} \times (\,u(n) - u(n\text{-}1)) \quad (3)$$

Figure 3 present the digital realization of Figure 3(a) PI controller, and the depiction of Figure 3(b) integrator. Digital realizations help us to evaluate the computation rate required by each PLL method, based on the number of arithmetic components in each element, and which will be discussed later in Table 1.

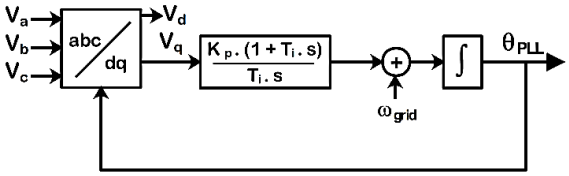

Figure 2. Composition and functional elements of the SRF-PLL structure

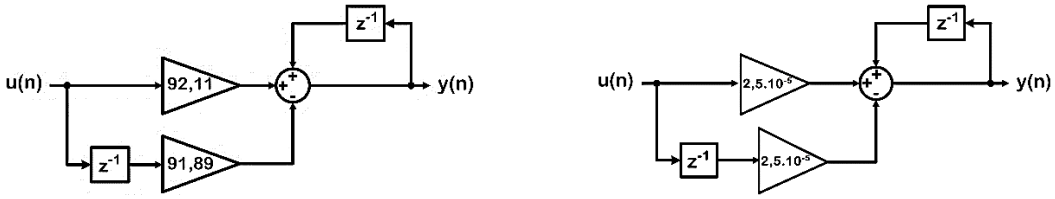

Figure 3. Digital model realizations of (a) the PI controller and (b) the integrator

2.2. Decoupled double synchronous reference frame (DDSRF-PLL)

In the event of grid imbalance, positive and negative sequence components of the grid voltage appear. As these components cannot be controlled independently in the SRF-PLL method, errors occur in the synchronization between the power converter and the grid [29]. The DDSRF-PLL method relies on the independent control of instantaneous symmetrical components sequences of the grid voltage [30], [31].

The DDSRF-PLL lies in the use of two transformations, the first is αβ/ dq^{+1}, where the dq^{+1} frame undergoes positive rotation at an angle "θ_{PLL}", and the αβ/ dq^{-1} transformation, where the dq^{-1} experiences negative rotation at an angle of "$-\theta_{PLL}$". To calculate the positive V^{+1} and negative V^{-1} sequences, we use two decoupling cells, as shown in the Figure 4(a) is the extracts variables from the negative rotating frame, while Figure 4(b) extracts variables from the positive rotating frame. The DC components situated along the dq^{-1} axes are denoted by $\overline{V_d^{-1}}$ and $\overline{V_q^{-1}}$.

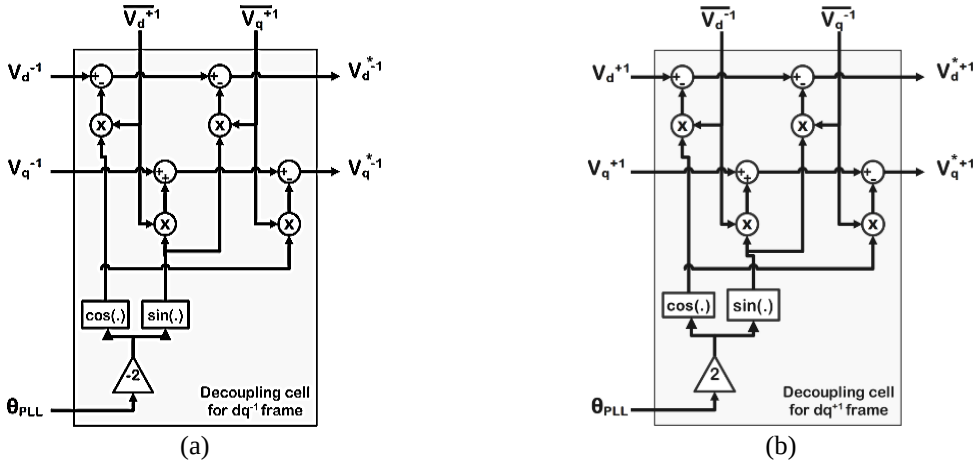

Figure 4. Decoupling cells of (a) dq^{-1} frame and (b) dq^{+1} frame used on a DDSRF-PLL

The signals generated by the decoupling cells « V^*_{d+1}; V^*_{q+1} ; $V^*_{d^{-1}}$; $V^*_{q^{-1}}$ » are nearly continuous terms, serving as valuable information to calculate the amplitude of the grid voltage. To achieve this, these signals undergo further processing by passing through a low-pass filter, to eliminate any residual oscillations present in the estimated voltage vectors as shown in Figure 5. Through the separation of the positive and negative sequences, the DDSRF-PLL provides a satisfactory performance in the case of an unbalanced grid. In the PLL structure illustrated in Figure 5, the four low-pass filters at the output of the decoupling cells must be discretized. The SRF-PLL forces the $V^*_{q^{+1}}$ component to reach zero, for the purpose of determining the positive component of the grid voltage $\overline{V_{d+1}}$. The difference equation of the low pass filter is given by (4) and the digital realization of the output low-pass filter is shown in the Figure 5. The digital realization of the output low-pass filter is shown in the Figure 6.

$$\text{Lowpass filter: } y(n) = 0{,}989 \times y(n\text{-}1) + 5{,}52.10^{-3} \times [u(n)+u(n\text{-}1)] \quad (4)$$

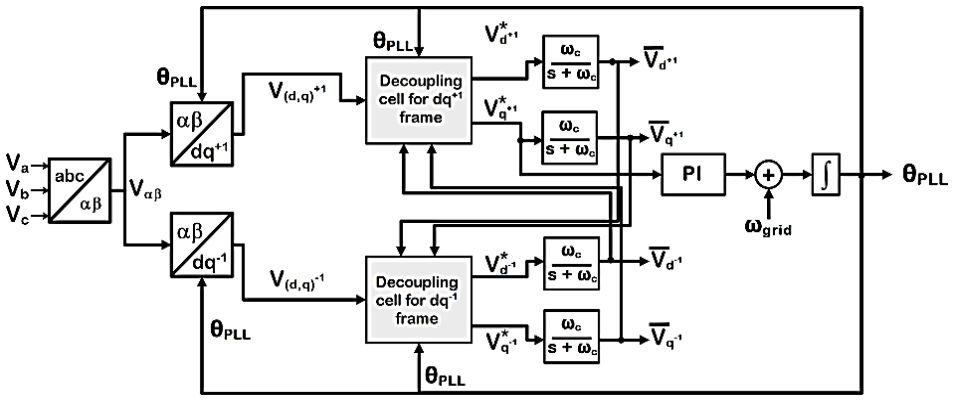

Figure 5. Functional elements of the decoupled double synchronous reference frame PLL

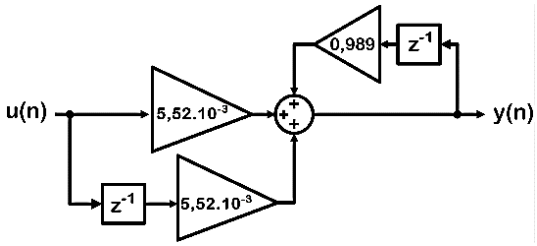

Figure 6. Digital implementation of low-pass filters for output signals refinement

3. DISCUSSIONS OF THE OBTAINED RESULTS

The various PLL methods discussed are tested in two fault scenarios. The first corresponding to a voltage imbalance on a 220 V grid as a positive component, where a negative component of 55 V has been introduced at t=0.16s, shown in Figure 7(a). While the second corresponds to the presence of the rank 5 harmonic of amplitude 55 V, shown in Figure 7(b), in order to see the response of the PLLs in real operating situations.

We have tried to experimentally realize discrete PLL models on a TMS320F28027F DSP in processor in the loop mode, as shown in Figure 8. In this mode, the PLL is implemented on the DSP board, which interacts with the grid voltages on MATLAB/Simulink, in order to validate the PLL's performance in a real operating situation. The generated and implemented program communicates with the grid model via serial communication. This DSP board operates at frequencies up to 60 MHz, offering fast, accurate processing for real-time applications, with a remarkable cycle time of 16.67 ns. The sampling period (Ts) is set at 50µs. In addition, for each control technique, we will evaluate the computation rate [32] required for its implementation, as well as the time required to estimate the results. In the following sections, we will discuss the PLL's response to its output variables (V_d, V_q and the phase angle θ_{PLL}) in presence of grid disturbances.

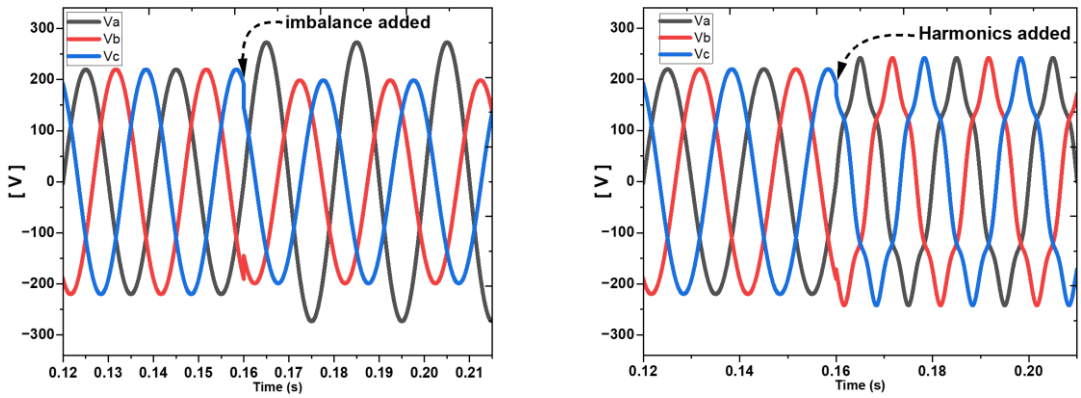

Figure 7. Test scenarios in presence of (a) imbalance and (b) harmonics

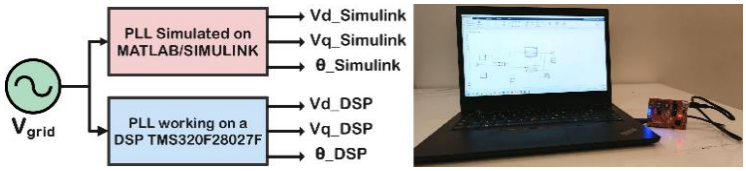

Figure 8. Schematic of the DSP in the Loop method alongside the practical experimental setup

3.1. First scenario: presence of imbalance

In the context of grid imbalance condition, Figures 9(a) and 9(b) serve as illustrative depictions of the output variable Vd for both the SRF-PLL and the DDSRF-PLL, respectively. the response of the PLLs simulated on Simulink are represented by dotted red curves, while those implemented on the DSP board are represented by blue curves. As illustrated, the DSP board provides a response that matches the one simulated on Simulink at the sampling instants.

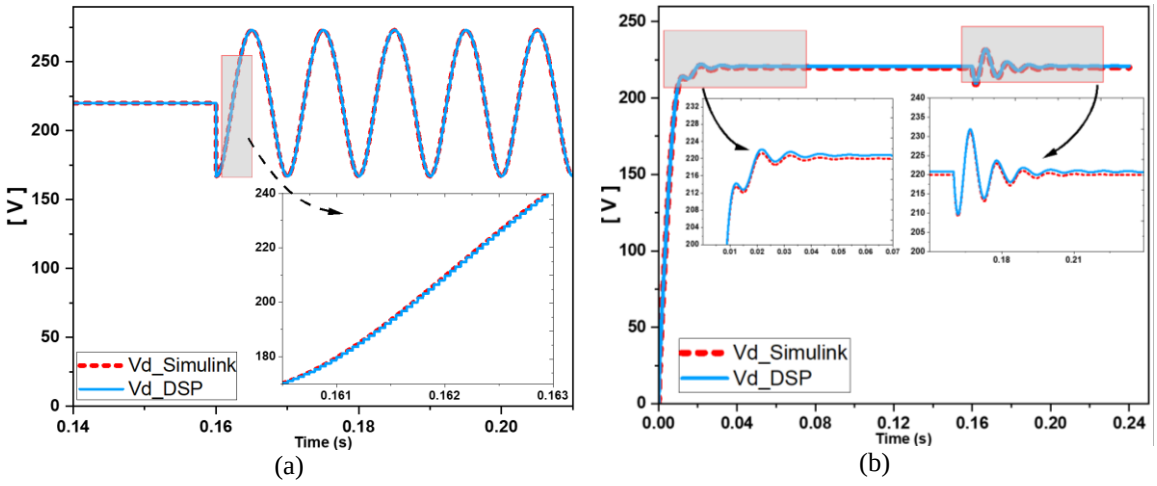

Figure 9. Vd component response of both (a) SRF-PLL and (b) DDSRF-PLL

In the absence of grid imbalance, the Vd component of the SRF-PLL stabilizes at a constant value of 220 V, corresponding to the positive sequence. However, when subjected to grid imbalance, the Vd component oscillates around 220 V. In particular, these oscillations occur with an amplitude of 50 V, corresponding to the amplitude of the negative sequence. In the absence of grid imbalance, the Vd component of the DDSRF-PLL

quickly stabilizes at a value of 220 V within 40 ms, demonstrating its rapid response to ideal operating conditions. When subjected to grid imbalance, the Vd component of the DDSRF-PLL initially oscillates around 220 V. But the presence of the decoupling cells attenuates these oscillations, and the PI corrector forces the Vq component to stabilize at zero as illustrated in Figure 10, resulting in the swift disappearance of the Vd oscillations. This dynamic behavior underlines the efficiency of the decoupling cells, ensuring the resilience and reliability of the DDSRF-PLL under variable operating conditions.

In order to compare the two PLLs in terms of the degree of linearity of the phase angle generated by them, we use the Root-Mean-Square-Error (RMSE) described by (5), where N is the number of samples over a period. Figure 11 provides a representation of the phase angle response for SRF-PLL and DDSRF-PLL. The dotted grey curve marks the evolution of the phase angle of the voltage's positive sequence. In the absence of imbalance, both PLLs show responses that align perfectly with the positive sequence. Once an imbalance is introduced, the SRF-PLL's response deviates from a linear trajectory, with an RMSE of 19%. In contrast, the DDSRF-PLL's response is close to a linear trajectory, with an RMSE of 4.77%. These responses show the DDSRF-PLL's strength to maintain phase alignment under imbalance.

$$\text{RMSE} = \sqrt{\frac{1}{N} \times \sum_{k=1}^{k=N} (\theta_{grid}(k.T_s) - \theta_{PLL}(k.T_s))^2} \quad (5)$$

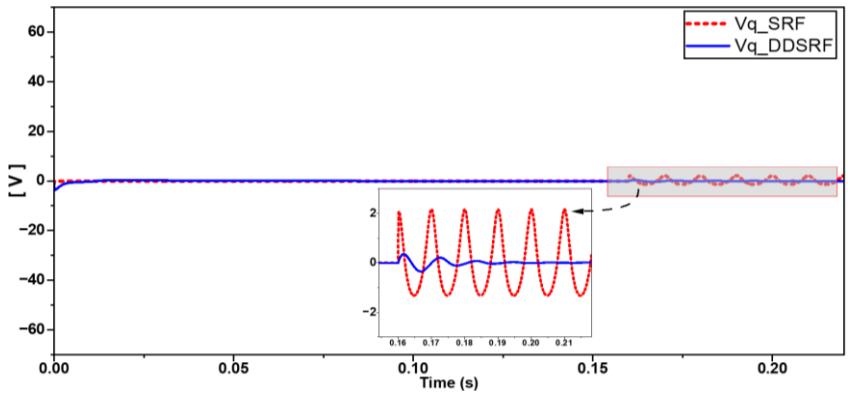

Figure 10. Vq component response of both SRF-PLL and DDSRF

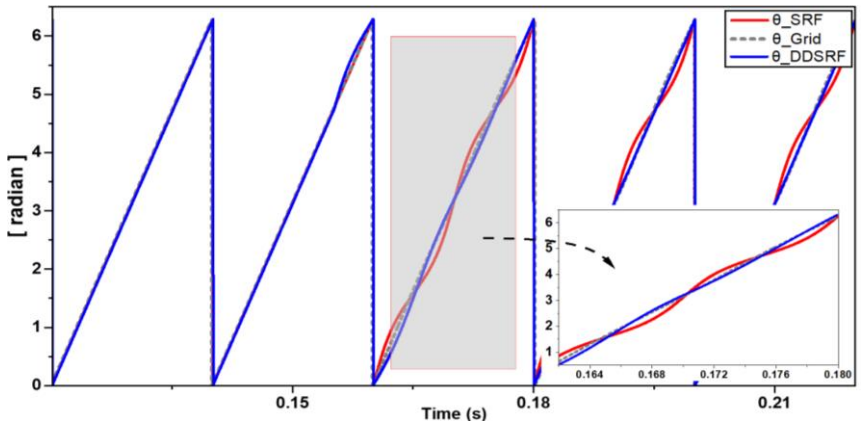

Figure 11. Phase angle response of PLLs in presence of imbalance

3.2. Second scenario: presence of harmonics

Figure 12 gives an overview of the responses of the SRF-PLL and DDSRF-PLL in presence of harmonics, where Figure 12(a) represents the Vd component and Figure 12(b) the phase angle. After the introduction of harmonics, the responses of the two PLLs in Figure 12(a) show oscillations around the positive 220 V component. In particular, the amplitude of oscillations in the response of the SRF-PLL is more pronounced than that of the DDSRF-PLL. A similar observation can be seen in Figure 12(b), where the two PLLs do not precisely follow the phase angle of the positive component.

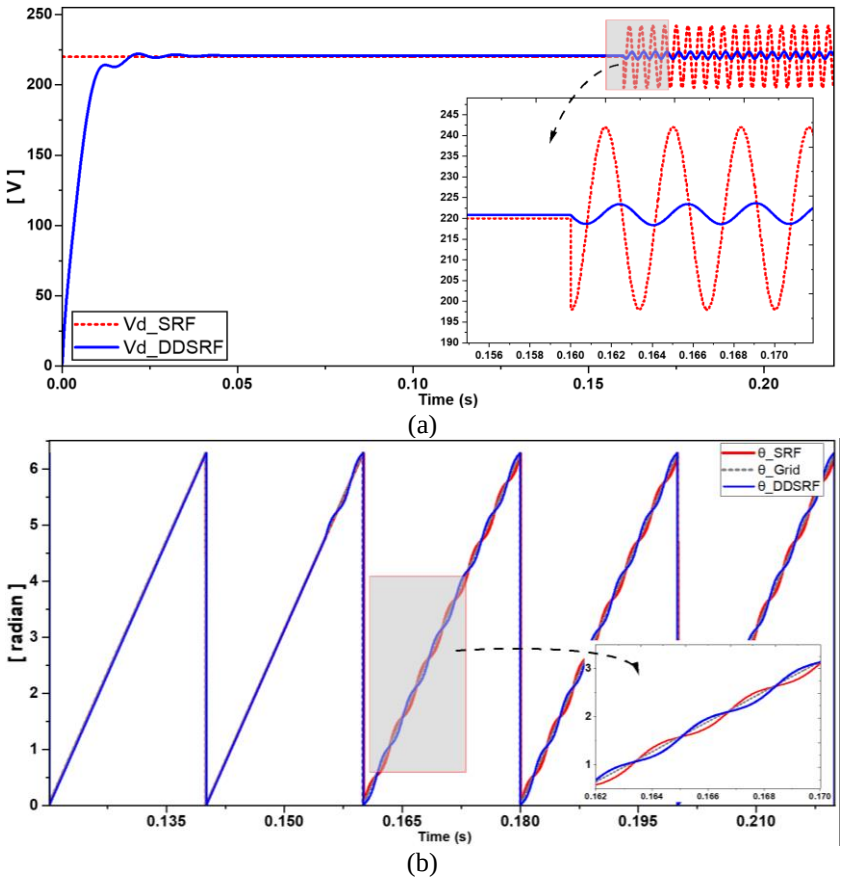

Figure 12. Comparison of component: (a) Vd and (b) phase angle responses of both SRF-PLL and DDSRF-PLL in presence of Harmonics in grid's voltage

3.3. Hardware requirements and computational rate of each PLL method

According to the DSP board's technical documentation, a single cycle time is allocated for the execution of addition operations, whereas multiplication operations require a more complex calculation process, requiring a range of four-cycle times to be completed, which determines the time needed for each PLL structure to provide its results. Table 1 gives an overview of the essential hardware resources for each method, as well as the computing time required to run them.

Table 1 reveals that the SRF-PLL requires fewer resources than its DDSRF counterpart, illustrating the fact that the SRF PLL's execution time is significantly shorter than that of the DDSRF PLL. In addition, the table highlights the strength of the DDSRF PLL in the face of grid's imperfections. In presenting these metrics, Table 1 summarizes the strengths associated with each PLL method, making it easier to select and implement synchronization solutions according to applications requirements.

Table 1. Required resources of the PLL structures and recommended conditions of use

PLL method	Addition	Multiplication	Lookup tables	Computing time	Conditions of use
SRF-PLL	9	10	1 Sine and cosine table	0.81683 µs	Balanced grid
DDSRF-PLL	17	20	1 Sine and cosine table	1.61214 µs	Unbalanced grid + harmonics

4. CONCLUSION

This paper discusses a discretization and an implementation of two PLL techniques « SRF-PLL and DDSRF-PLL » in a DSP board. we have made a comparative study of these PLL techniques from several angles under the most frequent grid operating conditions, and evaluated their hardware resource requirements, the feasibility of implementing them on a processor, and their effectiveness in rapidly detecting grid variables in the presence of imperfections and disturbances. The results of the MATLAB/Simulink simulation match those generated by the DSP board, so the latter will operate satisfactorily in the real-life situation of a grid subject to an imbalance or harmonics faults.

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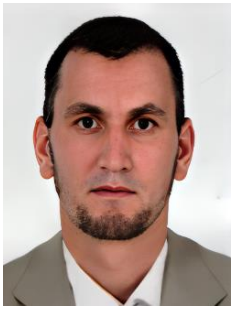

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