International Journal of Power Electronics and Drive Systems (IJPEDS)
Vol. 15, No. 3, September 2024, pp. 1573~1582
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v15.i3.pp1573-1582

A carrier pulse width modulation for asymmetric three-level NPC inverter

Quoc Thai Lam Cuong[1], Nho Van Nguyen[2,3]
[1]Faculty of Electrical and Electronics Engineering, Ton Duc Thang University, Ho Chi Minh City, Vietnam
[2]Faculty of Electrical and Electronics Engineering, Ho Chi Minh City University of Technology, Ho Chi Minh City, Vietnam
[3]Vietnam National University Ho Chi Minh City, Ho Chi Minh City, Vietnam

Article Info

Article history:

Received Nov 7, 2023
Revised Mar 13, 2024
Accepted Mar 21, 2024

Keywords:

Harmonic distortion
Inverter
Offset voltage control
PD carrier PWM
Three-level asymmetrical NPC

ABSTRACT

The three-level neutral point clamped (NPC) inverters are widely used in practice. One of nowadays research trends of multilevel inverter topologies has been reduction of switch number. For this aim, this paper presents an asymmetric three level NPC inverter and study on output performance of phase disposition (PD) carrier pulse width modulation (CBPWM) for different offset voltage functions. A MATLAB/Simulink model of three-level asymmetric NPC inverter is developed to examine the impact of varying the offset voltage on the CBPWM output performances. Total harmonics distortions factors (THD) of voltages and currents are investigated for the whole modulation indices range. The obtained results show that harmonics voltage contents would be advantageous to set in discontinuous pulse width modulation (PWM) methods, particularly at lower voltage range. For asymmetrical topology, simulation results show that switching frequency optimal (SFO)-PWM method has not good performance at low modulation indices and its harmonics content presents an improved at high modulation indices range. Finally, a comparison of the output voltage and current quality via THD index is made between the asymmetric three-level NPC circuit and the conventional three-level NPC circuit are also provided to evaluate the feasibility of the asymmetric three-level NPC inverter in applications.

Corresponding Author:

Nho Van Nguyen
Faculty of Electrical and Electronics Engineering, Ho Chi Minh City University of Technology
268 Ly Thuong Kiet, District 10, Ho Chi Minh City, Vietnam
Email: nvnho@hcmut.edu.vn

1. INTRODUCTION

An increasing amount of research is being focused on multi-level converters to improve the quality of output waveforms for various types of renewable energy sources including solar energy [1], [2], photovoltaic [3], [4], wind turbine system [5], [6], and fuel cell [7], [8]. Among these, the three-level inverter is more commonly used due to its inherent advantages such as lower stress, lower total harmonic distortion (THD), better electromagnetic compatibility, and higher quality output waveforms compared to two-level inverters [9], [10], and it offers a lower cost compared to higher-level inverters [11].

Three-level inverter configurations such as neutral point clamped (NPC), cascade H-bridge, and flying capacitor have been widely brought into practical applications [12]. Among them, the NPC inverter is extensively used due to its simple construction, low electromagnetic interference, and considerably high efficiency [13]. A drawback of multilevel topologies is higher cost. One of possible ways to save costs of the multilevel inverter while it retains acceptable output performance is to reduce number of components. Methods for reducing the number of components applied to asymmetric multi-level NPCs are primarily researched based

on their source and are divided into four types: symmetric, asymmetric, hybrid, and single [14]. Darmian and Barakati [15] has proposed an asymmetric multilevel inverter composed of a cascade connection of units, which has a lower total standing voltage, switching loss, and suits low to medium voltage applications. A hybrid asymmetric 9-level inverter consisting of a three-phase three-level integrated gate-commutated thyristor with a two-level insulated-gate bipolar transistor H-bridge in series with each phase is investigated by Veenstra and Rufer [16]. The simulation results demonstrate significant improvements for medium-voltage industrial drives through power balance by varying the common-mode voltage. A new E-type module generating 13 levels with reduced components for an asymmetrical multilevel inverter proposed by Samadaei *et al.* [17] has the ability to generate both positive and negative output voltage without additional circuits. The simulation and experimental results show that the obtained THD of 3.46% and 4.54%, respectively, satisfy the harmonic standards.

This author also proposes a new multilevel inverter topology named square T-type (ST-type) module, which can generate 17 levels with reduced components. This proposal achieves similar effectiveness based on evaluations of simulation and experimental results [18]. An advantageous structure of an asymmetrical multilevel inverter to reduce the count of insulated supplies and improve energetic efficiency has overcome the restriction of high resolution for three-phase applications, and the effectiveness of this structure has been verified through experiments [19]. In traction drive applications, the 27-level asymmetric inverter is focused on utilizing only one power supply. This topology also permits full regenerative braking working as a three-level converter [20]. A novel structure of symmetrical and asymmetrical multilevel inverter using hexagon switch cells has been capable of producing 7/9/11 output levels by utilizing seven controlled switches. The experimental results have shown a significant reduction in voltage stress across the switches [21]. Espinosa *et al.* [22] has presented a new modulation method for asymmetric inverters, featuring an AC output voltage of 13 levels and ensuring unidirectional power flow in every power cell.

This proposal has dedicated a voltage waveform with low dv/dt and THD reduction through power flow and sensitivity analysis [22]. A series connection of fundamental blocks, considered a new topology of multilevel inverter in voltage levels number with minimum switching devices, is proposed by Mokhberdoran and Ajami [23]. Four different operation modes, including 9-level, 25-level, 31-level, and 49-level, are experimented for verification of effectiveness at both high and low frequencies [23]. A virtual space vector PWM for asymmetric T-type NPC three-level inverter has been presented by Doan and Nguyen [24], and good performance and capacitor voltage balance are demonstrated through comparative evaluations between asymmetric T-type, two-level, and three-level inverters by simulation and experimental results. A large number of switching state asymmetric inverters associated with predictive control algorithms are exhibited to reduce processing time. The experiment of the 27-level inverter has achieved fast dynamic responses [25].

This paper presents a study of pulse width modulation (PWM) performance of an asymmetric three-level NPC inverter. The research content investigates an offset based phase disposition (PD) carrier pulse width modulation algorithm to find a suitable coefficient for the offset voltage function, aiming to optimize harmonics contents in output voltages and currents in whole range of modulation indices. This research is divided into several parts: i) In section 2, the asymmetric three-level NPC configuration is presented by replacing a two-level branch into conventional three-level NPC inverter; ii) Then, a carrier pulse width modulation algorithm using the offset voltage is proposed in section 3 in presence of the function of coefficient; iii) A MATLAB/Simulink model is built to evaluate the THD index in section 4 with the aim of demonstrate the effectiveness of proposed control algorithm and discuss suitable parameters for the effective operation of the asymmetric three-level NPC inverter; and iv) Finally, several crucial points from this study are summarized in section 5.

2. THE ASYMMETRICAL THREE-LEVEL NPC INVERTER

The three-level asymmetric NPC circuit has a schematic diagram as in Figure 1 (show in Appendix) and is powered by a DC voltage source U_d. Phase A is configured with 2 power MOSFETs, similar to a conventional three-phase bridge circuit, and is controlled by phase legs (S_A, S'_A). Phase B and phase C are configured with 4 power MOSFETs each, similar to a conventional three-level NPC inverter, and are controlled by phase legs (S_{B_1}, S_{B_2}, S'_{B_1}, S'_{B_2}) and (S_{C_1}, S_{C_2}, S'_{C_1}, S'_{C_2}), respectively. Three-phase loads $R-L$ are connected to the output terminals of the inverter.

3. PROPOSED CARRIER PULSE WIDTH MODULATION

A PD carrier based PWM controlled by an offset voltage is specifically proposed to control the switching state of power MOSFETs gates. To begin with, the limits of the offset voltage, which depend on the three-phase and DC voltage source U_d, are defined for CBPWM as in (1).

$$\begin{cases} V_{O_{max}} = U_d - Max \\ V_{O_{min}} = -Min \end{cases} \quad (1)$$

Where $Max = Max(V_A, V_B, V_C)$; $Min = Min(V_A, V_B, V_C)$; $V_{A,B,C}$ are the reference three-phase voltages.

The offset voltage lying between the upper and lower limits can be expressed as a function of coefficient η, $(0 \leq \eta \leq 1)$ as in (2).

$$\begin{cases} V_O = (1-\eta)V_{O_{min}} + \eta V_{O_{max}} \\ V_{O_{min}} \leq V_O \leq V_{O_{max}} \end{cases} \quad (2)$$

The inverter leg voltages are presented as (3).

$$\begin{cases} V_{AO} = V_A + V_O \\ V_{BO} = V_B + V_O \\ V_{CO} = V_C + V_O \end{cases} \quad (3)$$

The carrier wave of phase A has the same frequency, but its amplitude is two times higher than the PD carrier waves of the other two phases. The relationship between the control voltages calculated as (4) and the three-phase carrier wave is shown in Figures 2(a)-2(c).

$$\begin{cases} V_{dk_A} = \frac{V_{AO}}{U_d/2}; \ (0 \leq V_{dk_A} \leq 2) \\ V_{dk_B} = \frac{V_{BO}}{U_d/2}; \ (0 \leq V_{dk_B} \leq 2) \\ V_{dk_C} = \frac{V_{CO}}{U_d/2}; \ (0 \leq V_{dk_C} \leq 2) \end{cases} \quad (4)$$

Finally, the comparison between the carrier waves and the control voltage generates a signal to turn on and off the power MOSFETs, as shown in Figure 3, where S_{xj} , and S'_{xj} , x=A, B, and C and j=1,2 are complementary output signals, which are deduced from the same comparison but opposite to each other.

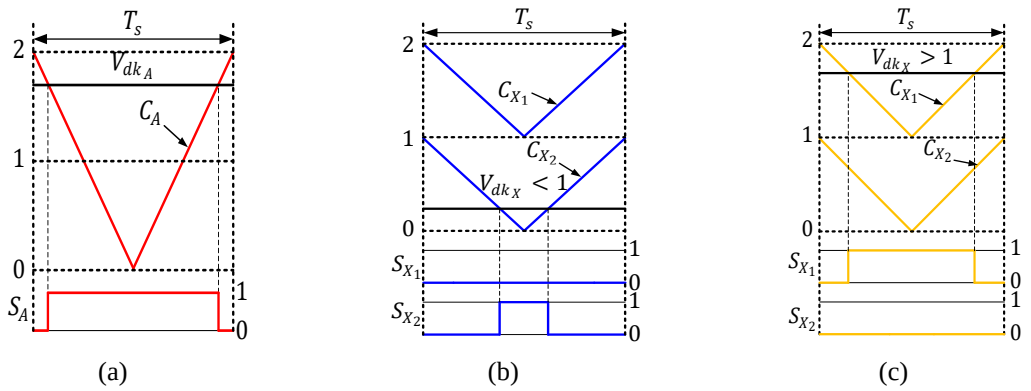


Figure 2. Diagrams of the carrier waves, the control voltages and the switching states: (a) in case of phase A, (b) in case of phases B, C with $V_{dk_X} < 1$, and (c) in case of phases B, C with $V_{dk_X} > 1$, $X = B, C$

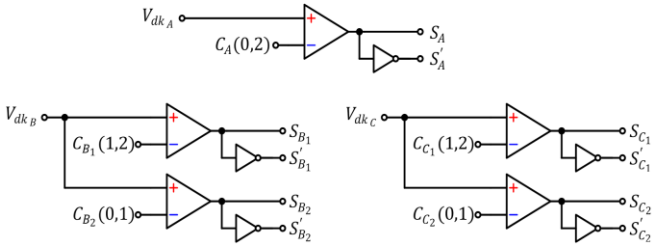


Figure 3. PWM signal generator for the asymmetrical three-level NPC

4. SIMULATION

The MATLAB/Simulink simulation model of the asymmetric three-level inverter circuit, including the power circuit and control circuit, is constructed as shown in Figure 4, with the parameters presented in Table 1. The three-phase input reference voltage has the form of a sine wave, as presented in (5). All simulation results are implemented with values of m ranging from 0 to 1.154 and values of η ranging from 0 to 1, with a step of 0.1.

$$\begin{cases} V_A = m\,V_{base} sin(2\pi f_r t) \\ V_B = m\,V_{base} \sin(2\pi f_r t - 2\pi/3) \\ V_C = m\,V_{base} sin(2\pi f_r t + 2\pi/3) \end{cases} \quad (5)$$

Where $0 \le m = \frac{V_{A,B,C}}{V_{base}} \le 2/\sqrt{3}$ is the modulation index, $V_{base} = U_d/2$ is the base voltage.

Table 1. The simulation parameters

Variables	Values	Variables	Values
Frequency of reference voltage, f_r	60 (Hz)	Sample time, T_s	0.00056 (s)
Frequency of carrier wave, f_c	1800 (Hz)	Mosfet resistance, R_m	0.01 (Ω)
Resistance load, R	1 (Ω)	Diode resistance, R_d	0.001 (Ω)
Inductance load, L	0.01 (H)	DC voltage source, U_d	200 (V)

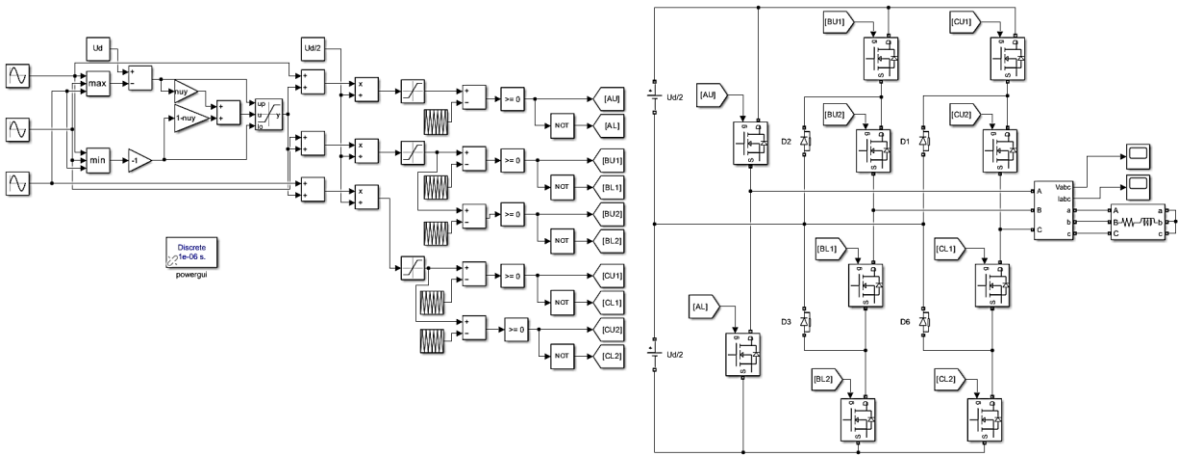


Figure 4. MATLAB/Simulink model of the asymmetrical three-level NPC

Figure 5(a) presents the simulation results of line voltage with $\eta = 0.5$. It is evident that there is a distinction in the voltage waveforms between V_{AB} , V_{BC} , and V_{CA} . Specifically, the line voltage BC is divided into five separate levels, resembling the voltage signal of the conventional three-level NPC circuit, and has a modulated step of 100 (V). Meanwhile, the two voltages V_{AB} , and V_{CA} also feature five levels, but there are several differences as beside modulated steps of 100 V, the voltages endure also larger steps of 200 V: {(0, 200), (-100, 100), (-200, 0)}.

The mentioned analyses are entirely reasonable due to the involvement of the two-level branch inverter leg in phase A. Consequently, the line AB and CA voltages as the outcomes of hybrid two-level and three-level voltage inverter have reduced their quality with an increased harmonics distortion. The line V_{BC} response is similar to corresponding voltage in conventional three-phase three-level NPC inverter, with good harmonics content. If phase load voltages are concerned, the two-level switching of the A-leg causes distorted waveform the most on A-phase, and it also deforms remaining phases B, C at certain level as shown in Figure 5. The phase voltages v_A, v_B, and v_C are also deduced in Figure 5(b). The two-leg topology shows a significant impact on the A-phase voltage, while in the remaining phases B and C, the voltage waveforms are less deformed. In Figure 6, it is demonstrated nearly sinusoidal three phase currents for $m = 1$ and $\eta = 0.5$. The AB current fluctuates at the rising and falling edges of the sinusoidal current waveform with a slight magnitude. The amplitude of the CA current is slightly larger than the other two components, and there is a minor fluctuation at the peak of the sinusoidal current waveform. The BC current exhibits the best performance with minor fluctuations.

In general, the THD of the phase voltage, line voltage, and current becomes worsen while modulation index decreased. The THD_{I_A} in Figure 7(a) is insignificantly lower than THD_{I_B} in Figure 7(b), and both of them are symmetrical with $\eta = 0.5$. At $m \leq 0.4$, the modulation quality tends to decrease, and the peak THD values for phase A and B are 37.5% and 20.3% at $m = 0.1, \eta = 0.5$, respectively. The best current quality is concentrated at $m = 1.154$ and $\eta = 0.5$, about 1.64% and 1.09% for phase THD_{I_A} and THD_{I_B}, respectively.

The influences of m and η on THD of the phase voltage A and B are shown in Figures 8(a) and 8(b), and the peak magnitudes of THD reach about 934% and 546% at $\eta = 0.5, m = 0.1$ for THD_{V_A} and THD_{V_B}, respectively. The optimal THD values occur at $m = 1.154$ and $\eta = 0.5$, with approximately 45.95% and 33% for phase A and B, respectively. Notably, it is evident that the THD of the phase is less dependent on η with $m > 0.4$.

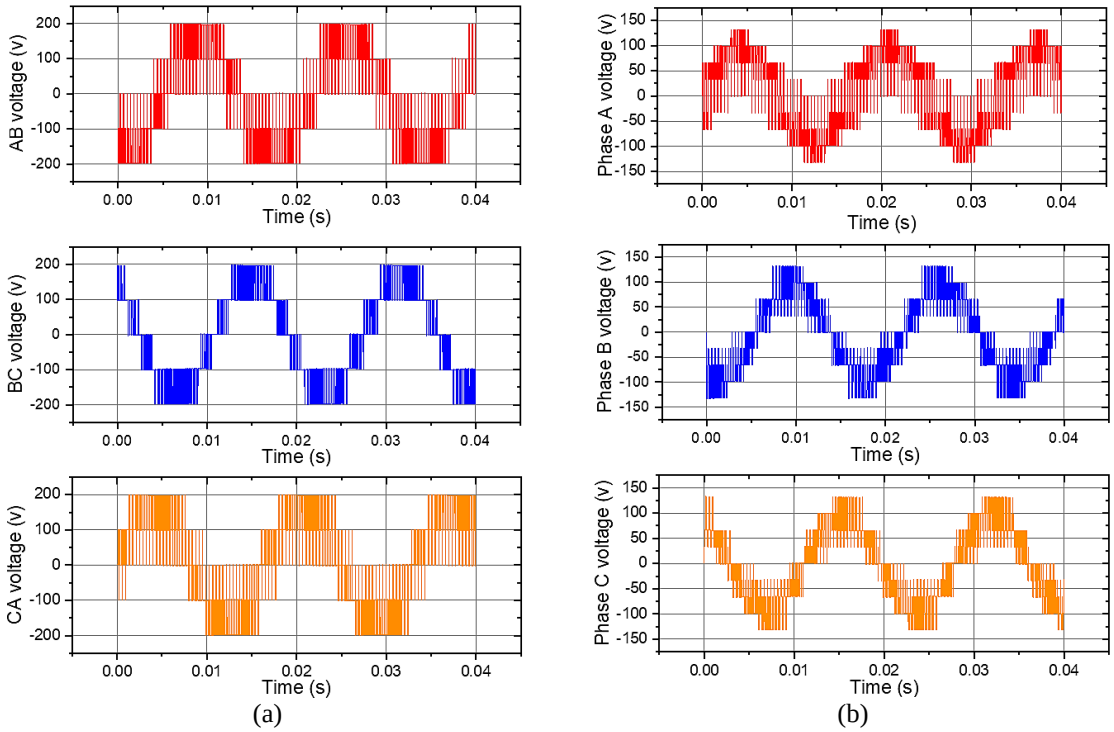


Figure 5. The voltage of the asymmetrical three-level NPC ($\eta = 0.5, m = 1$): (a) the line voltage and (b) the phase voltage

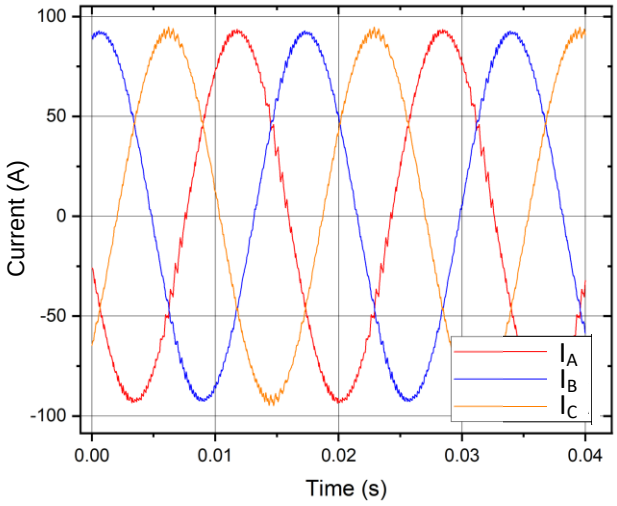
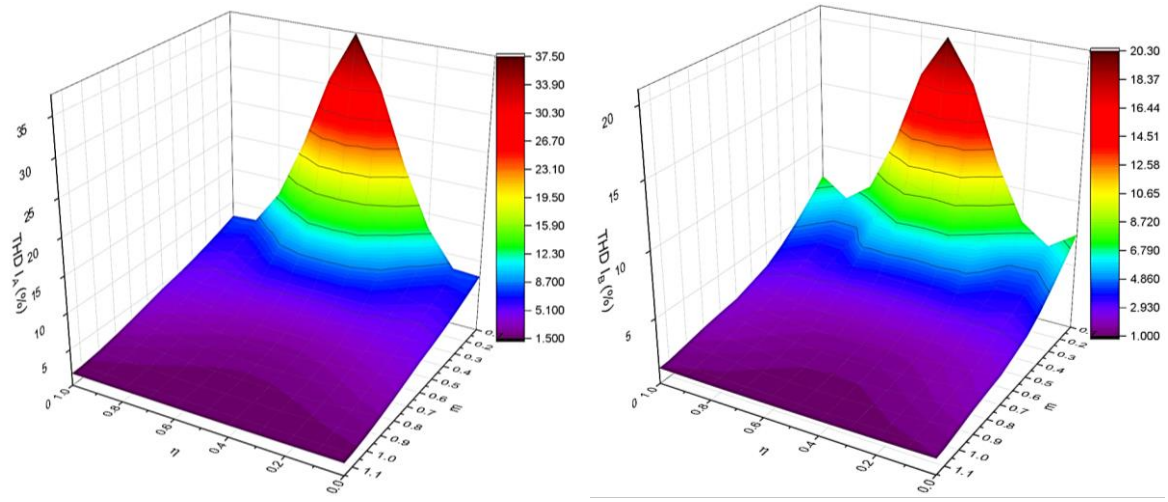
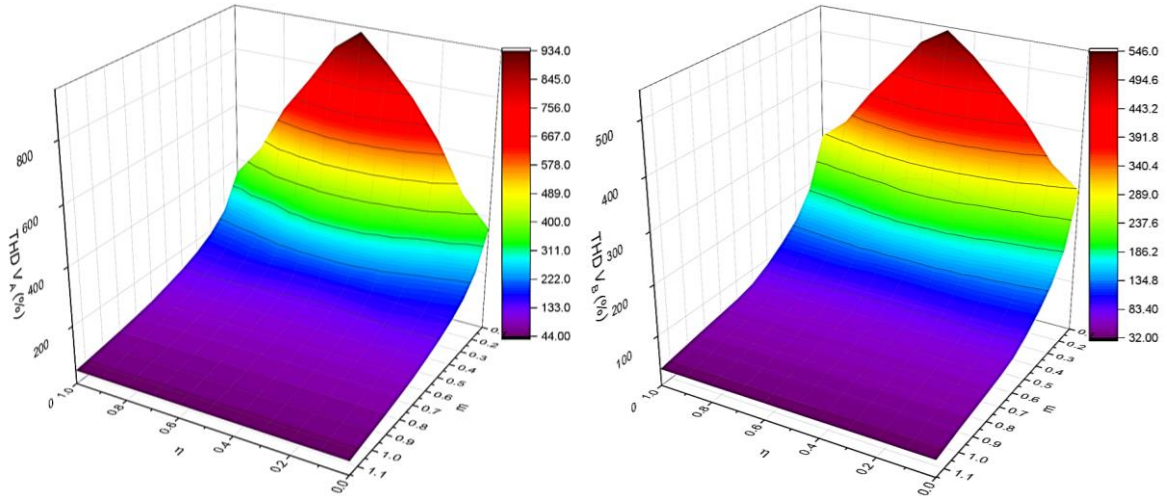


Figure 6. The three-phase current of the asymmetrical three-level NPC ($\eta = 0.5, m = 1$)



(a) (b)

Figure 7. Diagrams of current distortion THDi (m, η): (a) A phase current THD and (b) B phase current distortion



(a) (b)

Figure 8. Diagrams of voltage distortion THDU (m, η): (a) A phase voltage THD and (b) B phase voltage distortion

Similar to the THD of phase voltage, the $THD_{V_{AB}}$ and $THD_{V_{BC}}$ presented in Figures 9(a) and 9(b), respectively, are evenly distributed and do not significantly depend on η with $m > 0.4$. However, there is a substantial difference in the peak THD of the two-line voltages AB and BC, approximately 840% and 281%, respectively. The optimal $THD_{V_{AB}}$ and $THD_{V_{BC}}$ are located at $m = 1.154$, with around 42.19% and 27.31%, respectively.

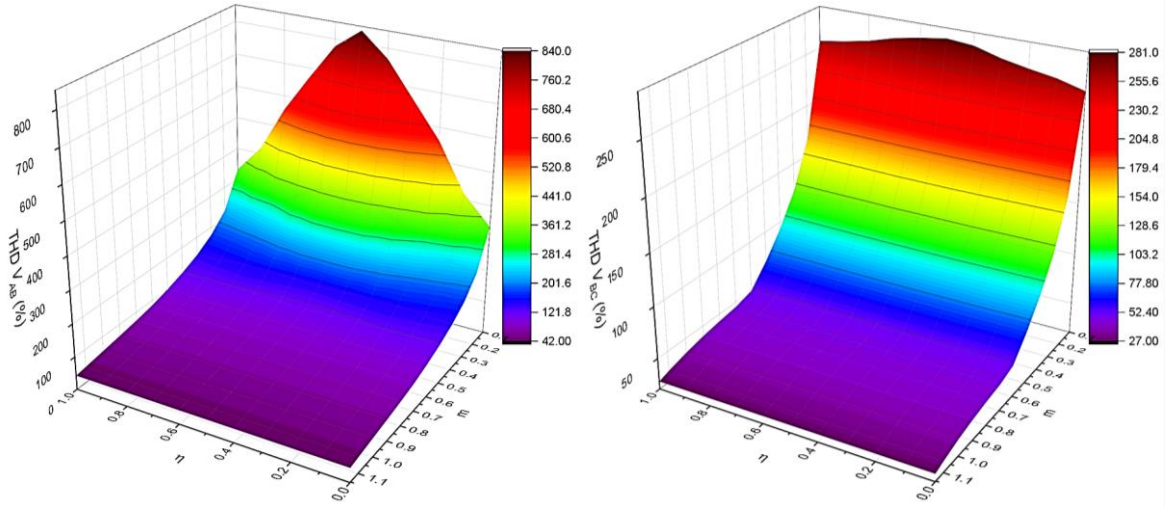
The optimal proportional coefficients, which exhibit best THD quality for asymmetric three-level NPC inverter, is recommended with each modulation index. Due to the inconsistency of THD between phases, it is necessary to calculate the average THD of the asymmetric three-level inverter, which is compared to the THD of the conventional three-level inverter in order to evaluate the effectiveness and the practical application potential of this circuit. The average THD quality of line voltage and current are defined via (6) and (7), respectively.

$$\overline{THD}_V = \sqrt{\frac{THD_{V_{AB}}^2 + THD_{V_{BC}}^2 + THD_{V_{CA}}^2}{3}} \quad (6)$$

$$\overline{THD_I} = \sqrt{\frac{THD_{I_{AB}}^2 + THD_{I_{BC}}^2 + THD_{I_{CA}}^2}{3}} \quad (7)$$

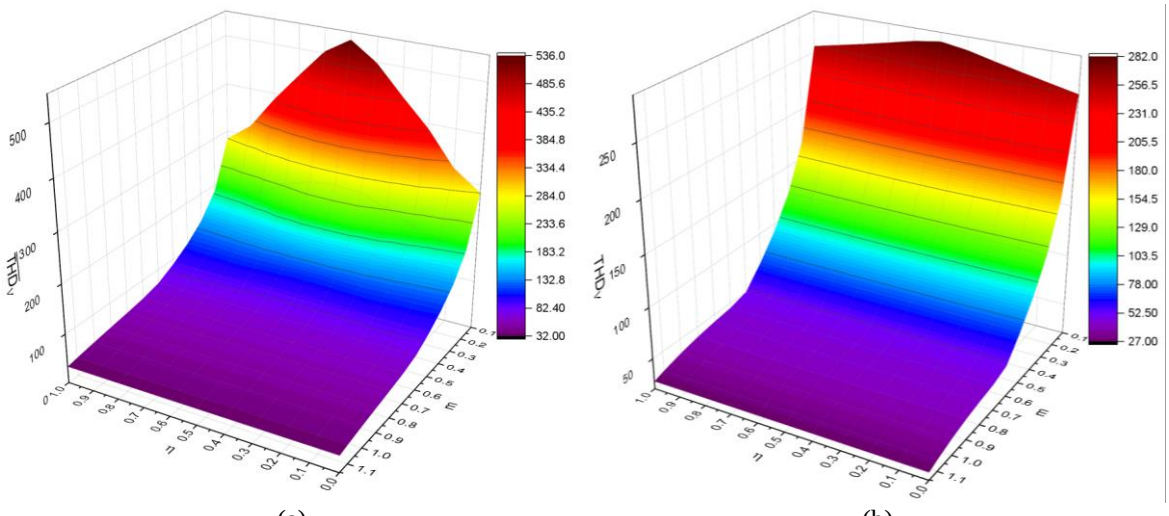
In general, the $\overline{\text{THD}}_\text{V}$ as shown in Figure 10(a) in asymmetric circuits is consistently lower than THD_V in Figure 10(b) of conventional circuits. The best and worst $\overline{\text{THD}}_\text{V}$ of asymmetric circuits are approximately 32.08% at $m = 1.154, \eta = 0$ and 535.25% at $m = 0.1, \eta = 0.5$, respectively. In contrast, the conventional three-level NPC inverter exhibit THD_V with the best and worst qualities being 27.34% at $m = 1.154, \eta = 0$ and 281.56% at $m = 0.1, \eta = 0.5$, respectively. Both types of inverters achieve optimal $\overline{\text{THD}}_\text{V}$ at $m = 1.154$, while the poorest quality is observed at $m = 0.1$ and is distributed symmetrically around $\eta = 0.5$.

Similar to the line voltage, the THD_I shown in Figure 11(a) of the conventional three-level NPC inverter always exhibits better quality than $\overline{\text{THD}}_\text{I}$ of the asymmetric one Figure 11(b). When choosing the proportional coefficient, the asymmetric three-level NPC inverter have to avoid selecting $\eta = 0.2 - 0.8$ at $m \leq 0.4$, as $\overline{\text{THD}}_\text{I}$ increases at these points, with the highest value being 27.24% at $\eta = 0.5, m = 0.1$. Instead, the proportional coefficients $\eta = 0.9$ & 0.1 are recommended, resulting in $\overline{\text{THD}}_\text{I}$ ranging from approximately 3.92% to 6.78% for m values ranging from 0.4 to 0.1. On the other hand, the $\overline{\text{THD}}_\text{I}$ and THD_I have better quality at $\eta = 0.5$ when $m > 0.4$, and the best one is concentrated at $m = 1.154$, with values of about 1.3% and 0.89% for the asymmetric and conventional three-level NPC inverter, respectively.



(a) (b)

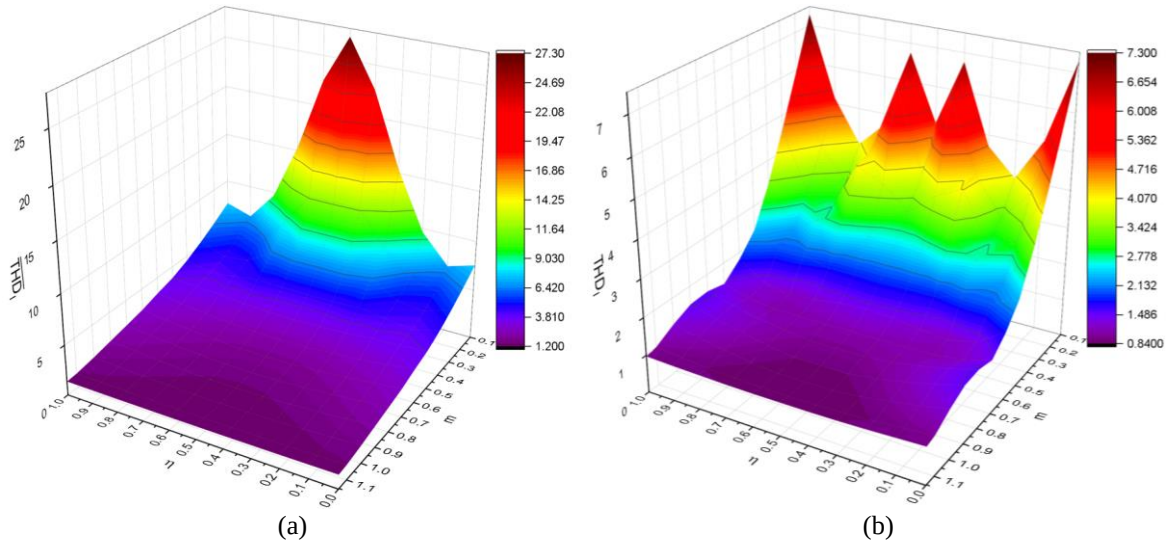
Figure 9. Diagrams of voltage distortion THD (m, η): (a) THD(VAB) and (b) THD(VBC)



(a) (b)

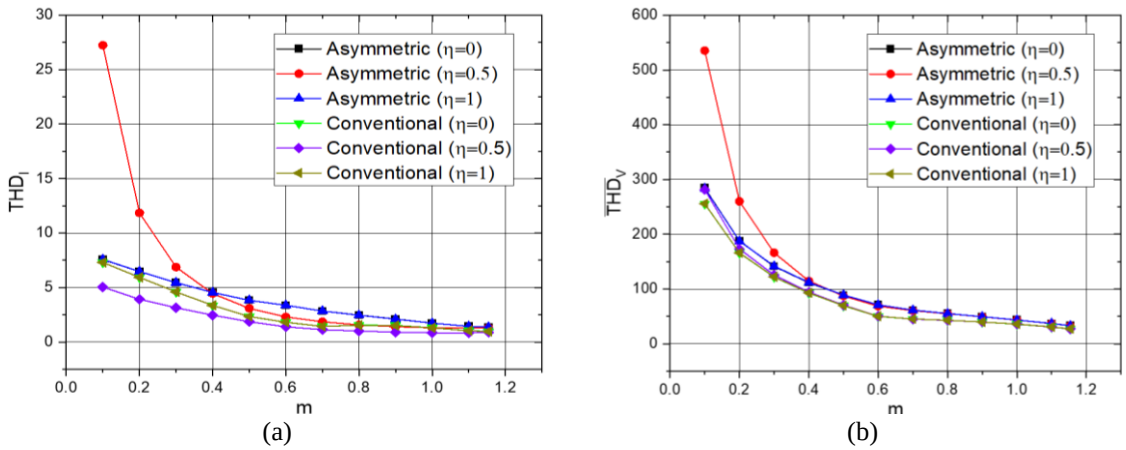
Figure 10. The comparison between (a) the average $\overline{\text{THD}}_\text{V}$ of line voltage in the asymmetric three-level NPC inverter and (b) the THD_V of line voltage in the conventional three-level NPC inverter

The comparisons of THD between the asymmetric and conventional three-level NPC inverter at various values η (0, 0.5, 1) are expressed for the current THD as shown in Figure 12(a) and the line voltage THD as shown in Figure 12(b). The $\overline{\text{THD}}_\text{I}$ and $\overline{\text{THD}}_\text{V}$ for two particular cases with $\eta = 0$ and $= 1$, which correspond to discontinuous pulse width modulation techniques, it can be seen the same and better THD performance than CBPWM with $\eta = 0.5$ (SFO-PWM) when $m \leq 0.4$. Therefore, the discontinuous CBPWM technique using $V_O = V_{O_{max}}$ or $V_O = V_{O_{min}}$ is preferable as an effective strategy for low modulation indices. Figure 12(b) shows that the difference in $\overline{\text{THD}}_\text{V}$ of the asymmetric three-level NPC inverter with three coefficient values $\eta = 0, 0.5, 1$ is insignificant when $m > 0.4$, but there is a larger difference in current $\overline{\text{THD}}_\text{I}$, with best case at $\eta = 0,5$. Therefore, the PWM technique with a medium offset $V_O = (V_{O_{max}} + V_{O_{min}})/2$ is advantageous used when $m > 0.4$. At close maximal modulation index m=1.154, the THD performance between discontinuous PWM $= (0; 1)$, and continuous PWM with $\eta = 0.5$ is negligible, then for lower switching loss, discontinuous PWM can be recommended.



(a) (b)

Figure 11. The comparison between (a) the average $\overline{\text{THD}}_\text{I}$ of current in the asymmetric three-level NPC inverter and (b) the THD_I of current in the conventional three-level NPC inverter



(a) (b)

Figure 12. The THD comparison between the optimal proportional coefficients of the asymmetric and conventional three-level NPC inverter for (a) the average $\overline{\text{THD}}_\text{I}$ of current and (b) the average $\overline{\text{THD}}_\text{V}$ of line voltage

5. CONCLUSION

This paper studies of the influence of offset function in PD carrier-based PWM algorithm for the three-level asymmetric NPC inverter. For given reference voltages, the calculation of average THD of the

asymmetric three-level NPC inverter is implemented with different offset values to evaluate its effectiveness when compared to the THD of the conventional one. Based on investigated results, the offset factor η can be recommended for given reference voltages in order to ensure the quality output of the phase voltages, the line voltages and the currents. Unlike conventional three-level NPC inverter, where SFO-PWM method commonly is advantageous for lower harmonics distortion content, the three-level asymmetric NPC inverter has a poor performance at low modulation index range. In contrary, the discontinuous PWM modes show better output voltage and current quality and they offer perspective solutions. For high modulation indices, SFO-PWM method shows a better performance for having lower current harmonics distortion.

ACKNOWLEDGEMENTS

This research is funded by VNU-HCM under grant number DN2022-20-03. We acknowledge Ho Chi Minh City University of Technology (HCMUT), VNU-HCM for supporting this study.

APPENDIX

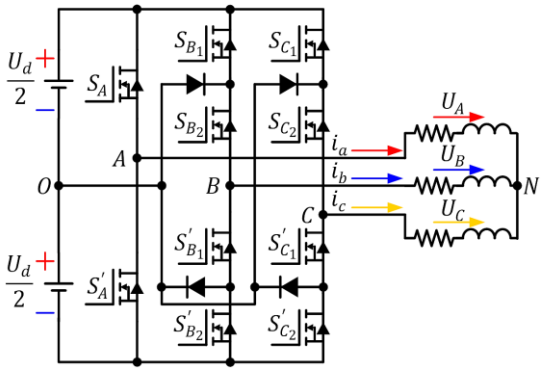


Figure 1. The circuit diagram of asymmetrical three-level NPC

REFERENCES

[1] V. K. Chinnaiyan, J. Jerome, and J. Karpagam, "An experimental investigation on a multilevel inverter for solar energy applications," *International Journal of Electrical Power & Energy Systems*, vol. 47, pp. 157–167, 2013, doi: https://doi.org/10.1016/j.ijepes.2012.10.025.

[2] D. Kumar, R. A. Raj, R. K. Nema, and S. Nema, "A novel higher level symmetrical and asymmetrical multilevel inverter for solar energy environment," *IETE Journal of Research*, vol. 68, no. 5, pp. 3670–3682, Sep. 2022, doi: 10.1080/03772063.2020.1774429.

[3] C. Cecati, F. Ciancetta, and P. Siano, "A multilevel inverter for photovoltaic systems with fuzzy logic control," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 12, pp. 4115–4125, 2010, doi: 10.1109/TIE.2010.2044119.

[4] M. V. Rajkumar, P. S. Manoharan, and A. Ravi, "Simulation and an experimental investigation of SVPWM technique on a multilevel voltage source inverter for photovoltaic systems," *International Journal of Electrical Power & Energy Systems*, vol. 52, pp. 116–131, Nov. 2013, doi: 10.1016/j.ijepes.2013.03.022.

[5] B. Novakovic and A. Nasiri, "Modular multilevel converter for wind energy storage applications," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 8867–8876, Nov. 2017, doi: 10.1109/TIE.2017.2677314.

[6] R. Melicio, V. M. F. Mendes, and J. P. S. Catalao, "Two-level and multilevel converters for wind energy systems: A comparative study," in *2008 13th International Power Electronics and Motion Control Conference*, Sep. 2008, pp. 1682–1687. doi: 10.1109/EPEPEMC.2008.4635509.

[7] R. Seyezhai and B. L. Mathur, "Hybrid multilevel inverter using ISPWM technique for fuel cell applications," *International Journal of Computer Applications*, vol. 9, no. 1, pp. 41–47, Nov. 2010, doi: 10.5120/1347-1817.

[8] C. Dhanamjayulu, S. R. Khasim, S. Padmanaban, G. Arunkumar, J. B. Holm-Nielsen, and F. Blaabjerg, "Design and implementation of multilevel inverters for fuel cell energy conversion system," *IEEE Access*, vol. 8, pp. 183690–183707, 2020, doi: 10.1109/ACCESS.2020.3029153.

[9] K. Thakre, K. B. Mohanty, A. Chatterjee, and V. S. Kommukuri, "A modified circuit for symmetric and asymmetric multilevel inverter with reduced components count," *International Transactions on Electrical Energy Systems*, vol. 29, no. 6, Jun. 2019, doi: 10.1002/2050-7038.12011.

[10] M. R. Baiju, K. K. Mohapatra, R. S. Kanchan, and K. Gopakumar, "A dual two-level inverter scheme with common mode voltage elimination for an induction motor drive," *IEEE Transactions on Power Electronics*, vol. 19, no. 3, pp. 794–805, May 2004, doi: 10.1109/TPEL.2004.826514.

[11] S. Luo, F. Wu, and K. Zhao, "Modified single-carrier multilevel SPWM and online efficiency enhancement for single-phase asymmetrical NPC grid-connected inverter," *IEEE Transactions on Industrial Informatics*, vol. 16, no. 5, pp. 3157–3167, May 2020, doi: 10.1109/TII.2019.2906248.

[12] V. Anand and V. Singh, "Compact symmetrical and asymmetrical multilevel inverter with reduced switches," *International Transactions on Electrical Energy Systems*, vol. 30, no. 8, Aug. 2020, doi: 10.1002/2050-7038.12458.

[13] V. Yaramasu, M. Rivera, M. Narimani, B. Wu, and J. Rodriguez, "High performance operation for a four-leg NPC inverter with two-sample-ahead predictive control strategy," *Electric Power Systems Research*, vol. 123, pp. 31–39, Jun. 2015, doi: 10.1016/j.epsr.2015.01.017.
[14] J. Venkataramanaiah, Y. Suresh, and A. K. Panda, "A review on symmetric, asymmetric, hybrid and single DC sources based multilevel inverter topologies," *Renewable and Sustainable Energy Reviews*, vol. 76, pp. 788–812, Sep. 2017, doi: 10.1016/j.rser.2017.03.066.
[15] S. Y. Darmian and S. M. Barakati, "A new asymmetric multilevel inverter with reduced number of components," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 4, pp. 4333–4342, Dec. 2020, doi: 10.1109/JESTPE.2019.2945757.
[16] M. Veenstra and A. Rufer, "Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives," *IEEE Transactions on Industry Applications*, vol. 41, no. 2, pp. 655–664, Mar. 2005, doi: 10.1109/TIA.2005.844382.
[17] E. Samadaei, S. A. Gholamian, A. Sheikholeslami, and J. Adabi, "An envelope type (E-Type) module: asymmetric multilevel inverters with reduced components," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 11, pp. 7148–7156, Nov. 2016, doi: 10.1109/TIE.2016.2520913.
[18] E. Samadaei, A. Sheikholeslami, S. A. Gholamian, and J. Adabi, "A Square T-Type (ST-Type) module for asymmetrical multilevel inverters," *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 987–996, Feb. 2018, doi: 10.1109/TPEL.2017.2675381.
[19] S. Mariethoz and A. Rufer, "New configurations for the three-phase asymmetrical multilevel inverter," in *Conference Record of the 2004 IEEE Industry Applications Conference, 2004. 39th IAS Annual Meeting.*, 2004, vol. 2, pp. 828–835. doi: 10.1109/IAS.2004.1348509.
[20] J. Dixon, J. Pereda, C. Castillo, and S. Bosch, "Asymmetrical multilevel inverter for traction drives using only one DC supply," *IEEE Transactions on Vehicular Technology*, vol. 59, no. 8, pp. 3736–3743, Oct. 2010, doi: 10.1109/TVT.2010.2057268.
[21] S. P. Gautam, L. K. Sahu, and S. Gupta, "Reduction in number of devices for symmetrical and asymmetrical multilevel inverters," *IET Power Electronics*, vol. 9, no. 4, pp. 698–709, Mar. 2016, doi: 10.1049/iet-pel.2015.0176.
[22] E. E. Espinosa *et al.*, "A new modulation method for a 13-level asymmetric inverter toward minimum THD," *IEEE Transactions on Industry Applications*, vol. 50, no. 3, pp. 1924–1933, May 2014, doi: 10.1109/TIA.2013.2282494.
[23] A. Mokhberdoran and A. Ajami, "Symmetric and asymmetric design and implementation of new cascaded multilevel inverter topology," *IEEE Transactions on Power Electronics*, vol. 29, no. 12, pp. 6712–6724, Dec. 2014, doi: 10.1109/TPEL.2014.2302873.
[24] N. X. Doan and N. Van Nguyen, "Virtual space vector pulse width modulation for asymmetric T-Type neutral point clamped 3-level inverter," *Mathematical Problems in Engineering*, vol. 2021, pp. 1–19, Dec. 2021, doi: 10.1155/2021/1379040.
[25] M. A. Perez, P. Cortes, and J. Rodriguez, "Predictive control algorithm technique for multilevel asymmetric cascaded H-Bridge inverters," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 12, pp. 4354–4361, Dec. 2008, doi: 10.1109/TIE.2008.2006948.

BIOGRAPHIES OF AUTHORS

Quoc Thai Lam Cuong is a lecturer in Electrical and Electronics Engineering Department at the Ton Duc Thang University (TDTU), Vietnam. He received the B.S. degree and the M.S. degree from Mechatronics Engineering, Ho Chi Minh City University of Technology, Ho Chi Minh, Vietnam in 2020 & 2023. Now, he is a PhD student of Ho Chi Minh City University of Technology. His current research interests include control theory, power electronics, motor drives, and robotics. He can be contacted at email: thailamcuongquoc@tdtu.edu.vn.

Nho Van Nguyen was born in Vietnam in 1964. He received the M.S. and Ph.D. degrees in Electrical Engineering from the University of West Bohemia, Plzen, Czech Republic, in 1988 and 1991, respectively. Since 1992, he has been with the Department of Electrical and Electronics Engineering, Ho Chi Minh University of Technology, Vietnam, where he is currently an associate professor. He was with KAIST as a postdoctoral fellow for six months in 2001 and a visiting professor for one year in 2003-2004. His research includes modeling and control of switching power active filters, and PWM techniques for power converters. He can be contacted at email: nvnho@hcmut.edu.vn.