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Buck-boost converter Fed nine level cascaded H-bridge inverter

Shobana Devendiren[1], R. Samuel Rajesh Babu[2], Subbulakshmy Ramamurthi[3]
[1]Department of Electrical Engineering, Panimalar Engineering College, Chennai, India
[2]Department of Electronics and Communication Engineering, Saveetha School of Engineering, Chennai, India
[3]Department of Electrical and Electronics Engineering, SRM Institute of Science and Technology, Ramapuram, Chennai, India

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ABSTRACT

This research investigates on simulation of a traditional cascaded H-bridge (CHB) five-level inverter and proposes a nine-level cascaded H-bridge inverter system. The performance of both five-level and nine-level inverter systems is evaluated by modeling and simulating the open-loop system. According to the simulation results, the nine-level multilevel inverter (MLI) has a lower total harmonic distortion (THD) than the five-level MLI. The work also introduces a boost converter positioned between a photovoltaic power source and the inverter. A nine-level inverter system is utilized to simulate the proposed photovoltaic and battery-based buck-boost converter (BBC). The effectiveness of the proposed inverter is verified through simulation studies under various scenarios. In terms of THD, the comparison of the open-loop systems indicates that the nine-level inverter performs better than the five-level inverter. Additionally, simulations for a battery-based buck-boost converter and photovoltaic system used to verify the effectiveness of the proposed inverter.

Corresponding Author:

Shobana Devendiren
Department of Electrical Engineering, Panimalar Engineering College
Poonamallee, Chennai, Tamil Nadu 600123, India
Email: shobana_d80@yahoo.co.in

1. INTRODUCTION

Multilevel inverters have attracted much interest from academics, industry professionals, and researchers lately. They have been extensively researched and used in medium voltage and high-power energy control applications. When compared to two-level converters with the same rating, multilevel inverters have the advantage of producing switch waveforms with less harmonic distortion. Multilevel inverters are used to reduce the harmonic distortion of the output while maintaining the inverter's output power [1]-[10].

Several multilevel topologies can be used, including cascaded multilevel inverters with independent DC sources, capacitor-clamped (flying capacitor) inverters, and diode inverters. These topologies make use of various strategies to increase voltage levels and eliminate distortion from harmonics in the waveform results [9]-[10]. The development of multilevel inverters has been driven by the need for improved power quality, increased efficiency, and reduced harmonic distortion in power conversion systems. They find applications in areas such as sustainable energy systems, electric vehicles, high voltage transmission systems, and industrial motor drives.

Research efforts in the field of multilevel inverters continue to explore new topologies, advanced modulation strategies, control techniques, and integration with renewable energy sources [11]-[15]. These developments are intended to further the progress of the power electronics field overall by improving the multilevel inverters' overall performance, efficiency, and dependability in a range of applications. The topology of a multilevel converter is highlighted in one such result along with depth information, such as a comparison with the output waveform and total harmonic distortion (THD) values. The development of a proposed 9-levels cascaded H-bridge (CBH) inverter along with a traditional 5-levels CHB inverter model are described in section 2. This paper also compares and analyzes the MATLAB simulation with their outcomes.

2. CONVENTIONAL CASCADED H BRIDGE INVERTER

An auxiliary circuit and an H-bridge attached in series are part of the five-level single-phase cascaded H bridge inverter, as seen in Figure 1. The number of sources and necessary switches are both decreased in this architecture. The preferred output voltage levels can be produced by selectively turning on particular switching combinations. To create the preferred output voltages depending on the stated switch combinations, the switches must be properly configured, as is implied by the information provided. When S_2 and S_5 switches are turned ON, it produces an output voltage of V_{dc}. The switching states of the traditional cascaded H bridge are displayed in Table 1.

An output voltage of $V_{dc}/2$ is produced when both switches S_1 and S_5 are toggled ON. It generates a resultant voltage of 0 whenever switches S_2 and S_4 or switches S_3 and S_5 are set to turn ON. It appears that either set of components can be utilized for the same output voltage level. When the switches S_1 and S_4 are activated, a $-V_{dc}/2$ output voltage is produced. S_4 and S_3 are turned on and producing an output voltage of $-V_{dc}$.

A cascaded multilevel inverter consists of a sequence of H-bridge (single-phase full-bridge) inverter modules connected in series. Its primary function is to produce a specific voltage level by utilizing multiple DC sources, such as batteries or fuel cells. The optimized structure of a single-phase cascaded inverter is depicted in Figure 2, where the AC terminal voltages of each H-bridge are connected in series. Unlike diode-clamped or flying-capacitor inverters, this design does not require voltage-clamping diodes or balancing capacitors. This makes it particularly suitable for constant frequency applications like active front-end rectifiers, reactive power compensation, and active power filters. In these scenarios, a voltage-regulated DC capacitor can serve as the power supply. The circuit configuration includes two CBH, with the load positioned to combine their outputs.

The ratio of the power supply voltage between the auxiliary and primary bridges is 1:3. Multilevel inverters leveraging voltage escalation offer significant advantages in power distribution and switching frequency, facilitating the practical use of these configurations [15]-[20]. The phase output voltage is generated by combining the outputs of two inverter bridges, each designed to produce three distinct voltage levels. The main bridge generates voltages of +3 V_{dc}, 0 V, and -3 V_{dc}, while the auxiliary bridge provides $+V_{dc}$, 0 V, and $-V_{dc}$. The voltage output of each bridge is determined by the configuration of its switches.

When the positive switches are activated, the bridge delivers a positive voltage; when the negative switches are activated, it delivers a negative voltage. For instance, the main bridge produces +3 V_{dc} when switches S1 and S2 are engaged and -3 V_{dc} when switches S3 and S4 are engaged. Similarly, the auxiliary bridge outputs $+V_{dc}$ when switches S5 and S6 are turned on and -Vdc when switches S7 and S8 are turned on. To obtain an output voltage of $+2V_{dc}$, switches S_1, S_2, S_7, and S_8 are activated, combining the positive voltage from the main bridge with the negative voltage from the auxiliary bridge. Conversely, to achieve an output voltage of $-2V_{dc}$, switches S_3, S_4, S_5, and S_6 are engaged, combining the negative voltage from the main bridge with the positive voltage from the auxiliary bridge. This setup allows the inverter to flexibly synthesize various output voltage levels by selectively operating different switch combinations across the main and auxiliary bridges, ensuring versatility in meeting specific voltage needs [21]-[23].

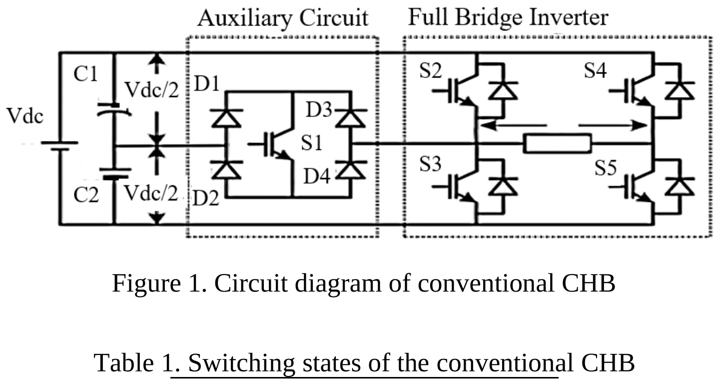

Figure 1. Circuit diagram of conventional CHB

Table 1. Switching states of the conventional CHB

Voltage levels	S_1	S_2	S_3	S_4	S_5
$+V_{dc}$	1	0	0	0	1
$+V_{dc}/2$	0	1	0	0	1
0	0	1	0	1	0
$-V_{dc}/2$	1	0	0	1	0
$-V_{dc}$	0	0	1	1	0

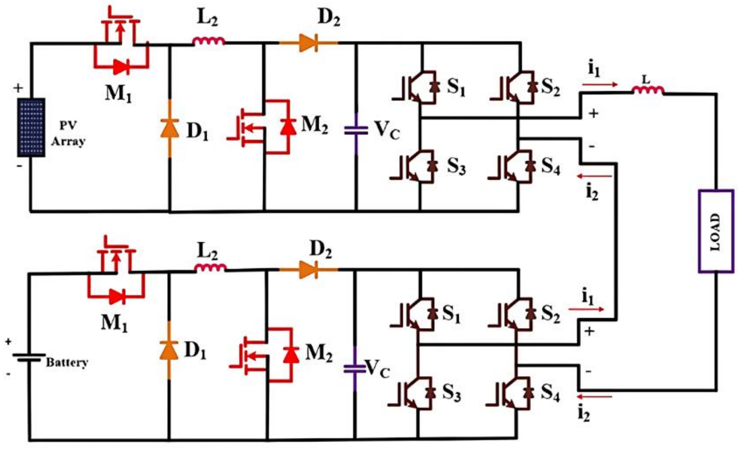

Figure 2. Schematic of the proposed CHB

3. RESULTS AND DISCUSSIONS

Cascaded Multi level inverter's THD is a vital parameter for evaluating voltage and current signal distortion due to harmonics. Pure sine waves have minimal harmonic content, while stepped waveforms show higher distortion [23]-[25]. Ongoing research aims to lower THD values to improve system efficiency, with experiments targeting load conditions that effectively reduce THD levels.

3.1. Simulation results of conventional CHB

The simulation results of a 5-level inverter with an RL load is simulated using MATLAB. Figure 3 displays the voltage cross PV, which has a value of 15 volts. Figure 4 shows the switching pulse for M1, M3, and it has a value of 1 volt. Figure 5 displays the output voltage across the RL load, which is 15 volts. Figure 6 shows the output current of the RL load, which is 0.3 amps. Figure 7 depicts the output current THD, which has a value of 28.25%. Figure 8 depicts the output power, which is 1.9 W.

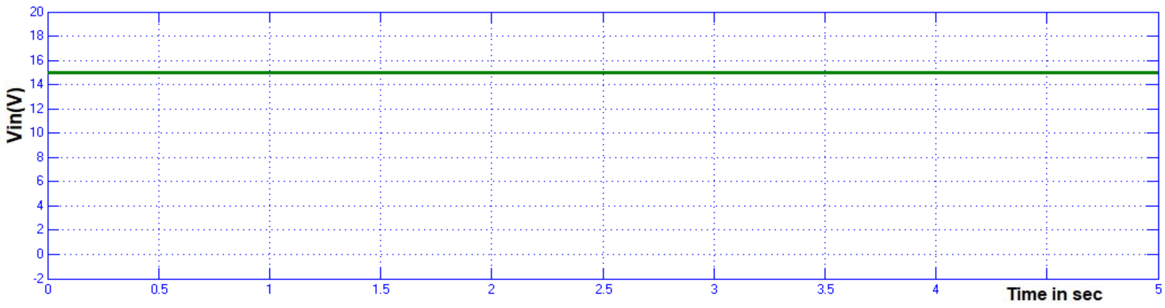

Figure 3. DC voltage throughout PV

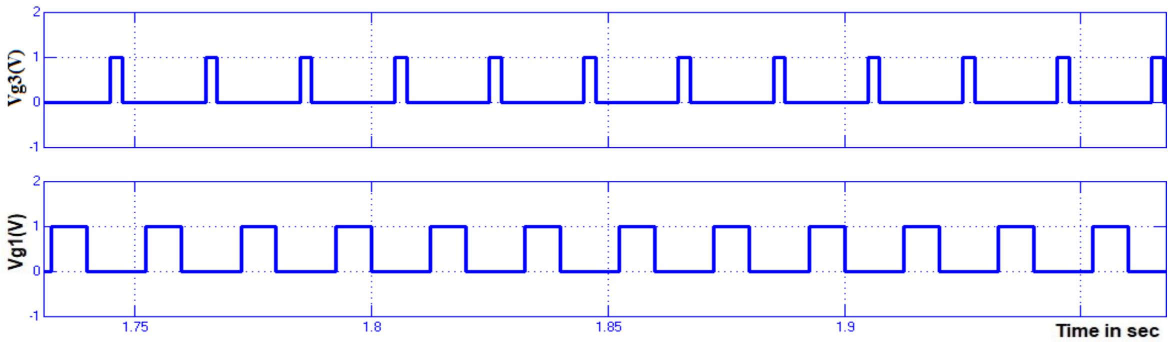

Figure 4. Switching pulses for M1, M3

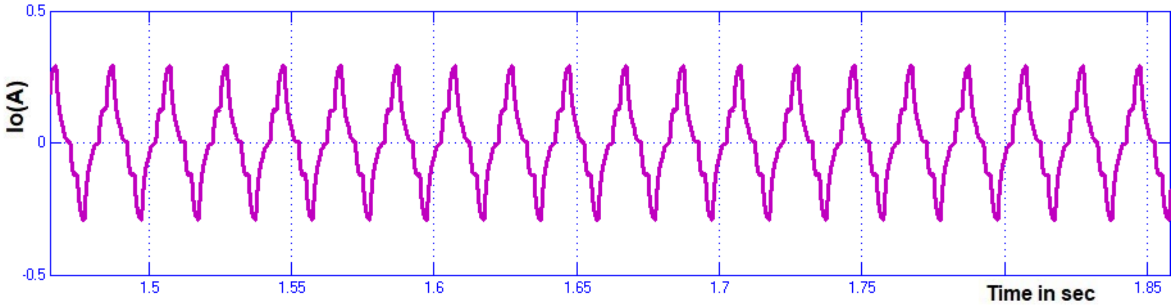

Figure 5. Output voltage across the RL load

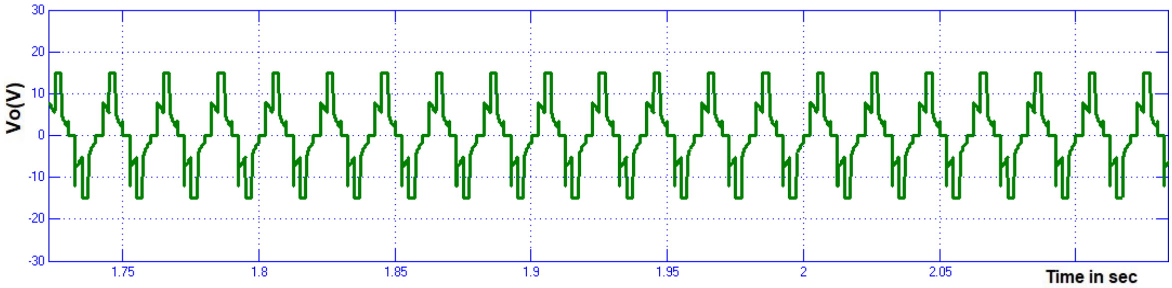

Figure 6. Output current through the RL load

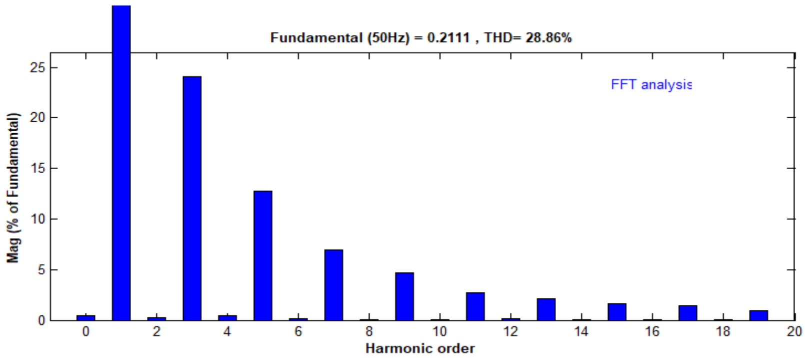

Figure 7. THD of the output current

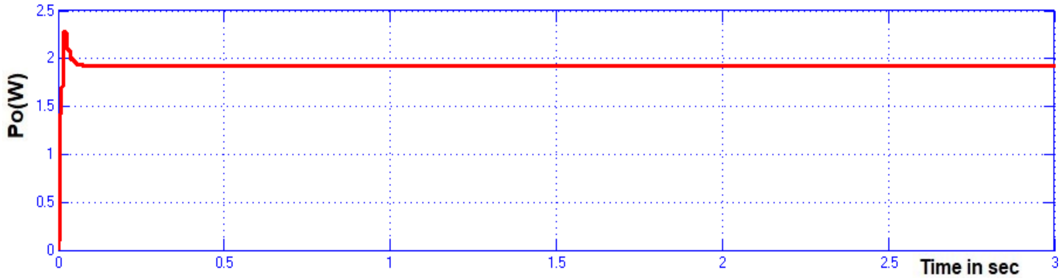

Figure 8. Output power

3.2. Simulation results of the proposed CHB

The simulation results of the proposed buck boost converter Fed CBH 9 level inverter with an RL load are presented in this section. Figure 9 depicts the voltage across the PV, which is 15 volts. This configuration integrates a buck-boost converter to regulate the input voltage for the inverter. The cascaded The H-bridge inverter then converts the regulated voltage into a 9-level output waveform. The RL load is connected to the inverter output, ensuring efficient power delivery. The setup aims to optimize the voltage regulation and waveform quality for the load.

3.2.1. Simulation results of the buck-boost converter section

The simulation results of a buck-boost converter are presented in this section. Figure 10 shows the voltage across buck-boost converter S1, which is 60 volts. Figure 11 shows the switching pulse for the buck-boost converter S1, and its value is 1 volt.

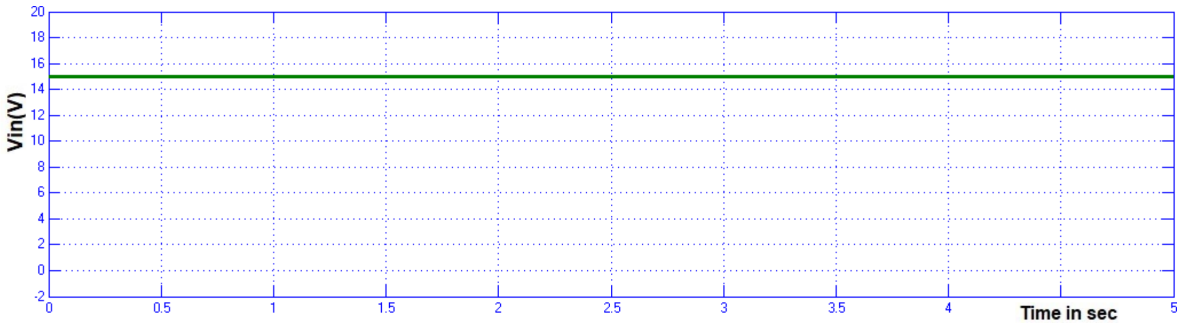

Figure 9. Voltage across PV

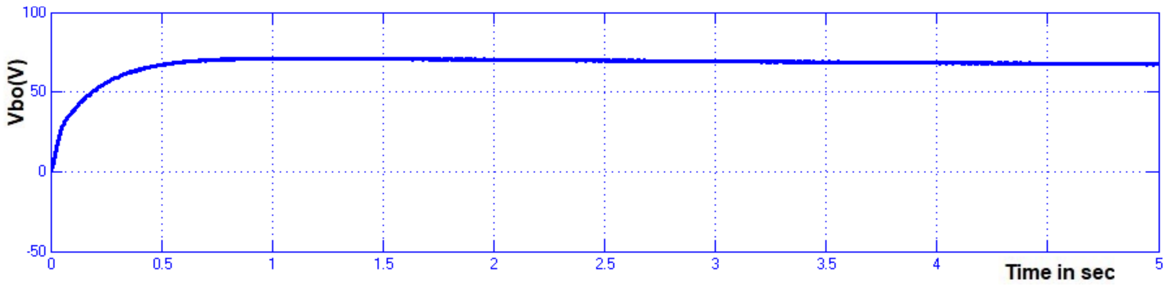

Figure 10. Voltage across buck boost converter

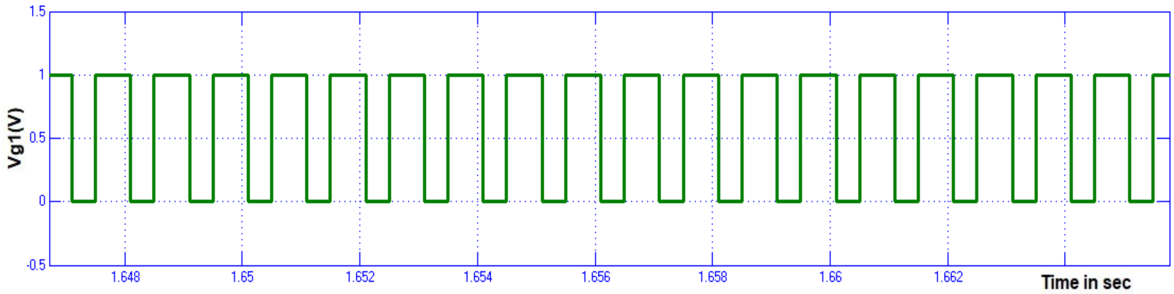

Figure 11. Switching pulse for S_1 in buck boost converter

3.2.2. Simulation results of the cascaded H-bridge inverter section

The simulation results of the 9-level CHB inverter are depicted in Figures 12 to 16. The switching pulses for the inverter's transistors M_1 and M_3 are illustrated in Figure 12, each pulse having a magnitude of 1 V. The voltage across the RL load is presented in Figure 13, showing a value of 60 Volts. Furthermore, the output current flowing through the RL load is displayed in Figure 14, with a magnitude of 0.41 A. The THD of the output current is graphed in Figure 15, demonstrating a value of 7.11%. Finally, the output power is showcased in Figure 16, with a value of 10 W.

Table 2 presents a comparison of output voltage and output power for multilevel inverter (MLI) systems with 5 levels and 9 levels, both with an RL load. In the case of the 9-level MLI system with an RL load, there is a significant improvement observed in both output voltage and output power compared to the 5-level system. Specifically, the output voltage increases from 15 to 60 V, while the output power increases from 1.8 to 10 W. Furthermore, utilizing the 9-level MLI system with an RL load leads to a notable reduction in the THD of the output current. The THD decreases from 28.86% to 7.11%, indicating improved output current quality and reduced distortion levels. Overall, transitioning from a 5-level to a 9-level MLI system with an RL load results in significant enhancements in output voltage, output power, and output current quality, highlighting the advantages of employing higher-level MLI configurations for improved performance in various applications.

Table 2 Comparison of output voltage and output power

MLI	Vo(V)	Po(W)	Output current THD (%)
5-level-RL-load	15	1.8	28.86
9-level-RL-load	60	10	7.11

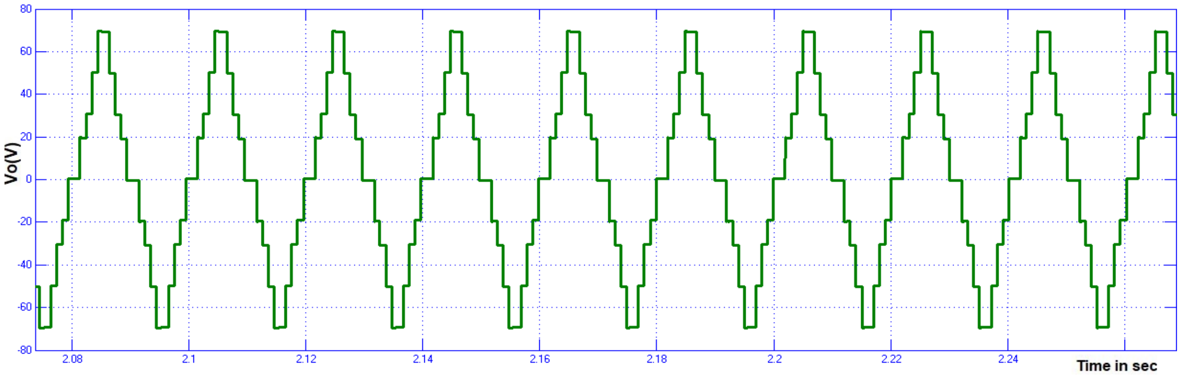

Figure 12. Switching pulse for inverter M1, M3

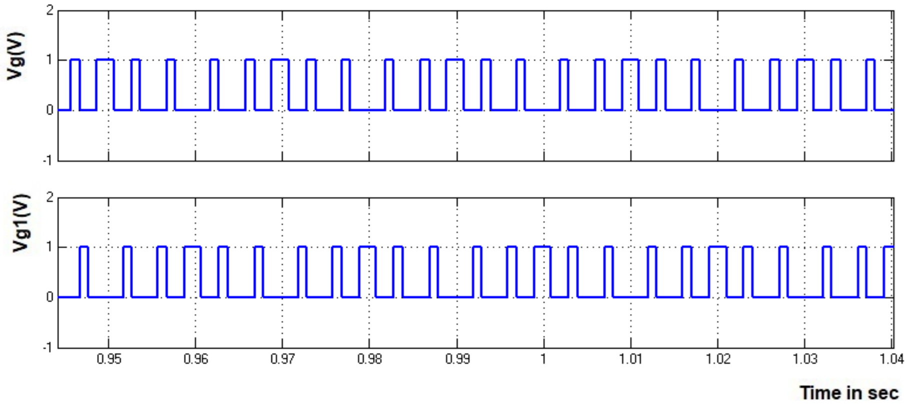

Figure 13. Output voltage across RL load

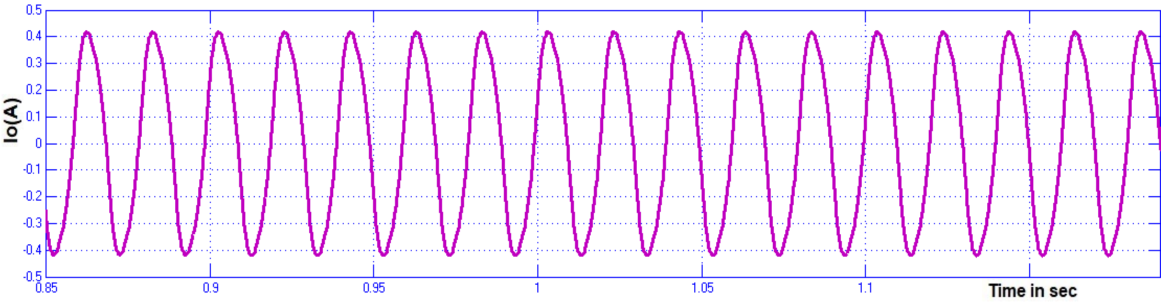

Figure 14. Output current through R load

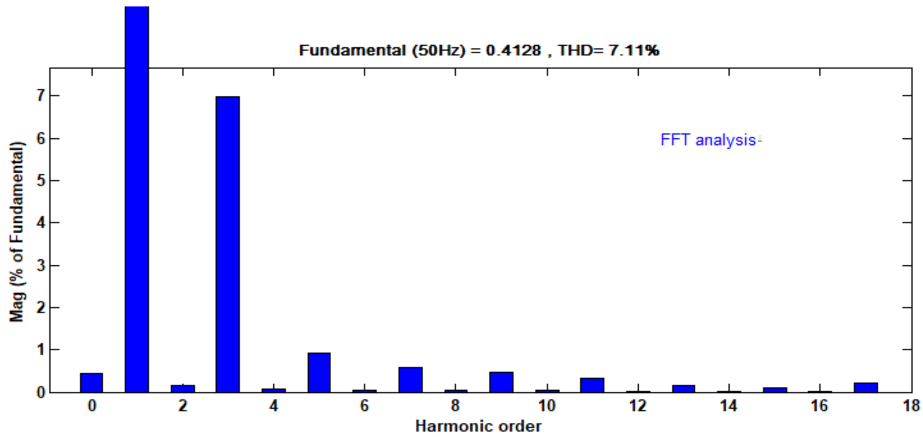

Figure 15. Output current THD

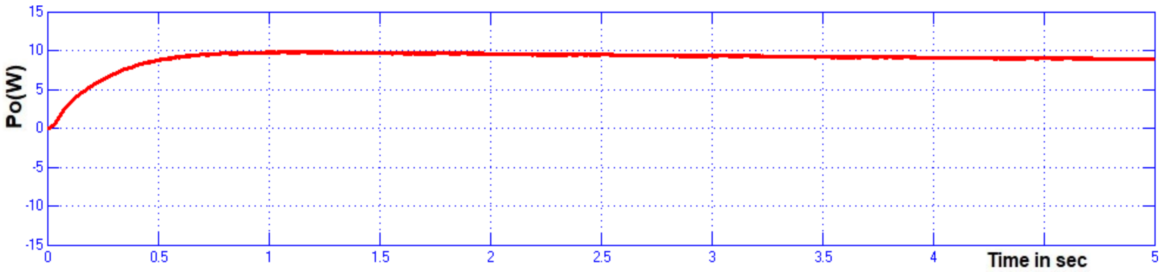

Figure 16. Output power

4. CONCLUSION

A simulation was conducted for a 5-level single-phase inverter system. Another simulation was performed for a single-phase buck-boost converter with a 9-level inverter system. The performance of these systems was compared. A circuit diagram was simulated for a modified H-bridge nine-level inverter system with a source disturbance. The output voltage of the nine-level multilevel Inverter system was improved from 15 to 60 V. Furthermore, the output power increased from 1.8 to 10 W with the implementation of the nine-level MLI system. The THD of the output current was reduced from 28.86% to 7.11%. Notably, the harmonics generated by the nine-level MLI system were found to be lower compared to those produced by the five-level MLI system.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Shobana Devendiren	✓	✓	✓	✓		✓	✓		✓	✓		✓		✓
R. Samuel Rajesh Babu	✓	✓		✓	✓			✓	✓		✓	✓	✓	
Subbulakshmy Ramamurthi	✓	✓	✓	✓		✓		✓	✓	✓	✓			

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper. Authors state no conflict of interest.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author, [SD], upon reasonable request. All simulation results and analysis outputs used in this research are documented within the manuscript. No publicly archived datasets were used or generated specifically for this study. Additional information may be provided to qualified researchers upon request.

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BIOGRAPHIES OF AUTHORS

Shobana Devendiren has obtained her B.E. degree from Madras University in 2003. She has obtained an M.E degree in Power Electronics and Drives from Anna University, Tirunelveli in 2009. Presently, she is doing research work with Sathyabama Institute of Science and Technology, Chennai, Tamil Nadu, India, in the area of power converters. Her area of interest includes the field of power electronics, motor drives, renewable energy, and control system engineering. She can be contacted at email: shobana_d80@yahoo.co.in.

Dr. R. Samuel Rajesh Babu has obtained his B.E. degree from Madras University in 2003. He obtained his M.E degree from Anna University in 2005. He obtained his Ph.D. degree from Sathyabama University in 2013. Presently, he is an Associate Professor in the Department of Electronics and Communication Engineering at Saveetha School of Engineering, Chennai. His areas of interest are power electronics and digital protection. He can be contacted at email: samuel.rajeshbabu@gmail.com.

Subbulakshmy Ramamurthi received her B.E. (EEE) and M.E (PED) from Mailam Engineering College, which is affiliated with Anna University, Chennai, India, in 2007 and 2009. She received her Ph.D. degree from the SRM Institute of Science and Technology, Chennai, India in 2024. She is currently working as an Assistant Professor in the Department of Electrical and Electronics Engineering, SRM Institute of Science and Technology, Ramapuram. Her current research interests include DC converters, multilevel inverters, renewable energy systems, and electric vehicles. She can be contacted at email: subbular2@srmist.edu.in.