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THD analysis of 15-level multilevel inverter using lesser number of switches with nearest level control technique

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ABSTRACT

The multilevel inverters are considered as the efficient power converters. Because of the predominant properties of multilevel inverters over the two-level inverters, these are acquiring more popularity. The aim of research is to minimize the number of switches as well as sources. In this paper, total harmonic distortion (THD) analysis for different modulation indices is carried out for a 15-level inverter with fewer switches. This 15-level inverter uses three asymmetrical sources with nine switching devices. Nearest level control modulation technique provides the pulses for the switching devices at fundamental switching frequency. Evaluation of THD has been carried out in MATLAB/Simulink.

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1. INTRODUCTION

Due to the predominant power quality of the multilevel inverters (MLI) over the conventional two-level inverter, the multilevel inverter topologies have acquired popularity. The output has only two levels in a conventional inverter, which has a heavy distortion from the sine wave. Multilevel inverters are used to produce various levels resulting in the lesser distortion in output that approaches near to sine wave. The applications of the multilevel inverter can be found where there is a need of medium and high power in the electrical engineering fields.

There are some complications in the traditional multilevel inverters like balancing the voltage across the capacitor in flying capacitor type topology, semiconductor switching devices are more in case of neutral point clamped inverter, more number of sources in cascaded H-bridge (CHB) topology [1], [2]. Researches are trying to solve the problems related to the multilevel inverters and are publishing huge number of papers in the past few years. In order to reimburse the downsides of the conventional MLI, new topologies are being introduced. The main focus of the researches is being on reducing the number of switching components, source requirement along with the increase in the number of levels in the output. The designing of the multilevel inverter relays on the number of levels required in the output, number of sources, number of switch requirement. Different topologies were put forward to prevail over the issues of the conventional multilevel inverters [3]-[8].

One such topology suggested is 15-level MLI [4]. This suggested topology uses asymmetrical configuration of the dc voltage sources and it includes features like, using three dc sources, reduction in the number of switches used, study of the total standing voltage, comparison with the other topologies. The topologies from previous studies [9], [10] describe the disadvantages of the conventional CHB. The proposed

topology in study by Samadaei *et al*. [10] produces 17 levels in the output without H-bridge configuration. It uses two T-type arrangements connected back to back. In study by Alishah *et al*. [11] , another topology which is modified H-bridge has been developed using diodes, capacitors, dc voltage sources. The capacitor gets charged to the double of the dc voltage supply and thus various multi levels are obtained at the output.

For high power applications, the multilevel inverter modulation techniques used are many modulation techniques in the literature such as space-vector modulation (SVM), nearest-level control (NLC), sinusoidal pulse width modulation (SPWM) and selective harmonic elimination-pulse width modulation (SHE-PWM) [12]-[17]. The modulation technique called nearest level control comes under the fundamental switching frequency techniques. Nearest level control is also termed as round control method, due to the levels in the output that are selected based on the rounded control method [18], [19]. For high level inverters the modulation technique preferred is the nearest level control but it is not suitable for low level inverters. In nearest level control a stepped waveform is obtained by rounding off a reference sine wave. MLI output is similar to that of rounded off stepped wave. Gate pulses to the switches are obtained in such a way that the output the inverter is same as that of the stepped waveform obtained from rounding off.

In this paper, the analysis of the total harmonic distortion (THD) in the output voltage has been carried out for the topology that has been proposed in previous research [4] with a resistive load of R=100 Ω for different modulation indices and is discussed in the section 4. Section 2 narrates the topology that has been used as a multilevel inverter while the section 3 expresses about the modulation technique that has been used. Section 4 confers about the various results that have been obtained through simulation and section 5 encapsulates the paper.

2. 15-LEVEL INVERTER TOPOLOGY

Three asymmetrical sources and nine switches are used in this topology as seen in Figure 1. The topology [20] uses 12 switches to produce 15-level output whereas ten switches are used in [21] for synthesizing the same output. The 11 switches are used in a novel inverter [22]. This topology uses only nine switches for obtaining 15-levels and hence switches are reduced. One voltage source having a magnitude of V_x whereas V_y is the magnitude of remaining sources. Out of the nine switches, eight switches are unidirectional (T_1-T_8) and one switch is bidirectional (T_9).

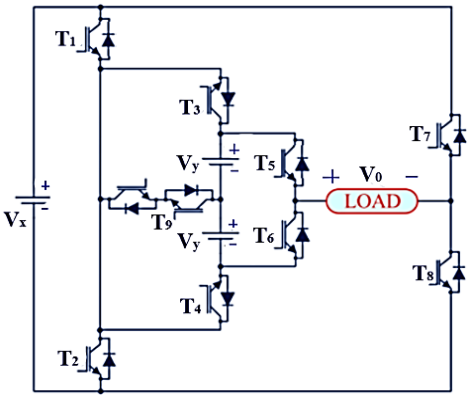


Figure 1. Fifteen-level multilevel topology

V_y sources including switches T_3, T_4, T_5, T_6, and T_9 constitutes the inner part of the topology whereas the outer part comprises of V_x and remaining switches viz. T_1, T_2, T_7 and T_8. The complementary switches are (T_1-T_2), (T_5-T_6), and (T_7-T_8). The magnitudes of the dc voltage sources chosen such that $V_x = V_s$ and $V_y = 3V_s$, making the topology an asymmetrical configuration. For the topology that has been taken, it generates 15 levels in the output voltage. 15-level MLI switching is given in Table 1. The peak output voltage (maximum level) of the inverter is in (1).

$$V_x + 2V_y = 7V_s \quad (1)$$

Total standing voltage in multilevel inverters refers to the cumulative of maximum blocking voltage across switches. By controlling and managing the levels of standing voltage, engineers can optimize the

performance and efficiency of these systems and reduce harmonics in the output. The switches voltage stress is in (2)-(4).

$$V_{T1}, V_{T2}, V_{T7}, V_{T8} = V_x = V_s \quad (2)$$

$$V_{T3}, V_{T4}, V_{T5}, V_{T6}, V_{T9} = 2V_y = 6V_s \quad (3)$$

$$Total\ Standing\ Voltage\ (TSV) = 34V_s \quad (4)$$

Table 1. States for 15-level multilevel inverter

Voltage	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
$+7V_s$	1	0	0	1	1	0	0	1	0
$+6V_s$	0	1	0	1	1	0	0	1	0
$+5V_s$	0	1	0	1	1	0	1	0	0
$+4V_s$	1	0	0	0	1	0	0	1	1
$+3V_s$	0	1	0	0	1	0	0	1	1
$+2V_s$	0	1	0	0	1	0	1	0	1
$+1V_s$	1	0	1	0	1	0	0	1	0
0	1	0	1	0	1	0	1	0	0
$-1V_s$	0	1	0	1	0	1	1	0	0
$-2V_s$	1	0	0	0	0	1	0	1	1
$-3V_s$	1	0	0	0	0	1	1	0	1
$-4V_s$	0	1	0	0	0	1	1	0	1
$-5V_s$	1	0	1	0	0	1	0	1	0
$-6V_s$	1	0	1	0	0	1	1	0	0
$-7V_s$	0	1	1	0	0	1	1	0	0

3. MODULATION TECHNIQUE

The modulation methods with high switching frequency and fundamental switching frequency are discussed in literature [23], [24], [25], [26], [27], [28]. For attaining high power conversion with lesser system cost, fundamental switching frequency would rather be used than high switching frequency. NLC is usually employed in MLI due to easy execution and control. The detailed THD analysis of voltage for a 15-level MLI is carried out at modulation indices of 0.4, 0.6, 0.7, 0.8, 0.9 and 1.0.

NLC modulation aims to select the nearest to the desired output levels at each instant as shown in Figure 2. This technique minimizes the switching losses and harmonic content in the output waveform, leading to improved efficiency and reduced distortion. To achieve the nearest voltage level, control algorithm then decides the switches of the inverter that needs to be turned on or off. Based on the switching decision, the control system generates the appropriate switching signals to control the inverter switches. It is commonly used in various multilevel inverter topologies, to improve their performance and efficiency.

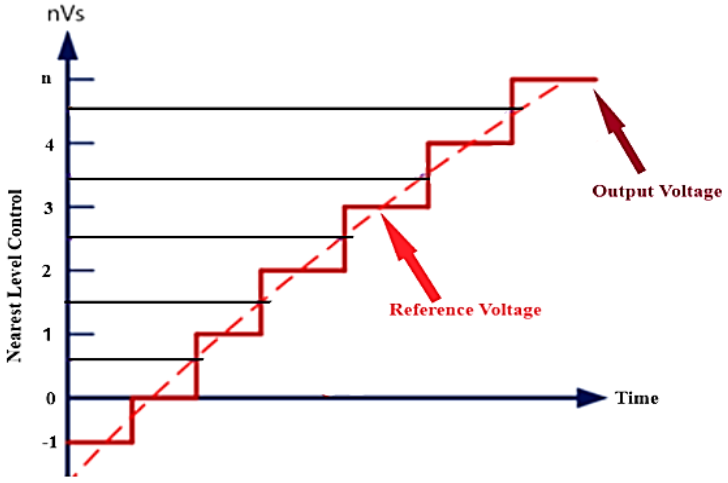


Figure 2. NLC strategy

4. SIMULATION RESULTS

15-level inverter Simulink model is shown in Figure 3, where V_x = 100 V and V_y = 300 V with R-load of 100 Ω. Peak value of output voltage is 700 V. By varying the modulation index, the corresponding outputs are obtained. The 5-levels are attained for a modulation index (m_a) of 0.4 as depicted in Figure 4(a) (see in Appendix). There is an increment of two levels in the output voltage as presented in Figure 4(b) (see in Appendix). The results for m_a of 0.7, 0.8, 0.9 and 1.0 can be seen in Figures 4(c) to 4(f) (see in Appendix).

For the m_a = 0.9, output has 13-levels with THD of 6.15% as shown in Figure 5(a). The THD for 15 level output voltage at m_a = 1.0 is 5.49 % as depicted in Figure 5(b). 0.66 % THD is decreased for m_a = 1.0 when compared to m_a = 0.9. Table 2 summerizes the output THD for different m_a. The comparison of various 15-level inverters is listed in Table 3 [29], [30].

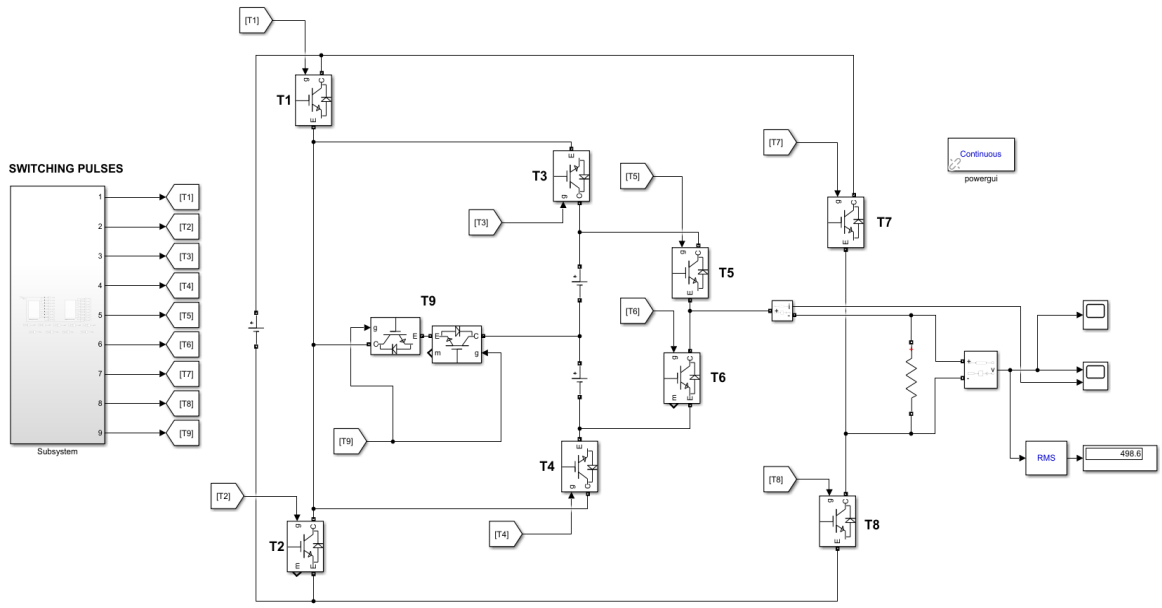
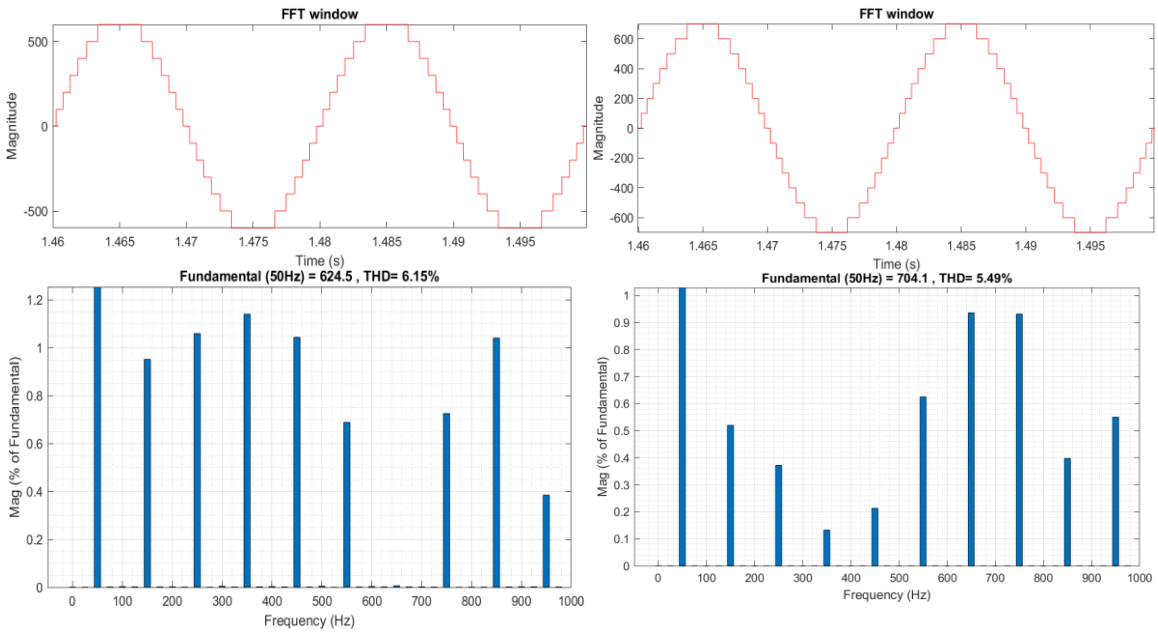


Figure 3. Simulink model of the 15-level topology



(a) (b)

Figure 5. FFT analysis for output voltage at (a) m_a = 0.9 and (b) m_a = 1.0

Table 2. Output voltage THD for different modulation indices

Modulation index	Number of levels in output	THD (%)
0.4	5	16.83
0.6	7	12.08
0.7	9	8.89
0.8	11	7.94
0.9	13	6.15
1.0	15	5.49

Table 3. Comparative analysis for different 15-Level inverter topologies

15-level inverters	Switch count
Conventional cascaded H-bridge	28
Conventional diode clamped asymmetrical inverter	24
Inverter with reduce switch count [29]	11
Hybrid multilevel inverter [30]	10
Inverter with nearest level control	09

This paper evaluates the effectiveness of the nearest level control strategy by comparing it to sinusoidal pulse width modulation techniques from existing literature. The analysis reveals that THD of the output voltage is lower with the nearest level control technique. Table 4 summarizes the comparison of THD for various modulation techniques.

Table 4. THD in output voltage for 15-level inverter with various modulation methods

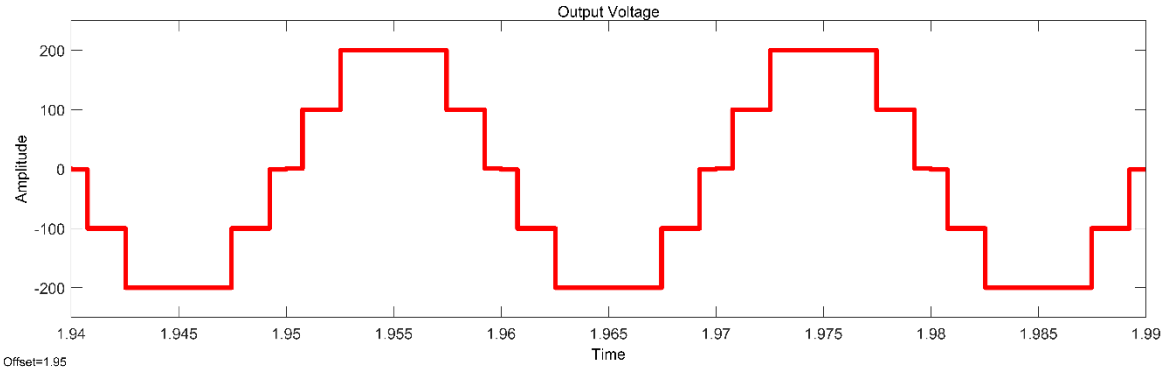
THD (%) of output voltage for 15-level inverter					
SPWM [31]					
PD PWM	APOD PWM	POD PWM	Hybrid PWM	Phase shifted PWM	Nearest level control technique
8.98	9.03	9.42	9.15	9.14	5.49

Note: Phase disposition (PD), alternative phase opposition disposition (APOD), and phase opposition disposition (POD)

5. CONCLUSION

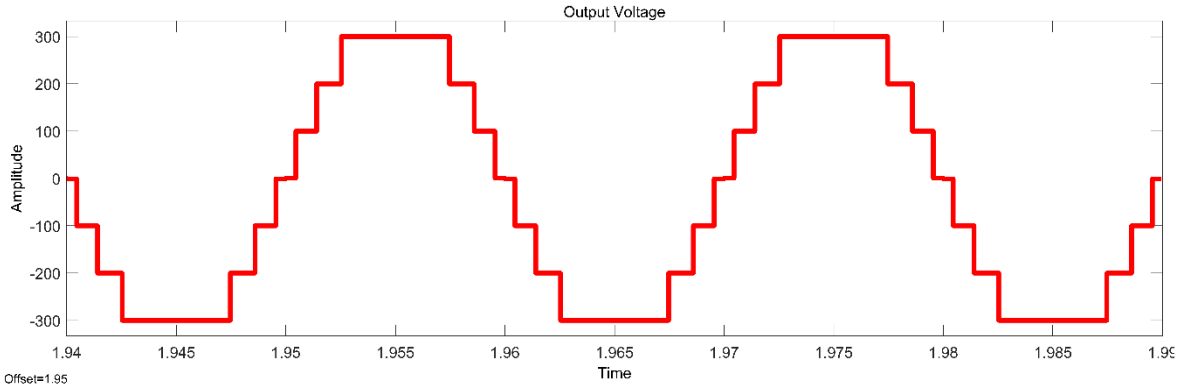
The THD analysis of a 15-level inverter is carried out for various modulation indices with lesser switches. It is found that THD in the voltage for 15-levels in the output is around 5.49% at 50Hz frequency. In case of motor drives, electric vehicles and PV applications, this multilevel inverter has a great significance and better future scope.

APPENDIX

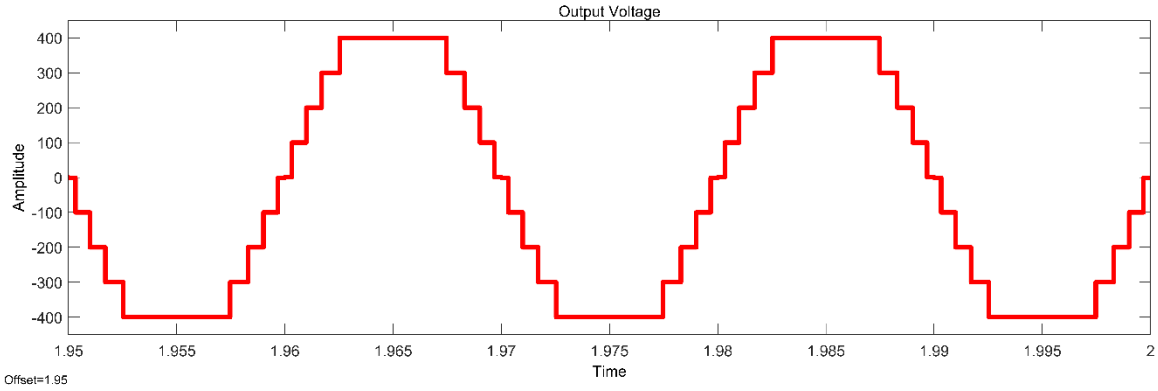


(a)

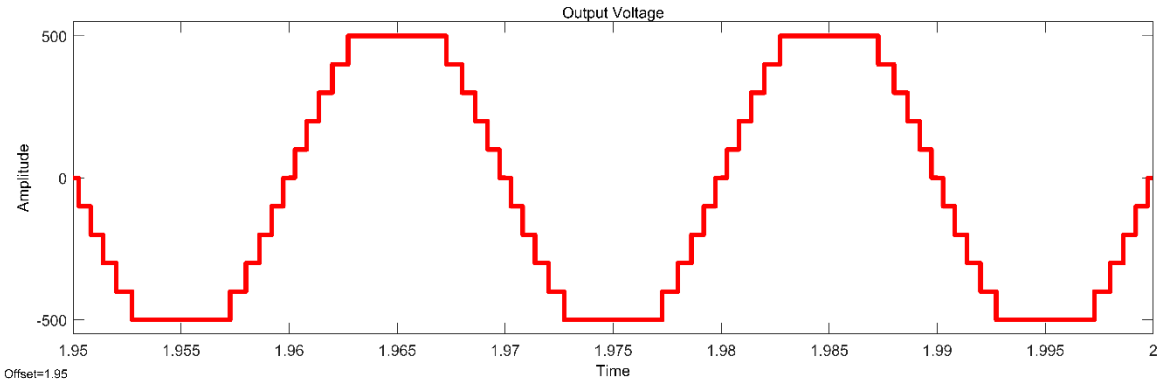
Figure 4. Output voltage for 15-level inverter at (a) $m_a = 0.4$



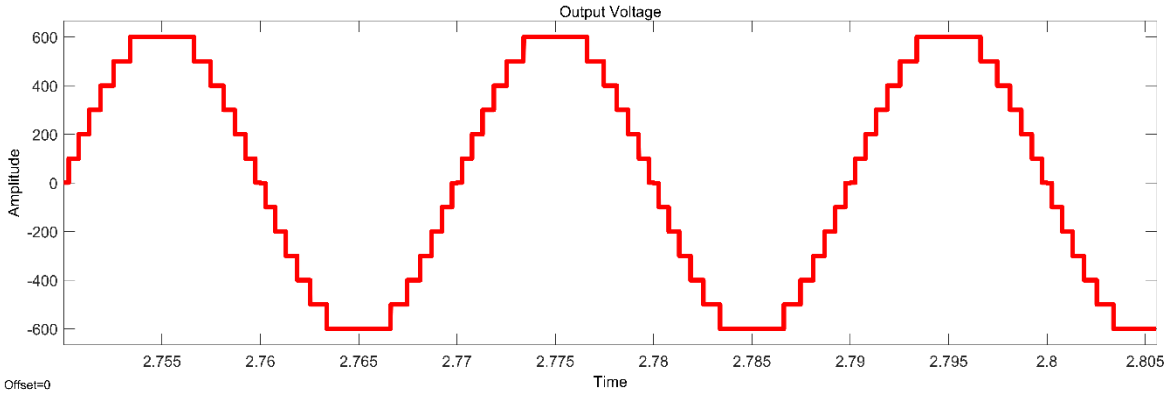
(b)



(c)

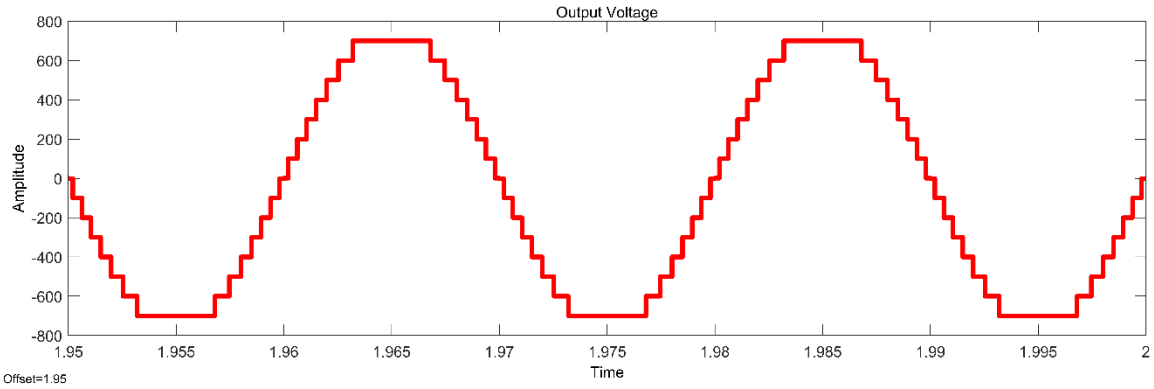


(d)



(e)

Figure 4. Output voltage for 15-level inverter at (b) $m_a = 0.6$, (c) $m_a = 0.7$ (d) $m_a = 0.8$, (e) $m_a = 0.9$, and (f) $m_a = 1.0$ (continued)



(f)

Figure 4. Output voltage for 15-level inverter at (f) $m_a = 1.0$ (continued)

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