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A new configuration of multilevel inverter to generate higher voltage level with lower components

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ABSTRACT

Nowadays, the demand for cleaner and higher quality electricity supply is increasing among various industries and individual consumers. When compared to conventional two-level inverters, multi-level inverters are becoming more and more common, as these inverters deliver high-quality power with fewer harmonics. Here a new multilevel inverter circuit designed with variable direct current (DC) voltage sources is proposed, this circuit requires limited circuit components, and is compared with the other topologies with the same voltage in the output. The proposed topology requires nine switches in order to generate a single-phase 13-level output voltage without connecting to a polarity-generating circuit. The output voltage level and performance parameters associated with the total harmonic distortion (THD) of the voltage level in the output generated by the proposed multilevel inverter or MLI are evaluated in a MATLAB environment. The final simulation results confirm the behavioral accuracy in the proposed topology while creating all the levels. Also, real-time work is done to verify the operation of the inverter and the results are showcased.

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1. INTRODUCTION

An electrical device that converts direct current (DC) voltage to alternating current (AC) voltage is termed an inverter. These inverters are classified into two types. They are current source inverters and voltage source inverters. It consists of switches like metal-oxide-semiconductor field-effect transistor (MOSFET), insulated-gate bipolar transistor (IGBT), supply chain risk management (SCRm), and so on. The inverter can be built to convert solar power input or to function as a backup of power source with batteries that are charged independently. If it's a component of a bigger circuit, like as power supply unit or UPS, the alternate configuration is employed. It is also used in various control drives of electrical machines. In this instance, the inverter is powered by rectified mains AC from the power supply unit (PSU), rectified mains AC from the UPS, and batteries when there is no power. There are different types of inverters which are mainly classified based on their output level and circuit configurations. The inverter produces excess voltage under no-load conditions or very light load conditions, it produces AC at a non-specific frequency. Some of the inverter components require more than one isolated DC supply.

Multilevel inverters have advanced in order to address the drawbacks of traditional inverters. A multilevel inverter is an electronic device that may provide the required alternating voltage by connecting with a minimum DC source. A stepped ac voltage waveform with reduced harmonics can be generated by combining several different DC voltage source ranges. Multilevel inverters have piqued with the interest of

the scholarly community and industry during the last few decades as they are a viable technology for many applications. Baker and Banniser [1] published a patent in the mid-19's outlining the discovery of a topology capable of producing multilevel voltage from separated DC sources and it is called as cascaded topology. Many studies in recent decades have focused on the diode clamp, flying capacitor, and cascaded H-bridge topologies.

In contrast to cascaded H-bridge inverters, the converter can generate a multilayer waveform from a single DC source by connecting additional diodes to the neutral point. This topology is now commonly known as a neutral point-clamped inverter or a diode-clamped inverter. Much of the research in the 1980s was limited to three levels, and the flying capacitor topology was introduced in the 1990s.The requirements of filters are reduced when the output voltage produced is high. The various methods of multicarrier pulse width modulation such as nearest level modulation and pulse width modulation are used to manage the harmonics. The main challenge faced while proposing an inverter is that it should produce a lesser amount of harmonics.

The proposed inverter [2] produces fifteen levels of output voltage just by using eight switches. It can be easily cascaded and produces a higher number of voltage levels. Kahwa *et al.* [3] describes the development of a five-level inverter that has a reduced switching count. The advantage of the H-bridge inverter is that it reduces switching deficiency and total harmonic distortion in motor drives. The phase-shifted sinusoidal pulse width modulation was based on a switching frequency of 6 kHz, and five levels of a single-phase multilevel inverter were constructed using the computer model. The physical security information management (PSIM) based software environments are used to model the outcomes.

Kakar *et al*. [4], an enhanced asymmetrical multilevel inverter design with 17 output voltage levels from two different DC sources is suggested. Arif *et al*. [5] illustrates a brand-new asymmetrical single-phase multilevel inverter design that can provide nine levels of output voltage while using fewer devices. DC sources are used to produce the desired voltage in the output connected in all addition and subtraction combinations using various switches. The proposed topology minimizes the count of dc sources, switches, losses, cost, and inverter size. For the gate drive circuits, the proposed multi-level inverter employs fewer switching components. The proposed inverter consists of a conventional H-bridge and cascade-connected four-level basic cell inverters, as opposed to other popular topologies like the cascade H-bridge and neutral-point-clamped multilevel inverter in [6].

Luciano *et al*. [7] proposes a new switched-source multilevel inverter (SSMLI) topology that requires fewer switches to produce a higher voltage level. An experimental 40 W model inverter was built and tested in [8]. The proposed three H-bridge 27-level cascaded multilevel inverter based on SPWM has been experimentally validated. Babaei [9] shows a multilevel converter topology made up of series-connected sub-multilevel converter blocks with higher output voltage levels. This topology's optimal structures are investigated for a variety of objectives, including multilevel with the reduced number of switches, capacitors, and switch standing voltage.

Babaei and Hosseini [10] develops a novel multilevel inverter that can produce more output voltage levels. A standard H-bridge can be connected in cascade with a simpler cell to create more output voltage levels. Dhanamjayulu *et al.* [11] shows how to build a 31-level asymmetrical multilevel converter without an H-bridge circuit using fewer parts. Three different algorithms for figuring out the magnitudes of DC voltage sources have been given in [12] in order to generate a 53-level to load. A new enhanced three-phase 5-level current-source inverter (CSI) followed in [13] developed with an optimized current control technique. Chaitanya *et al*. [14] seven level seven switch inverter is designed which is tied to the grid.

The proposed inverter reduces the component count when compared to conventional multilevel inverters (MLIs). Power loss and hardware costs are reduced as a result. A 21-level asymmetrical inverter topology is used to support solar PV applications. The developed topology achieves a 21-level voltage output without use of H-bridge by using the asymmetric DC supply [15].

The designed inverter in [16] has six capacitors, five diodes, six DC sources, and nine MOSFETs which generate step signals at load which yields a THD of 7.3%. The inverter designed here performs better than other multilevel inverters (MLIs) when connect to the grid. Kowstubha *et al*. [17] a thirteen-level inverter is developed. Also, a seven-step, nine-step, eleven steps and thirteen-step inverter are designed using MATLAB/Simulink using sine pulse-width modulation (PWM) and a comparison of total harmonic distortion (THD) is done to check and verify the final performance of an inverter [18]–[25].

Authors [1]–[4] use minimum DC sources to generate higher voltage levels, whereas [9] and [16] uses capacitor to clamp the voltages. The extra components make the circuit bulky. In this work, an advanced topology is designed to generate a 13-level inverter with 3 DC sources in the ratio of selected 1:2:4 ratio with 9 MOSFETs and load. Hence, simulation findings of the proposed inverter is analyzed using MATLAB/Simulink software.

2. METHOD

The suggested topology can result in 13-level output voltage with a minimum number of switches than the conventional multilevel topologies and Figure 1 exhibits the topology's planned block diagram. The designed MLI is connected with DC sources. The pulse for the MLI is given by the driver circuit where the logic sequences are included in it.

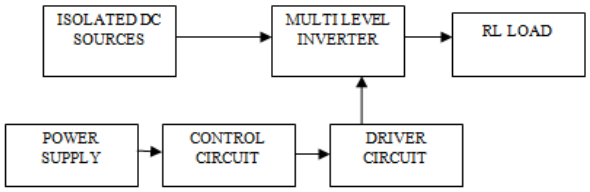

Figure 1. Block diagram of proposed topology

Determination of voltage source and the parameters:

- Ideation 1

The amplitude of the source voltages can be computed from (1).

$$VDC1=VDC2=VDC3=Vdc \quad (1)$$

The switch count for the proposed inverter can be computed as in (2).

$$N_{sw} = 2m+3 \quad (2)$$

The level count for the proposed topology can be computed as (3).

$$N_{lvl} = 2(m-1) +1 \quad (3)$$

The voltage at a peak output of the inverter is achieved as (4).

$$V_{0,\,max} = 2(m-2) \times VDC \quad (4)$$

Where ‘m’ is given as the number of voltage sources connected in the proposed unit.

- Ideation 2

The amplitude of the source voltages can be calculated from (5)-(7).

$$VDC1=Vdc \quad (5)$$

$$VDC2=2Vdc \quad (6)$$

$$VDC3=3Vdc \quad (7)$$

The switch count for the proposed inverter is calculated as given in (8).

$$N_{sw}= 2m+3 \quad (8)$$

The level count for the proposed topology is calculated as given in (9).

$$N_{lvl} = 2m+2 \quad (9)$$

The voltage at a peak output of the inverter is achieved as given in (10).

$$V_{0,\,max} = (2m-1) \times VDC \quad (10)$$

Where ‘m’ is given as a number of voltage sources connected in the proposed unit.

- Ideation 3

The amplitude of the source voltages can be calculated from equations (11)-(13).

$$VDC1=Vdc \quad (11)$$

$$VDC2=2Vdc \quad (12)$$

$$VDC3=4Vdc \quad (13)$$

The switch count for the proposed inverter can be computed as (14).

$$N_{sw} = 2m+3 \quad (14)$$

For the proposed topology, the level count can be calculated as (15).

$$N_{lvl} = 2(m+1) -3 \quad (15)$$

The voltage at a peak output of the inverter is achieved as (16).

$$V_{0,\,max} = 2m \times VDC \quad (16)$$

Where 'm' is given as a number of voltage sources connected in the proposed section.

For the design circuit shown in Figure 2, the voltage levels are chosen in the ratio of 1:2:4 with respect to ideation 3 and Figure 2 exhibits the proposed circuit diagram for thirteen level inverter. Table 1 shows several switching states of the new proposed topology. Here, '1' represents the state of the switch is ON, and '0' represent that the switch is off. The proximate level modulation technique is implemented in order to suppress the presence of harmonics across the load. The modes of operating generating various voltage levels are shown in Figure 3 to Figure 7.

Table 1. Switching state of 13-level inverter

Vo	S1	S2	S3	S4	S5	S6	S7	S8	S9	Vo	S1	S2	S3	S4	S5	S6	S7	S8	S9
V2+V3	1	0	0	1	0	1	1	0	1	–(V2–V1)	0	1	1	0	0	1	1	1	0
V1+V3	0	1	1	1	0	1	1	0	0	– (V2)	1	0	1	0	0	1	1	1	0
V3	1	0	1	1	0	1	1	0	0	– (V3–V1)	0	1	0	0	1	1	0	1	1
V1+V2	0	1	0	1	1	1	0	0	1	– (V3)	1	0	0	0	1	1	0	1	1
V2	1	0	0	1	1	1	0	0	1	– (V3+V2–V1)	0	1	1	0	1	1	0	1	0
V1	0	1	1	1	1	1	0	0	0	– (V3+V2)	1	0	1	0	1	1	0	1	0
0	1	0	1	1	1	1	0	0	0										

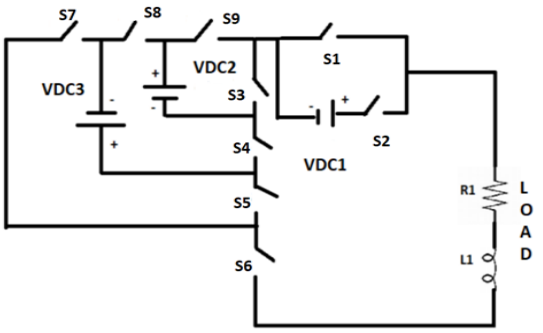

Figure 2. Circuit diagram of 13-level asymmetrical inverter topology

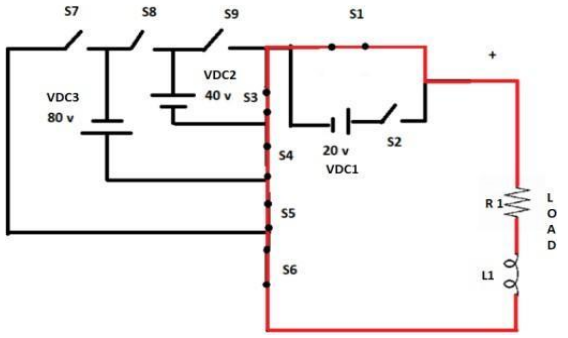

Figure 3. The mode of voltage levels 0 V

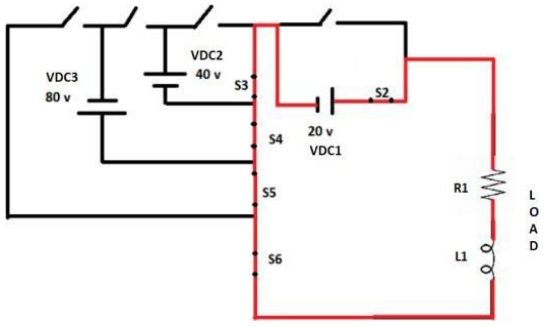

Figure 4. The mode of voltage levels 20 V

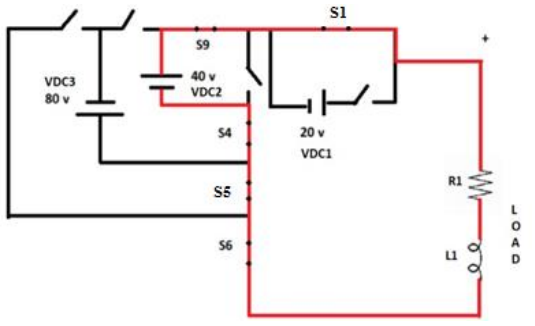

Figure 5. The mode of voltage levels 40 V

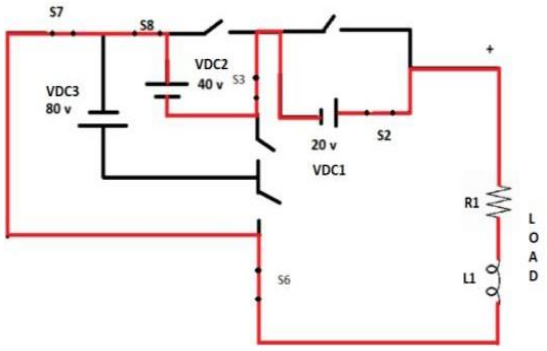

Figure 6. The mode of voltage levels -20 V

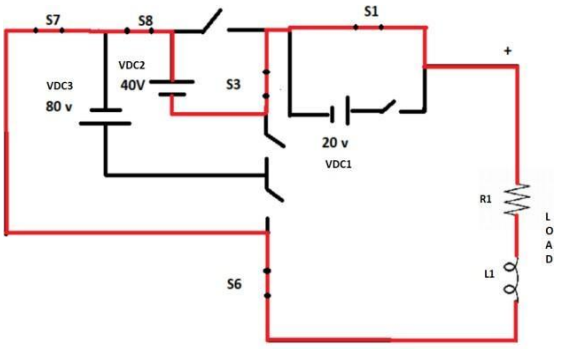

Figure 7. The mode of voltage levels -40 V

2.1. Design of 13-level inverter VIA simulation study

2.1.1. Nearest level modulation

The pulse width modulation is one of the controlling techniques which control the inverter internally without the usage of external circuits. These PWM techniques are broadly classified into several types and the most commonly used is sinusoidal pulse width modulation (SPWM) which requires the carrier signal. Among the various types of pulse width modulation, nearest level modulation does not require any carrier signals such as triangular wave or square wave signals. This nearest level modulation (NLM) technique is one of the most popular modulations which reduce the THD to a higher extent. The sine wave for the required level is generated in this method and it is shown in Figure 8. Then the generated wave is split using the constant block. The comparison of the original wave and split wave using a comparator and fed the comparator output to the AND gate and then fix the gain and it is fed to other stage is summer. Then the output of the summer is fed to the multiport switch to give the generated pulse to the MOSFET gate.

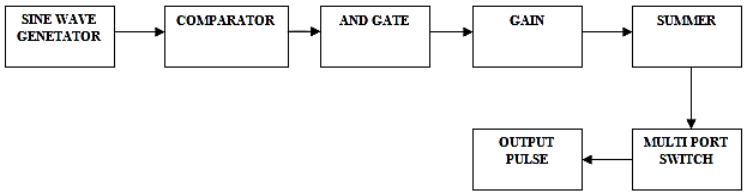

Figure 8. Block diagram of nearest level modulation

3. RESULTS AND DISCUSSION

3.1. Simulation results

The performance and analysis of the new proposed topology a facsimile model of the single phase 13-level new multilevel inverter is developed using MATLAB/Simulink environment based on Figure 1. Three input DC sources with VDC1 =2 V, VDC2= 4 V, VDC3=8 V chooses to generate 13 voltage steps at the load. The gate pulses to the switches are given using the nearest level modulation technique as shown in the Table 1. The designed MLI is checked with repellent and impedance load, and the output waveforms of R load (R= 10 Ω) are shown in Figure 9. The designed 13-level inverter is fed to RL load (R=10 Ω, L= 5 mH), and the output waveforms is shown in Figure 10. The presence of symphonic in load waveforms are observed using fast fourier transform (FFT) analyzer from the simulation model and it is shown in Figures 11 and 12 respectively for resistive and impedance loads. The THD of current waveform using R load is measured as 6.93% where for RL load, it is observed as 3.91% which is shown in Figure 13.

3.2. Design of 13 - level inverter – experimental works

Design of 13-level inverter is carried out in the real-time to test the performance of the inverter. The development circuit consists of MOSFET switches, opto-coupler, peripheral interface controller or PIC microcontrollers for generating gate signals and it is shown in Figure 14. The developed 13-level inverter is subjected to experimentation for R and RL load as per the parameters shown in Table 2 and the test results are shown in Figure 15 for R load and Figure 16. for RL load, when combined with multilevel inverters, are crucial for applications requiring reduced harmonic distortion, improved efficiency, precise voltage regulation, and grid compatibility.

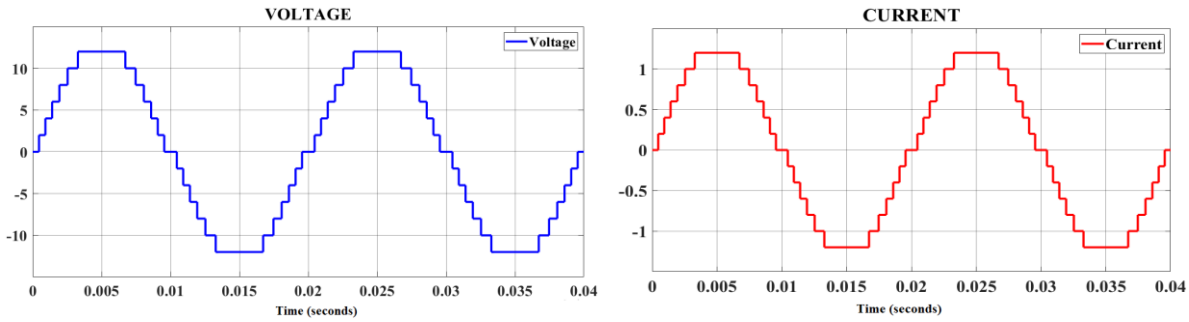

Figure 9. Output voltage and current waveform of R load

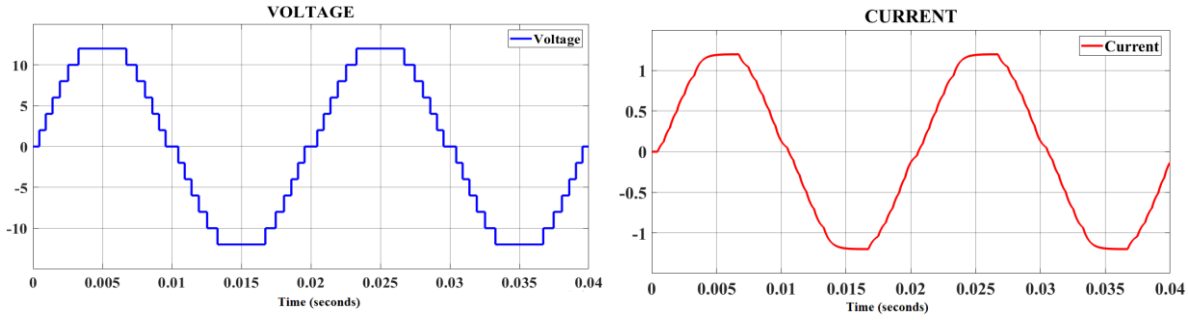

Figure 10. Output voltage and current waveform of RL load

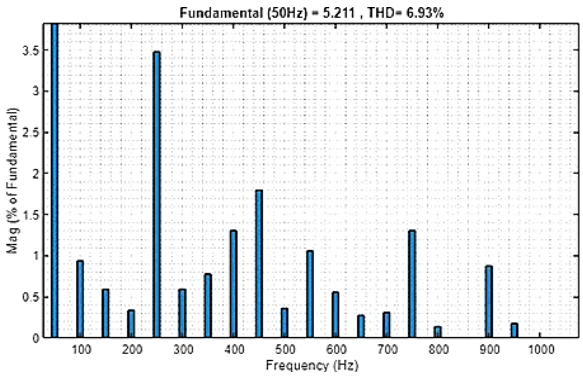

Figure 11. Output voltage and current THD for R load

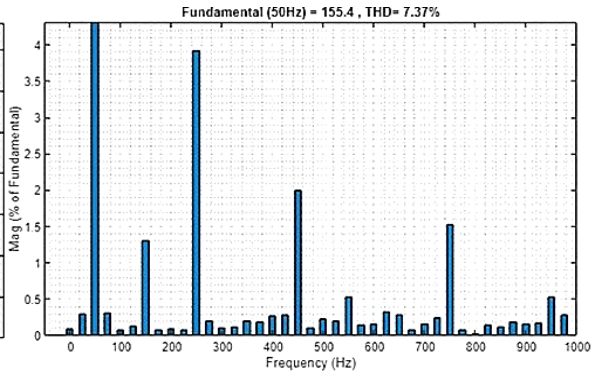

Figure 12. Output voltage THD for RL load

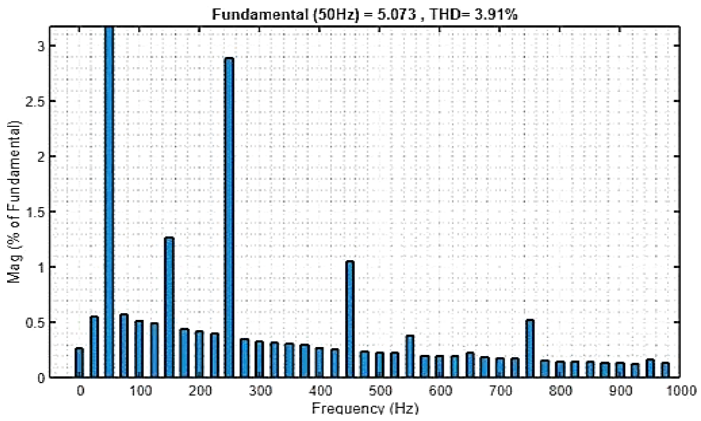

Figure.13. Output current THD for RL load

Table 2. Specification of components in developed inverter

Name of the component	Specifications
MOSFET	IRF840
Driver Circuit	L239D
Step-down Transformer	25V
Bridge Rectifier	MB3510
Voltage Regulator	7805
Microcontroller	PIC16F877
R load	600Ω
RL load	500Ω and 300 mH

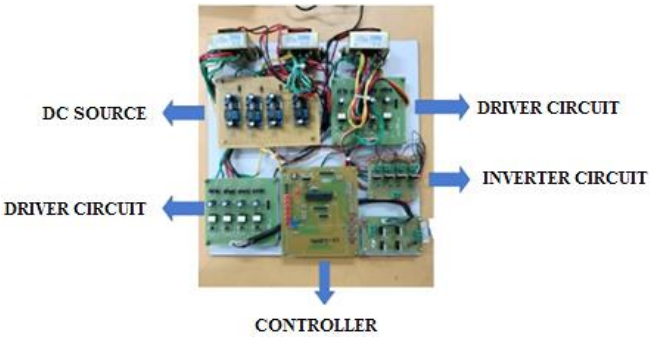

Figure 14. Hardware set up-13 level inverter

3.3. A comparison on specification between the proposed with developed inverters

A design comparison is made in Table 3 to show the required number of switches, sources, trigger circuits, diodes, capacitors and on state switches in the circuit for the conventional inverters, recent inverter design and proposed new inverter which is shown in Figure 17 and Figure 18. The comparison is made to study the inverter's performance in terms of reduction in circuit components. From the figure, it is seen that for generating 13 voltage steps at the load, the proposed inverter uses minimum circuit components compared to the other inverter.

Table 3. Design comparison between developed inverter and proposed

Details	NPC	FC	CHB	Kumar and Thakura [16]	Kowstubha *et al*. [17]	Proposed
No. of switches	28	28	24	9	20	9
No. of sources	12	12	6	6	5	3
No. of drivers	28	28	24	9	20	9
No. of ON state switch	14	14	12	3	10	5
No. of diodes/capacitors	14	12	-	-	-	-
No. of voltage step	13	13	13	13	13	13

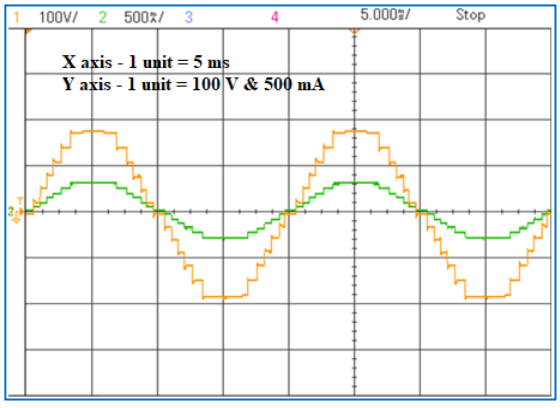

Figure 15. Output voltage and current for R load

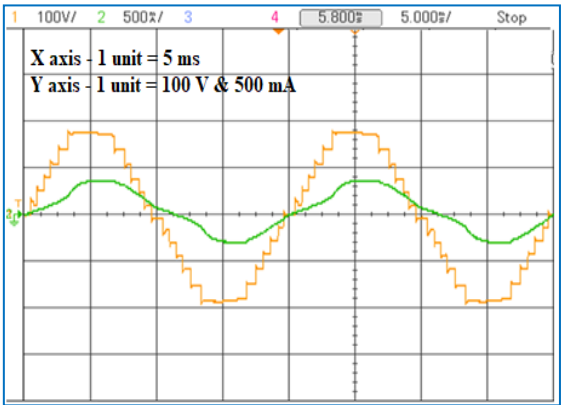

Figure 16. Output voltage and current for RL load

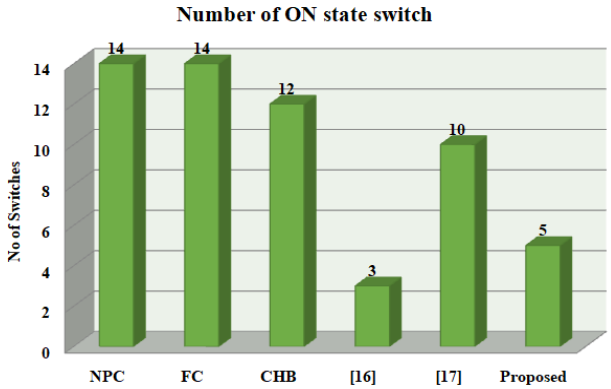

Figure 17. Number of ON state switches

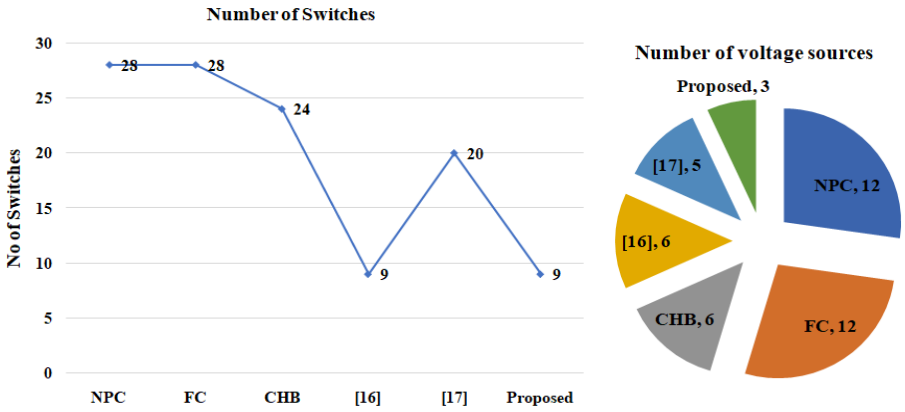

Figure 18. Number of switches and voltage sources

4. CONCLUSION

This study depicts a new single-phase MLI topology which generated 13 voltage levels across the load. The main proposed objective of implementing the MLI is to manufacture electronic components with reduced power components. The proposed topology generates 13 voltage levels using 3 asymmetric source configurations with 9 switches and it can generate all voltage levels without using the H-bridge inverter. The current THD observed from the design topology is 3.91% for RL load. Here, a low voltage-rated semiconductor component is used in this circuit. In order to illustrate its performance, it is also compared to other newly developed MLIs and conventional MLIs in terms of the quantity of power switches and the DC sources. Studies show that compared to other topologies and low-voltage switches, this MLI architecture uses fewer power switches. The effectiveness and viability of the MLI circuit have been validated by simulation and prototype findings.

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