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Common mode voltage mitigation in a three phase 21-level asymmetrical inverter fed induction motor

Mamatha Narayana, Ramesh Honnappanahalli Rajappa
Department of Electrical Engineering, University Visvesvaraya College of Engineering,
Bangalore University, Bangalore, India

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ABSTRACT

For many years, numerous high-power applications have been found to cause mechanical damage to the rotating shaft. This research demonstrates that common mode voltage (CMV), which causes common mode leakage currents to flow into the motor bearings and spinning shaft, is one of the main contributing factors to mechanical shaft failures. By applying a carrier based Sinusoidal pulse width modulation (PWM) approach in conjunction with a proportional integral or PI controller technique in the feedback, the study aims to reduce leakage currents by mitigating the common mode voltages induced by the inverter output asymmetry. To accomplish the stated goal, an asymmetrical inverter architecture with a 21-level is employed. The literature emphasized the trade-off between total harmonic distortion (THD) and CMV, which is attempted to be kept well below IEEE's allowable bounds. The system stability is verified and proved by plotting the bode diagram.

Corresponding Author:

Mamatha Narayana
Department of Electrical Engineering, University Visvesvaraya College of Engineering
Bangalore University
Bangalore-560001, Karnataka, India
Email: nayak.mamtha@gmail.com

1. INTRODUCTION

Conventional pulse width modulation (PWM)-based inverters operate at high frequencies based on the switching frequencies of the switch, resulting in high di/dt and dv/dt outputs [1]. This can lead to a leakage current reaching the load due to parasitic capacitance between the motor winding and the iron core [2]. Spikes in the leakage current align with the insulated-gate bipolar transistor/metal-oxide-semiconductor field-effect transistor (IGBT/MOSFET) switching moment. Anyone who touches the ungrounded motor core risks electrocution.

Fast-switching inverter-fed electrical AC devices may experience bearing failures due to current and voltage stress [2]. Voltage source inverters (VSI) have high dv/dt at machine contacts due to high-frequency machine capacitances, resulting in voltages discharged through bearings when they exceed the lubricant breakdown voltage (1.5–30 V), causing electric discharge machining (EDM) currents [3]. The High-frequency common mode (CM) currents flowing to the ground result in undesirable parasitic effects [4], most notably electromagnetic interference (EMI) with electrical equipment, grounding issues, or effects on drive control. Fast-switching of power semiconductor devices in the inverter produces electrical interference signals with high transient and current pulses, becoming a significant source of disturbance in motor driving systems [5].

The issue of converter asymmetry must be addressed to minimize leakage current in the induction motor (IM) [6], [7]. This can be mitigated by choosing the right PWM technique. Multiple phase inverters can help in CMV reduction [8], [9]. The concept of a dual voltage source inverter is discussed in [10], [11]. Various

modulation methods like carrier based - phase-shifted, level-shifted PWM [12], [13], multi-reference PWM [14], low-switching-frequency modulation techniques such as synchronous optimum PWM [15], nearest level control, active harmonic elimination [16], and selective harmonic elimination [17] have been documented in the literature. The superiority of SVPWM in eliminating CMV in VSI-fed VSDs is proven [18]. However, SVPWM's complexity at higher levels and its lack of acceptance among users have led researchers to consider other PWM implementations, such as hybrid PWM [19]. AMLI has been highly regarded in the literature due to its numerous advantages. These include reducing stress on switches, utilizing lower voltage rating switches, decreasing filter size, or even eliminating filters. Additionally, AMLI offers better THD, a higher quality output voltage, and facilitates easy implementation of topology for higher ratings [20], [21]. Consequently, AMLI configurations find application in three-phase high-power scenarios effectively.

There are two primary approaches for reducing the CMV in power electronic systems: hardware circuit-based methods and PWM based methods. The hardware circuit-based methods have shown success in eliminating CMV but have drawbacks such as requiring additional components, frequent maintenance, increased cost and size, and losses. PWM-based methods aim to mitigate CMV by using scientifically designed topologies and suitable PWM strategies without requiring extra components. Instead, they rely on optimizing the PWM strategy to address both THD and CMV [2].

We propose a 3-phase, 21-level asymmetrical inverter for powering an induction motor. Level-shifted carrier-based PWM with higher DC utilization switches MOSFETs optimally, reducing THDs. A PI controller monitors CMV and provides signals to CVS blocks, reducing leakage currents. A well-known PI controller simplifies design without advanced optimization. The paper introduces system stability assessment via Bode plot and adoption of CVS blocks, unique in similar literature.

2. PWM INVERTER GENERATED COMMON MODE VOLTAGE

Figure 1 depicts the widely used three phases, a 2-level VSI with three legs and six switch structures used in variable speed drives (VSDs) [2]. The two capacitors with value $V_{dc}/2$ divide the V_{dc} into two halves and create a midpoint between them which is treated as common ground point 'g'. This inverter drives a 3-phase star connected Induction motor with 3 equal impedances Z_{Rm}, $Z_{Ym,}$ and Z_{Bm} with the neutral to ground parasitic impedance Z_{mg}.

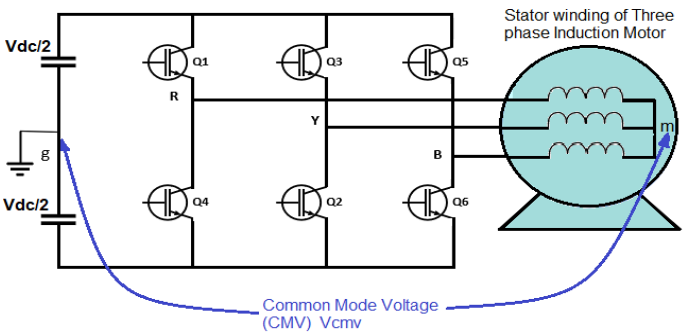


Figure 1. Three phase 2-level VSI

According to the principle of charge conservation, the equation for the circuit can be written as (1).

$$\frac{V_{mg}}{Z_{mg}} = \frac{V_{Rg}-V_{mg}}{Z_{Rm}} + \frac{V_{Yg}-V_{mg}}{Z_{Ym}} + \frac{V_{Bg}-V_{mg}}{Z_{Bm}} \quad (1)$$

For a balanced motor with an equal value of phase impedance, we can write as in (2).

$$Z_{Rm} = Z_{Ym} = Z_{Bm} \quad (2)$$

Now the neutral point voltage can be expressed as (3).

$$V_{mg}(t) = \frac{3Z_{mg}}{3Z_{mg}+Z_{Rm}} * Vcm(t) \quad (3)$$

Where $Vcm(t)$ is the CMV and is defined as (4) and (5).

$$Vcmv = \frac{Z_{Rm}+Z_{Ym}+Z_{Bm}}{3} \quad (4)$$

$$Vcmv = \frac{1}{3}\sum_{R}^{B} V_{Xm} \quad (5)$$

Where X= R, Y, B. From the above equation, it can be concluded that the CMV will not be generated in the motor drives whose input voltages satisfy the (6).

$$V_{Rg} + V_{Yg} + V_{Bg} = 0 \quad (6)$$

The CMV is produced between the neutral of the motor drive load and the DC midpoint/common dc point in the PWM driven inverter due to its output being discretized. The common mode phenomenon negatively impacts the electrical insulation performance, characteristics, and lifespan, and can lead to motor burnout. Parasitic capacitances can be identified by measuring the induction motor impedance using an LCR bridge. The magnitude and frequency of the generated CMV are proportional to the DC link voltage and inverter circuit switching frequency, respectively. The output phase voltage for the above circuit is given by (7).

$$\begin{aligned} V_{Rm} &= V_{Rg} - V_{mg} = R_s i_R + L_s \frac{di_R}{dt} + e_R \\ V_{Ym} &= V_{Yg} - V_{mg} = R_s i_Y + L_s \frac{di_Y}{dt} + e_Y \\ V_{Bm} &= V_{Bg} - V_{mg} = R_s i_B + L_s \frac{di_B}{dt} + e_B \end{aligned} \quad (7)$$

Where R_s and L_s define the stator resistance and reactance. V_{mg} represents the voltage difference between the dc bus midpoint 'g' and the stator neutral 'm' which can be given as shown in the (8) [22].

$$\begin{aligned} V_{mg} &= \frac{1}{3}\left\{\left(V_{Rg} + V_{Yg} + V_{Bg}\right) - R_s(i_R + i_Y + i_B) - \frac{d}{dt}(i_R + i_Y + i_B) - (e_R + e_Y + e_B)\right\} \\ &= \frac{1}{3}\left\{\left(V_{Rg} + V_{Yg} + V_{Bg}\right) - R_s i_o - \frac{d}{dt}(i_o) - e_o\right\} \end{aligned} \quad (8)$$

Where, $i_o = i_R + i_Y + i_B$ and $e_o = e_R + e_Y + e_B$

3. GENERALIZED AMLI TOPOLOGY (R-PHASE) WITH LESS SWITCHES

In this section, a 3-phase generalized topology with fewer switches is explained for the R-phase of the circuit as displayed in Figure 2. It is an Asymmetrical MLI topology divided into two main sections: the Voltage level generating section with MOSFET switches and DC sources in series with diodes, and the polarity changing section with 4 switches. For 'x' DC sources, each phase needs the same number of diodes and 4+x switches. The polarity-changing block changes the DC voltage to generate converter output voltages up to 'b' levels (1:2:3:4 ratio, x=4 and b=21 in this paper). Changing the Vdc ratio increases voltage levels for the same circuit. A Cascaded H-Bridge topology with a similar number of DC sources is limited to 9 levels only [23].

To implement the circuit for a 3-phase 21-levels inverter, each phase of the voltage levels generating section must include four DC sources and 8 switches (including 4 diodes). This generates voltage levels with the magnitudes of 0, $\pm 1V_{dc}$, $\pm 2V_{dc}$, $\pm 3V_{dc}$, $\pm 4V_{dc}$, $\pm 5V_{dc}$, $\pm 6V_{dc}$, $\pm 7V_{dc}$, $\pm 8V_{dc}$, $\pm 9V_{dc}$, and $\pm 10V_{dc}$ where the second part of the circuit majorly contributes for the polarity reversal. The circuit diagram of a 21-level AMLI with less number of switches implemented for three phases is shown in Figure 3.
The generalized switching function (Spx) for the 21-level AMLI is given by (9).

$$V_{ph}(t) = \sum_{1}^{4}[xVdc * Spx] * (\pm 1) \quad (9)$$

Where, x= number of dc sources, p= R, Y and B

Whereas Spx signifies the on and off state of the switches with 'p' representing the phase. Table 1 details the switching sequences for various R-phase modes. Phases Y & B follow the same pattern with 120 and 240-degree phase shifts, generating output voltage levels from +10Vdc to -10Vdc. The adopted topology's operation for positive rising levels is displayed in Figure 4, with equivalent circuits. Similar analysis can be applied to other levels in the positive and entire negative cycle.

Table 1. Switching table of 21 level AMLI

S1	S2	S3	S4	S5	S6	S7	S8	Switching function	Output voltage
1	1	1	1	1	1	0	0	$[1V_{dc}+2V_{dc}+3V_{dc}+4V_{dc}][S_{1,2.3.4}]$	10V1
0	1	1	1	1	1	0	0	$[2V_{dc}+3Vdc+4V_{dc}][S_{2,3,4}]$	9V1
1	0	1	1	1	1	0	0	$[1V_{dc}+3Vdc+4V_{dc}][S_{1,3,4}]$	8V1
0	0	1	1	1	1	0	0	$[3V_{dc}+4V_{dc}][S_{3,4}]$	7V1
0	1	0	1	1	1	0	0	$[2V_{dc}+4V_{dc}][S_{2,4}]$	6V1
1	0	0	1	1	1	0	0	$[1V_{dc}+4V_{dc}][S_{1,4}]$	5V1
0	0	0	1	1	1	0	0	$[4V_{dc}][S_4]$	4V1
0	0	1	0	1	1	0	0	$[3V_{dc}][S_3]$	3V1
0	1	0	0	1	1	0	0	$[2V_{dc}][S_2]$	2V1
1	0	0	0	1	1	0	0	$[1V_{dc}][S_1]$	1V1
0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	1	1	$[1V_{dc}][S_1](-1)$	-1V1
0	1	0	0	0	0	1	1	$[2V_{dc}][S_2](-1)$	-2V1
0	0	1	0	0	0	1	1	$[3V_{dc}][S_3](-1)$	-3V1
0	0	0	1	0	0	1	1	$[4V_{dc}][S_4](-1)$	-4V1
1	0	0	1	0	0	1	1	$[1V_{dc}+4V_{dc}][S_{1,4}](-1)$	-5V1
0	1	0	1	0	0	1	1	$[2V_{dc}+4V_{dc}][S_{2,4}](-1)$	-6V1
0	0	1	1	0	0	1	1	$[3V_{dc}+4V_{dc}][S_{3,4}](-1)$	-7V1
1	0	1	1	0	0	1	1	$[1V_{dc}+3Vdc+4V_{dc}][S_{1,3,4}](-1)$	-8V1
0	1	1	1	0	0	1	1	$[2V_{dc}+3Vdc+4V_{dc}][S_{2,3,4}](-1)$	-9V1
1	1	1	1	0	0	1	1	$[V_{dc}+2V_{dc}+3V_{dc}+4V_{dc}][S_{1,2.3.4}](-1)$	-10V1

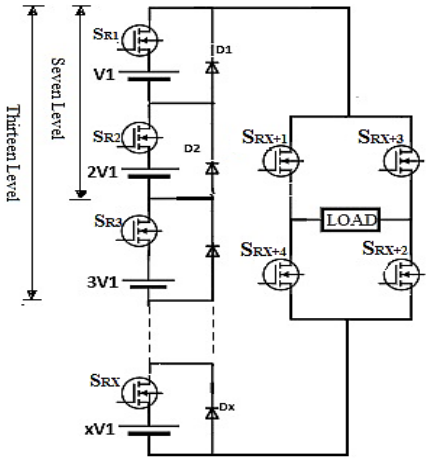


Figure 2. Generalized AMLI topology (R-Phase)

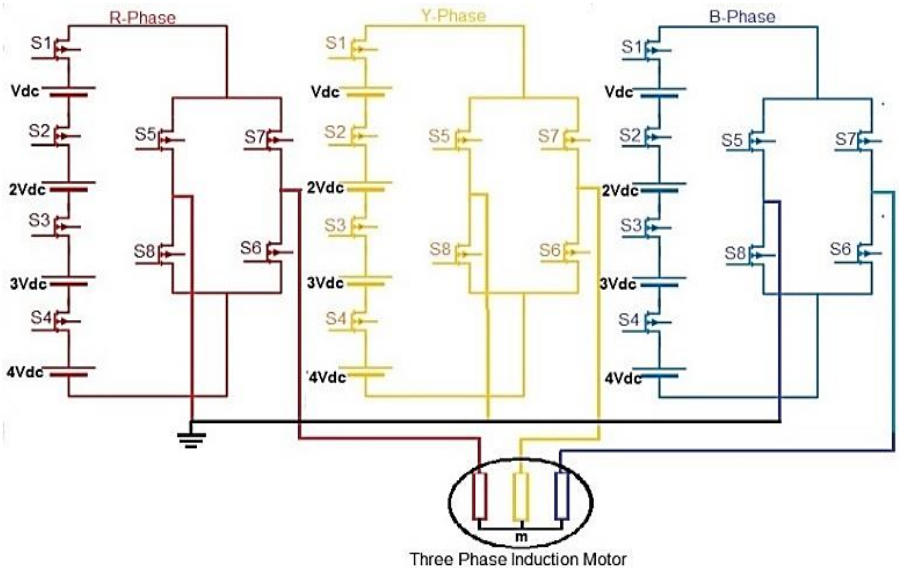


Figure 3. Three phase 21-level AMLI topology

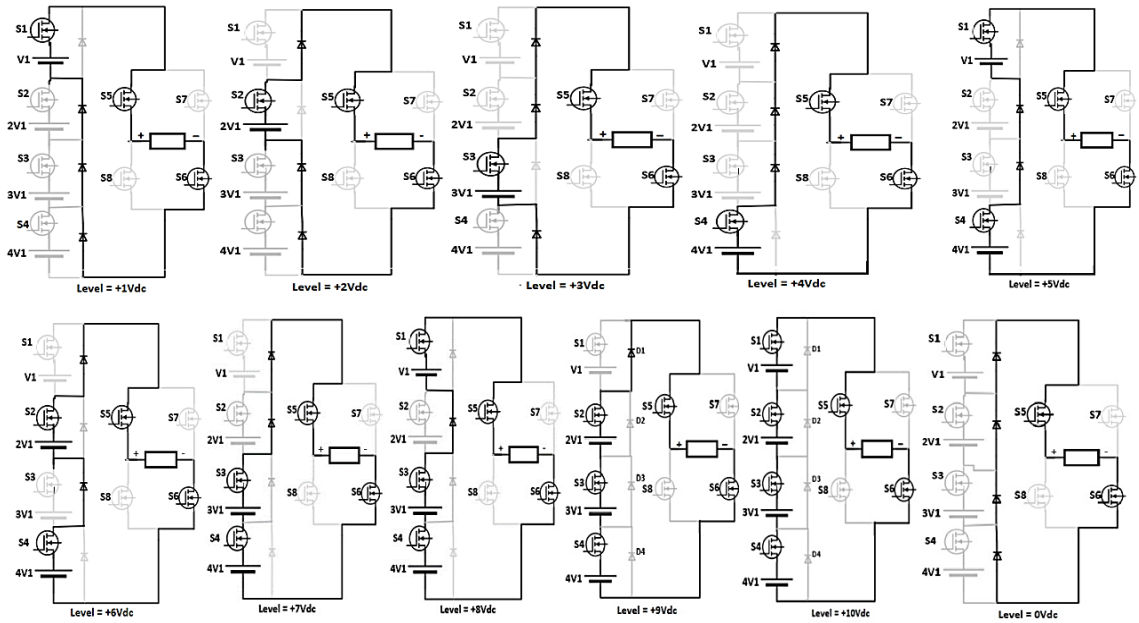


Figure 4. Equivalent circuit diagrams for R-phase of 21 level inverter for various levels

4. OPERATION PRINCIPLE OF THE PROPOSED PWM

It is evident in the literature that CMV can be minimized by avoiding traditional PWM techniques like SPWM [24]-[26]. This section presents the basic idea behind such PWMs, which aim to eliminate CMV at all points in time. To overcome the complexity of the SVPWM at higher levels, a carrier-based SPWM with PI control technique is adopted in this work. The Phase Opposition Disposition PWM Switching control having 20 carrier waves of high frequency (3 kHz) is compared with a sinusoidal waveform of fundamental frequency with a modulation index of 0.9 to generate the required gating signals. The phase voltage expression for a 'x' number of dc sources, 'b' level inverter is given by (10).

$$V_{ph} = \pm V_{dc}(t) \pm 2V_{dc}(t) \pm \ \ldots\ldots\ldots\ldots \pm (2x+2)\, V_{dc}(t) \quad (10)$$

Where, $V_{ph}(t)$ for any phase is given by the equation (9), which can be expanded for 21 levels further as (11).

$$V_{R_{ph}}(t) = \sum_{x=1}^{4} [1V_{dc} * S_{R1} + 2V_{dc} * S_{R2} + 3V_{dc} * S_{R3} + 4V_{dc} * S_{R4}] * [S_{R(x+1)} * S_{R(x+2)}] \quad (11)$$

The closed-loop implementation reduces V_{cmv} by comparing the common mode signal with zero value. Typically, the block receives an input in the form of an error signal, which represents the disparity between a reference signal and the system's CMV output. The proportional (P) and integral (I) constants of the PI controller can be adjusted either manually or automatically. The output of the PI controller block is a combination of a weighted sum of the input signal and the integral of the input signal, along with the derivative of the input signal. The weights are the proportional, integral, and derivative gain parameters. The DC voltage sources used are the Controlled Voltage Source type which converts the error input signal into an equivalent voltage source. The PI controller implemented with the CVS block in place of the dc voltage source results in a mitigation of CMV along with achieving minimal THDs.

5. RESULTS AND DISCUSSION

A MATLAB simulation model shown in Figure 5 is developed to verify the modulation method proposed in the paper. An AMLI topology with Closed-loop control ensures leakage current-free operation of the induction motor. The asymmetrical topology comprises four sources with voltage ratios of V1: 2V1: 3V1: 4V1 to feed a 5.4HP (4 kW), 400 V, 50 Hz, 1430rpm 3-phase induction motor load. A total DC link voltage of 320 V is distributed based on the ratio. The CVS block is initialized with a specific voltage, while error CMV is converted into a DC source and fed to the CVS block. Shaft mechanical torque is calculated as per [27], Tm = 26.7 Nm, and the inverter's switching frequency is set at 3 kHz for simulation. The output CMV is fed to the controlled voltage source block, enhancing DC bus utilization by 8.8%.

To verify the efficacy of the proposed control technique in reducing the CMV and THD of the AMLI, detailed analysis is carried out for PD, POD, and APOD. The graphical representation of the resultant values

is shown in Figure 6. CMV is drastically reduced from PD, POD, and APOD as Vdc/29, Vdc/33, and Vdc/45, respectively. CMV and THD of both voltage and current are reduced in the APOD case compared to other techniques. Closed-loop control maintains CMV as low as possible throughout the operation.

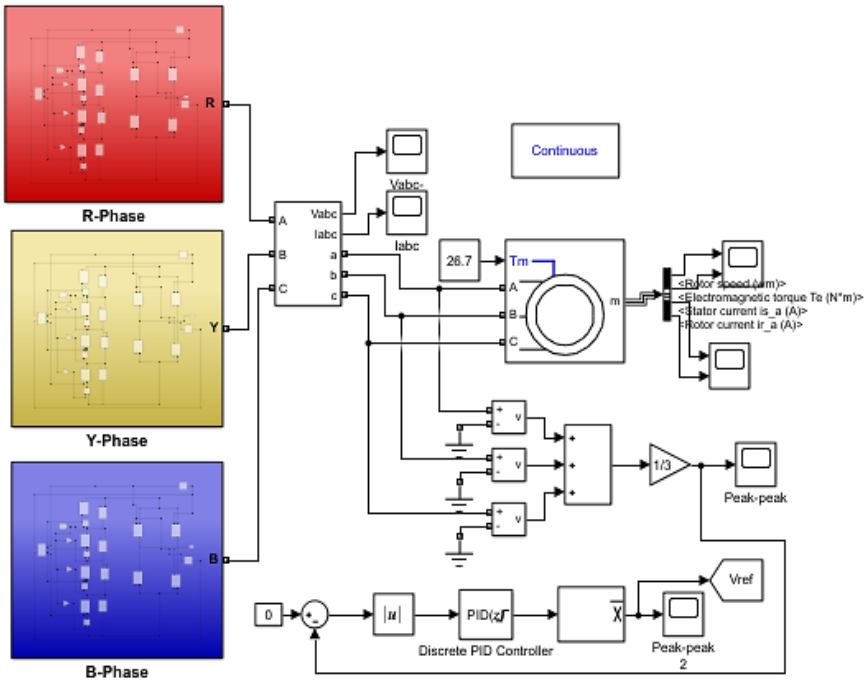


Figure 5. Simulink model of the 21 level AMLI topology

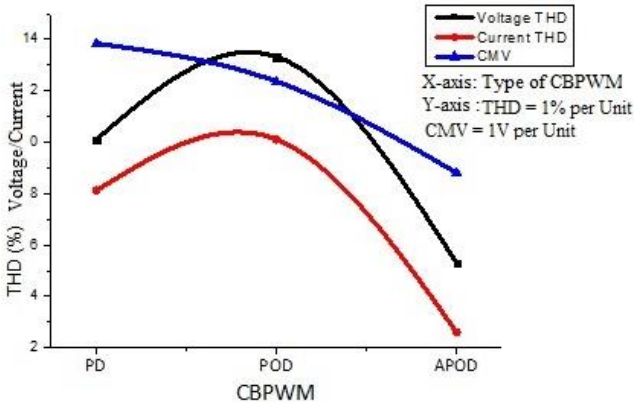


Figure 6. Comparison of CBPWM technique

Figure 7 shows three phase transient current waveform when the induction motor is controlled by the proposed control technique and AMLI. The three phase currents namely I_R, I_Y, and I_B are plotted and displayed. The peak value of the R-phase transient current is found to be 47 A, Y-Phase and B-Phase transient currents to be 38 A and 30 A respectively. After a settling time of 0.12 sec, the steady state value of each maximum phase current is found to be 12 A. Figure 8 shows the output phase voltages obtained from the multilevel inverter which is applied to the stator of 3-phase induction motor. The output voltage peak of each phase is found to be 520 V. Thus, $520/\sqrt{2} = 367$ V is the rms value, which is lower than the induction motor rated voltage.

The harmonic analysis of three phase output waveform is carried out using Fast Fourier Transformation (FFT) analysis and the harmonic content of the output voltage is found to be 5.16% and the currents is 2.60% as shown in Figure 9, which is well within the standard permitted value of IEEE. The resultant CMV waveform having a magnitude of 8.84 V with a frequency of 591 Hz and the waveform of CMV without the proposed controller with a magnitude of 51V ($V_{dc}/6$) are seen in Figure 10. In the proposed work, the

tradeoff between the THD and CMV has been overcome by reducing the CMV by keeping the THDs within the allowable limits of IEEE. The corresponding speed and torque waveforms of the induction motor are displayed in Figure 11.

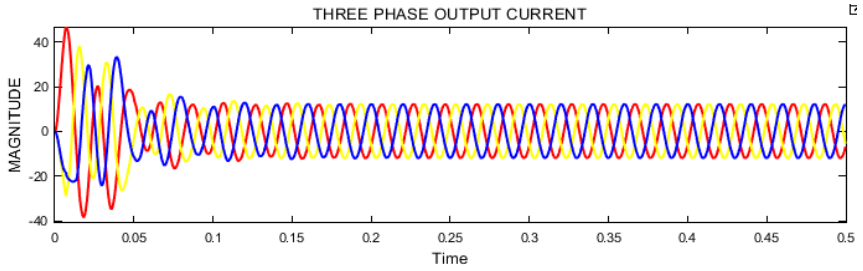


Figure 7. 3-phase transient current waveform

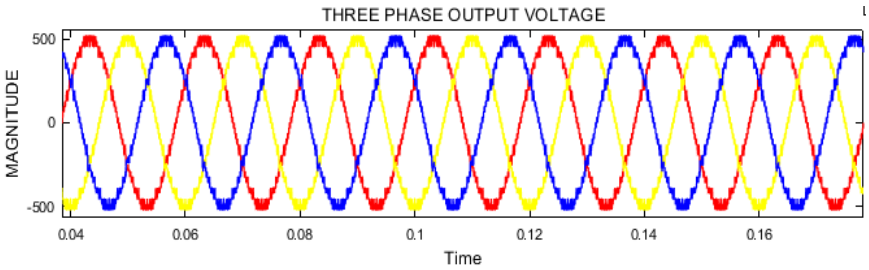
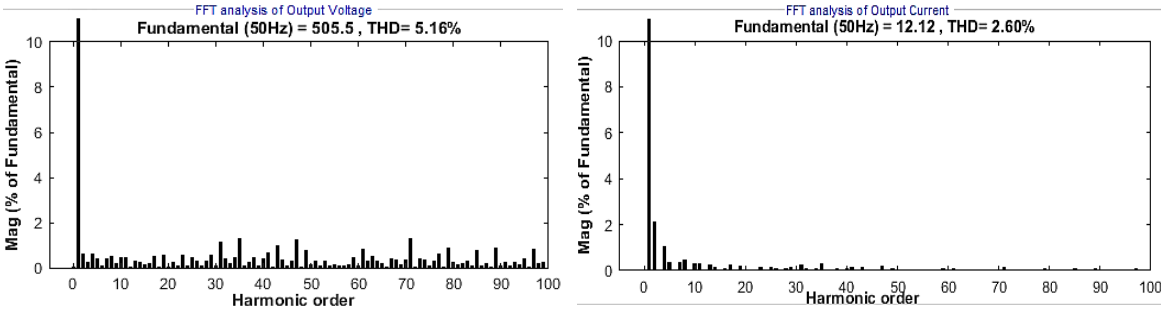


Figure 8. 3-phase output voltage waveform of MLI



(a) (b)

Figure 9. FFT analysis of output of (a) voltage and (b) current

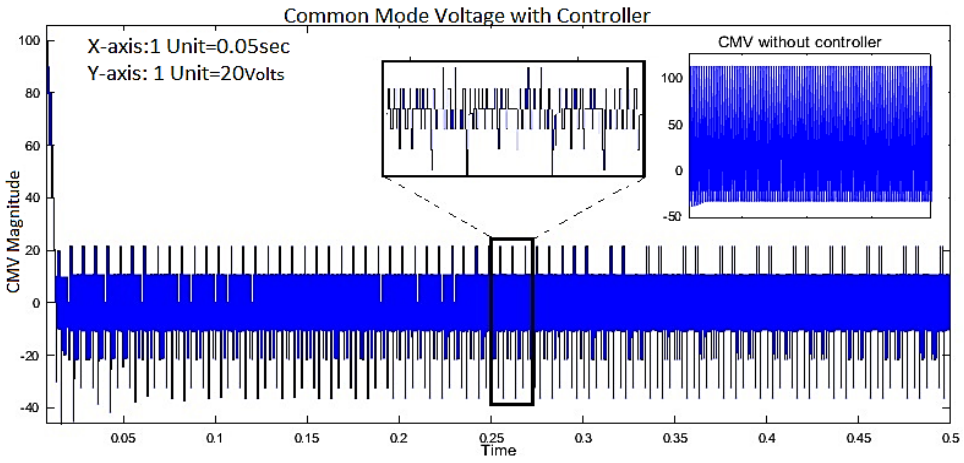


Figure 10. The resultant CMV waveform without controller and with controller

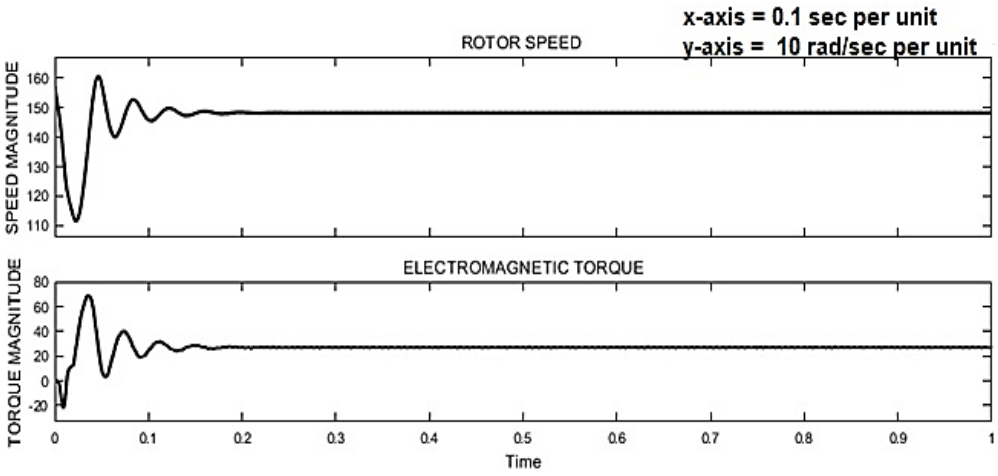


Figure 11. Rotor speed and torque waveform of AMLI fed induction motor

To evaluate system stability and justify the proposed technique, the Bode plot method is adopted, which represents a distinctive approach that is not widely adopted in similar papers. By determining the system transfer function (g) and plotting a bode diagram as displayed in Figure 12, the output speed waveform is examined to confirm the stability of the system. The magnitude plot shows the change in the magnitude of the system concerning the increase in the frequency. The phase plot displays the change in the system phase concerning the change in frequency at 35.5 rad/sec & positive. Phase gain = 174 degrees positive. The stability of the system was manually verified using the RH criteria method with the obtained transfer function.

The findings such as number of switches, diodes, DC sources, CMV magnitude obtained from the proposed methodology are compared with the literature on 21-level inverters that is already available. Table 2 illustrates the superiority of the proposed control methodology in reducing the THD as well as CMV magnitude. The adopted topology is bearing least number of switches compared to other mentioned references.

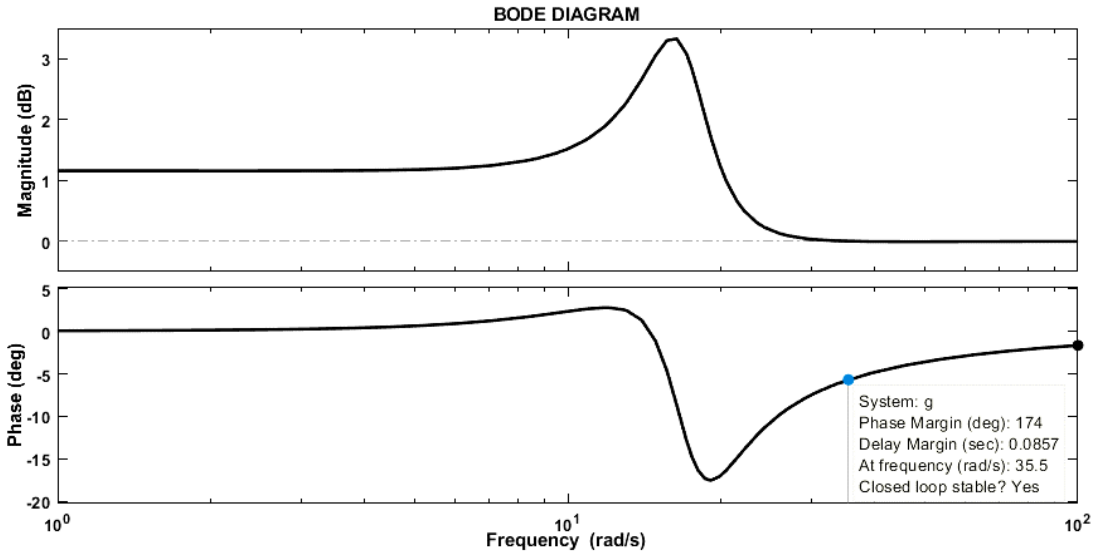


Figure 12. Bode diagram indicating the system stability

Table 2. Component and performance metrics in related works

Ref	Levels	No of switches	No of diodes	DC sources	Vthd (%)	CMV (V)
[12]	21	11	3	4	5.50	-
[28]	21	10	0	3	5.65	17.57
[29]	21	12	0	3	4.8	-
[30]	21	10	0	3	5.96	-
[Proposed]	21	8	4	4	5.16	8.84

6. CONCLUSION

A 3-phase 21-level AMLI fed IM configuration employing reduced switches with a control technique is proposed in this paper. With a lesser number of switches, the reduction of CMV and THD for higher output levels is designed and simulated in the MATLAB Simulink platform. A CBSPWM method has been adopted with the PI controller in the feedback loop which is further connected to the CVS blocks to address the tradeoff between CMV and THD. The performance of the PD, POD, and APOD techniques is compared, and the results are analyzed to validate the effectiveness of the proposed approach. Among these techniques, the APOD approach demonstrates superior performance, exhibiting lower CMV and THD levels that comply with the IEEE 519 standard. The CVS blocks succeed in efficient utilization of the DC bus (8.8% more) compared to the open loop system. The recommended control technique gives control engineers a way to reduce the bearing current, shaft voltage, and undesired harmonic torque components brought on by the asymmetry of inverter outputs. It is also flexible, adaptive, and simply expandable to higher voltage levels of the VSIs. It is discovered that there are straightforward correlations between CMV, THD, levels of inverters, and CMV frequencies. Addressing these issues might greatly reduce the amount of hardware components required during the design phase.

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BIOGRAPHIES OF AUTHORS

Mamatha Narayana received a B.E degree in Electrical and Electronics Engineering from Siddaganga Institute of Techno1ogy (VTU), Tumkur, India in 2009 and M.Tech. degree in Power Electronics from REVA Institute of Technology and Management (VTU), Bangalore, India in 2013. She worked as an assistant professor at REVA University from 2014 to 2019 and currently pursuing Ph.D in UVCE, at Banga1ore University, India. Her research interests inc1ude the field of power electronics, transformer1ess inverters, mu1ti1eve1 inverters, PWM techniques. She can be contacted at email: nayak.mamtha@gmail.com

Ramesh Honnappanahalli Rajappa received bachelor's degree in E1ectrica1 Engineering from UVCE, Banga1ore University, Banga1ore, India, in 1995, M.Tech. degree in Power E1ectronics from BMSIT, Banga1ore, India in 1999, and a Ph.D. degree in E1ectrica1 Engineering from UVCE, Banga1ore University. He is current1y a professor at UVCE, Banga1ore University. His fie1d of interest inc1ude mu1ti1eve1 inverters, PWM techniques, and electric vehic1es. He can be contacted at email: nayaka.ramesh73@gmail.com.