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A level shift carrier based SPWM for reduced switch 5-level multilevel inverter topology

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ABSTRACT

Multilevel inverters (MLI) seek attention from many researchers these days for high/medium power industrial applications because their output power quality is better than 2-level inverters. This research work presents a detailed comparative analysis of multicarrier level shift (LSPWM) technique implemented on five level conventional and modified multilevel inverters in MATLAB/Simulink software. With the aim of decreasing number of gate drives, switching devices, and DC sources there is a greater focus on emerging multilevel topologies, even though majority of traditional topologies are employed in important application. MLIs have bright future in industry-focused applications, but their size, cost, device count, and switching complexity have hindered their commercial acceptance. Researchers are always creating next generation topologies, or reducing the components and switches used in (RSC) MLIs, to illustrate the shortcomings of MLIs. Conventional five level inverter uses eight semiconductor switches, eight driver circuit and suffers from switching complexity while the proposed symmetrical 5-level smart MLI topology offers reduced quantity of switching elements, gate driver circuits, low cost, space requirement, low dv/dt stress, low switching losses over the traditional topology. The effect of % output harmonic contents are analyzed with phase-disposition and phase-opposition disposition technique for different loads.

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1. INTRODUCTION

Although multilevel inverter technology is constantly being researched and developed, new multilevel inverters (MLI) topologies have recently been demonstrated, growth of such technologies has increased considerably in recent years. A multilevel inverter's primary function is to connect numerous semiconductor power switches with DC sources to create AC voltage waveform close to sinusoidal shape. MLI topologies are in demand as they provide switches with lower power ratings. Creating a staircase waveform closely as sinusoidal shape can reduce electromagnetic interference and improve harmonic performance.

These inverters are intended to achieve greater voltage levels. The three most popular and well-known inverter designs are diode clamped (DCMLI) [1], flying capacitor (FCMLI) [2], and cascaded H-bridge (CHB) [3].

Even though industry and academia have shown a great deal of interest in these topologies, their application is heavily influenced by switching complexity, cost, and application.

Power electronic devices and renewable systems employ the MLI, a DC/AC conversion technology with minimum switching losses on the switches. The quality of output voltage is measured with total harmonic distortion (THD) generated by MLI [4]-[6]. AC output voltage generated mimics a stepped voltage with the required number of levels. To generate required levels, it is essential to consider appropriate switching technique to calculate the switching pulses with least possible THD [7].

Both fundamental and high switching frequencies can be used to drive multilevel inverters [8]. Multi-carrier modulation techniques, such as phase shift PWM (PS PWM) [9], level shift PWM (LS PWM) [10], and space-vector PWM technique (SVPWM) [11], can be considered to shrink the overall harmonic distortion and provide a better output waveform. Above techniques are revived the most in the literature for improving the MLI's output waveform. Additionally, a novel PWM scheme is suggested to regulate the circuit. A novel configuration of five-level single-phase inverter topologies, supported by level shift modulation technique, presented in the paper. This new topology's main goals are to lower the inverter's size, lower costs, minimize stress on the switching stress, and increase the system's overall efficiency.

2. PROPOSED REDUCED SWITCH 5-LEVEL MLI TOPOLOGY

High power and voltage applications are in high demand, and this demand is rising quickly. Constrained factors related to system size, volume, cost, and weight are growing concurrently. This prevents low frequency bulky transformers which would have been a workable solution being effectually used in some high-power applications. Additionally, input & output voltage variation is limited by the use of low frequency transformers. Power conditioners that offer extended bandwidth for changes in input and output voltage, benefits of low weight, low cost, and controllability are therefore necessary. Because of these factors, the researchers ongoing research focuses on HV power converters. With benefits like high power quality (low THD), decreased switching loss, and decreased dv/dt stress, MLIs are a good option among the others for high-voltage applications. As revealed in Figure 1, the proposed 5-level inverter used two symmetrical Dc sources [12] and six controlled power semiconductor switches.

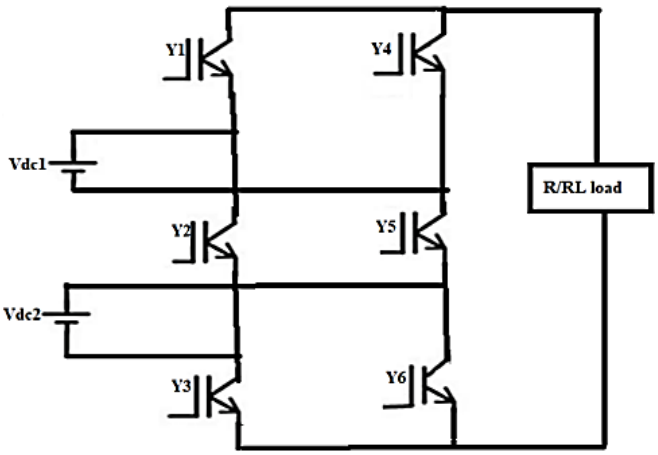


Figure 1. Proposed 5-level inverter circuit

To prevent switching loss and needless expenses, the circuit diagram shown in Figure 1 and its switching state in Table 1 (modes, level generated and output voltage at the load) have been altered. Circuit consists of complementary pairs of three semiconductor switches, Yj (j = 1 to 6), which will enhance the output waveform and lower overall harmonic distortion. The modes of operation with current path to provide the voltage of five different levels—±Vdc, ±2 Vdc, and zero—are explained in Figures 2 through 7. One such unique features is that, by setting the two dc input voltages to be equal (symmetric) or different (asymmetric), it is used as seven-level or five-level CHB MLI, respectively. One important observation during the conduction state is also that, switch Y5 always conducts in all the three modes (modes 1, 2 and 3) for generating the positive voltage with zero level and simultaneously the power semiconductor switch Y2 always conducts during negative voltage along with zero level respectively (modes 5, 6 and 7).

Operating modes of RSC MLI

- Mode 1 (0 V): Referring to the Figure 2 during this mode the switches Y4, Y5 and Y6 are turned ON producing a short circuit path with 0 Vdc.
- Mode 2 (V1dc): Figure 3 portrays path for V1dc in positive direction at the output with Y1, Y4 and Y6 switches are turned ON.
- Mode 3 (V1dc+V2dc): Figure 4 depicts the path in positive direction to add both the supply voltages V1dc+V2dc by turning ON the switches Y1, Y3 and Y5 and remaining OFF.
- Mode 4 (0 V): Figure 5 is analogous to Mode1 where the complimentary switches Y1, Y2 and Y3 are turned ON to obtain 0Vdc.
- Mode 5 (-V1dc): Figure.6. illustrates the switching path in negative direction to obtain – V1dc at load end with Y2, Y3 and Y4 switches in ON state and remaining are OFF.
- Mode 6 –(V1dc+V2dc): Figure.7 portrays the switching path in negative direction to obtain – (V1dc+V2dc) at load with Y2, Y4 and Y6 switches ON and remaining in OFF position.

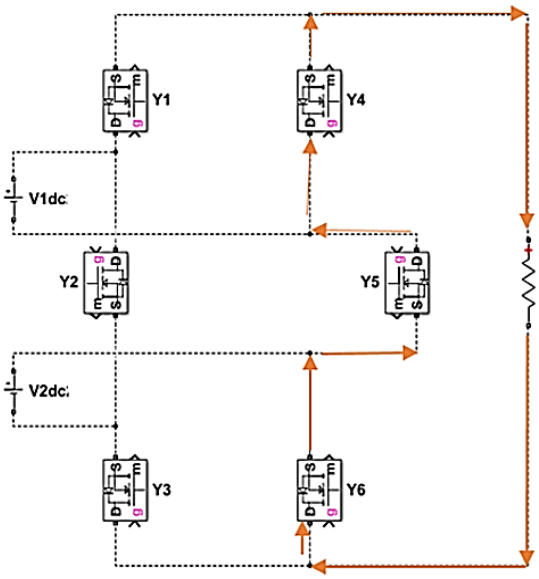


Figure 2. Mode1 (0 V)

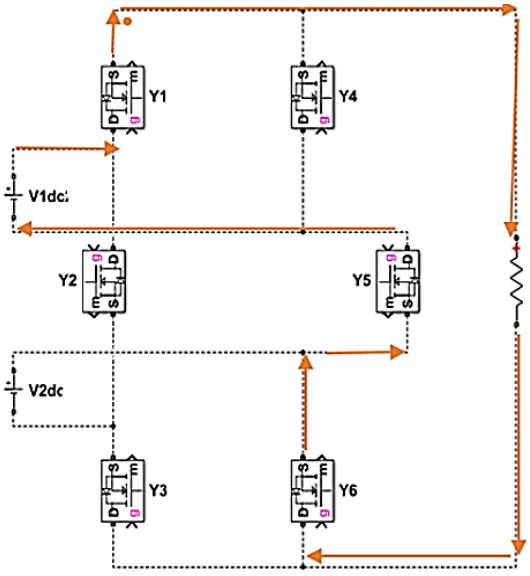


Figure 3. Mode2 (V1dc)

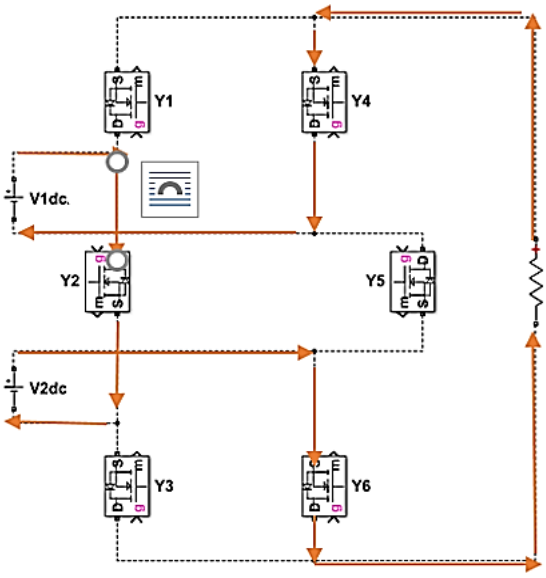


Figure 4. Mode 3 (V1dc+V2dc)

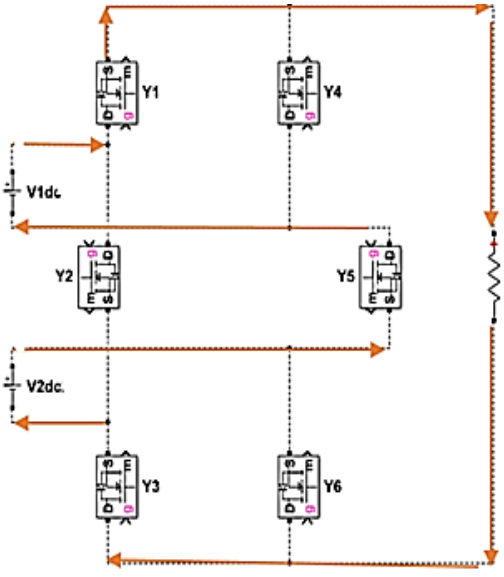


Figure 5. Mode 4 (0 V)

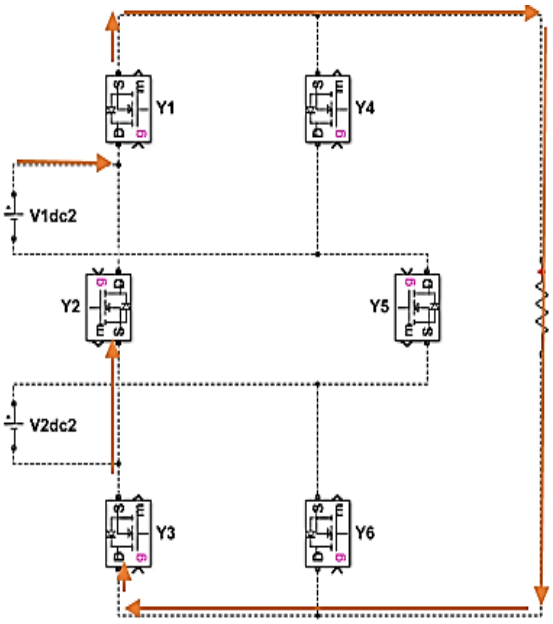


Figure 6. Mode 5 (-V1dc)

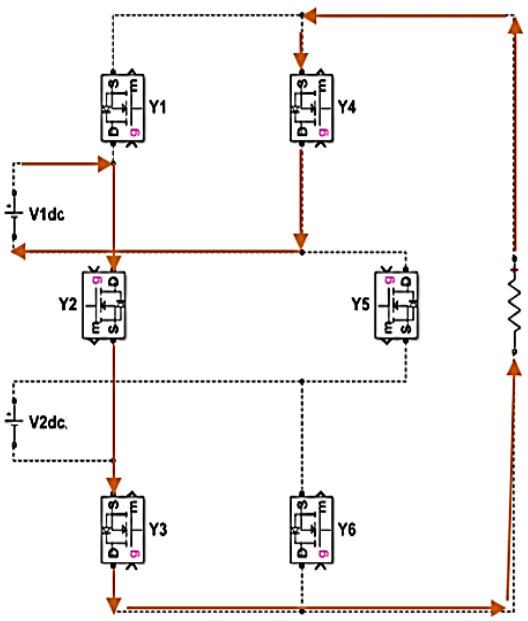


Figure 7. Mode 6 -(V1dc+V2dc)

From Figure 1, switches Y_i (i=1 to 6) operate complementarily. Let S_i be the switching function corresponding to switch Y_i defined as (1).

$$S_i = \begin{cases} 1, Yi\ is\ ON \\ 0, Yi\ is\ OFF \end{cases} \quad (1)$$

The output load terminal voltage with symmetrical dc sources is obtained as (2).

$$v_L(t) = \sum_{i=1}^{n+1}(-1)^i(1 - S_i)(Vdc_i + Vdc_{i-1}) \quad (2)$$

The voltage stress on i^{th} switch pairs can be stated as (3).

$$V_{stress,i} = Vdc_{i-1} + Vdc_i \text{ where i=1 to (n+1), with n=number of DC input} \quad (3)$$

For a symmetrical DC sources, the stress built-in by pair of switches are equal to Vdc each, whereas all other switches, build about 2Vdc respectively. Furthermore, increase in the levels and peak voltage is obtained as (4) and (5).

$$L=2n+1 \quad (4)$$

$$v_{max} = nV_{dc} \quad (5)$$

Table 1 Modes, levels, switching states and output voltage for suggested topology

Mode	Levels	Switching states (1=ON, 0=OFF)						V_{LOAD}
		Y1	Y2	Y3	Y4	Y5	Y6	
1/4	1	0	0	0	1	1	1	0
2	2	1	0	0	0	1	1	+Vdc
3	3	1	0	1	0	1	0	+2Vdc
4/1	-1	1	1	1	0	0	0	0
5	-2	0	1	1	1	0	0	-Vdc
6	-3	0	1	0	1	0	1	-2Vdc

3. METHOD

3.1. Modulation technique

Diverse forms of controlling techniques are available for multilayer inverter circuits. MLI modulation strategies has been achieved through the high-switching-frequency techniques viz. SVPWM modulation and multicarrier PWM [13], [14]. Generally, in SPWM, two signals play a vital role: one is the sinusoidal signal

and second one is the carrier signal [15]. Conversely, selective harmonic reduction and active harmonic elimination with basic frequency method and elimination are taken into consideration as techniques for low-switching frequencies [16], [17]. The current work uses a multicarrier level shift PWM scheme with in Phase disposition and phase opposition disposition. A modulated pulse width is produced based on how much reference signal or waveform differs from carrier signal. The modulating ratio M_F is $M_F = \frac{Fc}{Fm}$, where Fm-modulating frequency, Fc – carrier frequency

3.1.1. In phase disposition SPWM strategy (IPsD PWM)

Phase disposition is the method used if every carrier chosen has the same phase. The technique is generally acknowledged to result in least number of harmonics at higher modulation index. Figure 8 shows in-phase disposition preparation of PWM technique where all the carriers are at same frequencies and amplitude of Fc, Ac respectively are arranged in phase and level shifted with each other [18], [19].

3.1.2. Phase opposition disposition PWM strategy (PsOD PWM)

On the same line, phase opposition disposition is used where all carriers are at same frequency. However, triangular waves above zero axis are 180 degrees out of phase with those below zero reference as seen in Figure 9. This method assures minimum harmonics with very high frequency at higher modulation index > 0.9.

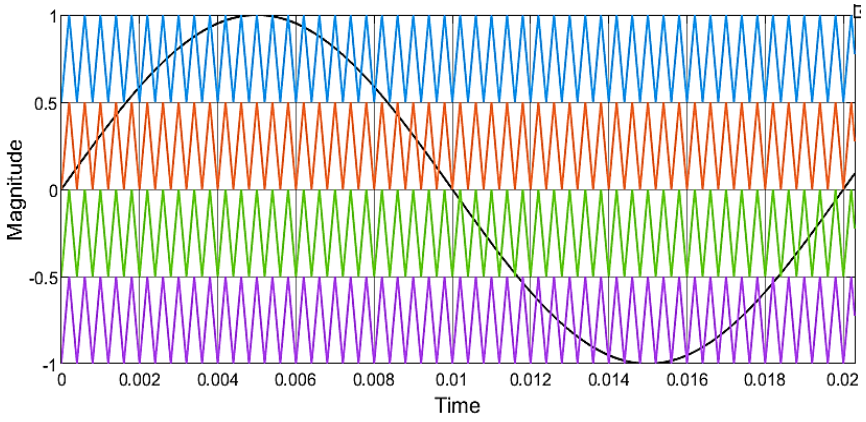


Figure 8. Arrangement of in phase disposition PWM method

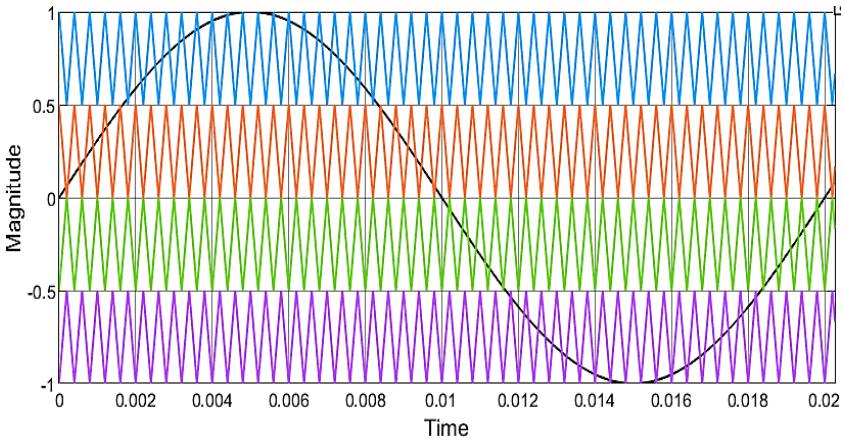


Figure 9. Arrangement of in PsOD PWM

4. RESULTS AND DISCUSSION

The proposed reduced switch five level inverter is simulated in MATLAB Simulink environment that includes two symmetrical dc source with only six switches as seen in Figure 10. The corresponding input control signals are displayed in section 3.1.1 and 3.1.2, while Figure 11 displays the schematic diagram of the modulation at 2.5 kHz. Phase opposition and phase disposition configurations/methods are derived for

generating switching pulses [19]. Reference signal assumed to be a 50 Hz sinusoidal waveform. Positive carriers are identified as being above zero reference, and negative carriers are identified as being below zero reference. There is continuous comparison between the reference and carriers. Switching pulses from logical operator are obtained by adding the signals in the manner shown in control circuit [20].

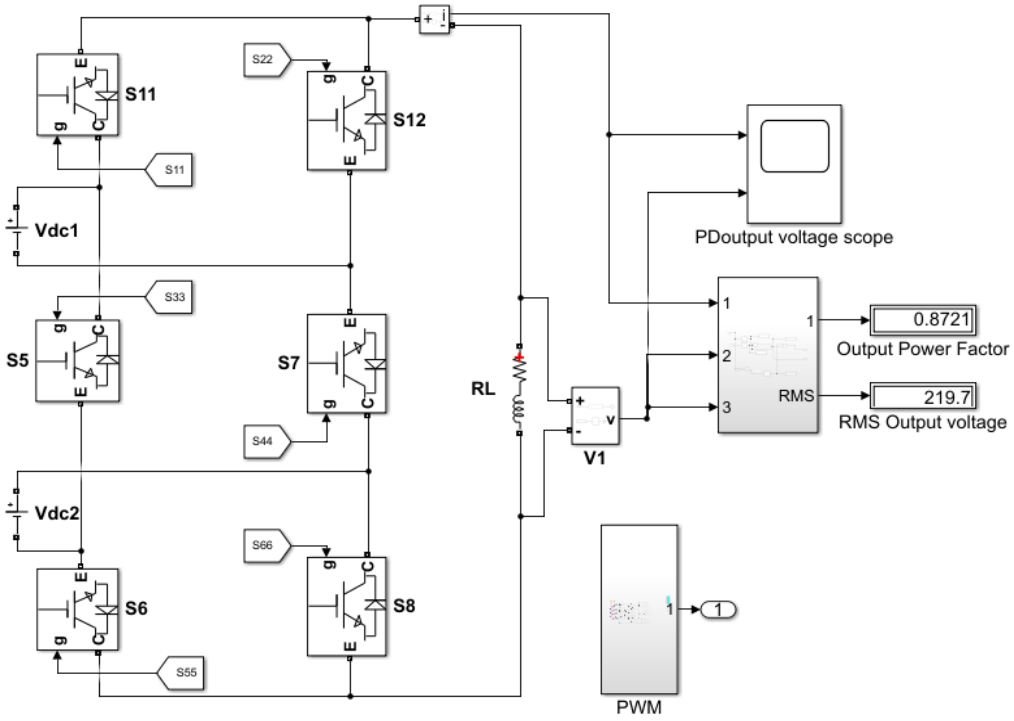


Figure 10. MATLAB Simulink model of five-level reduced switch MLI topology

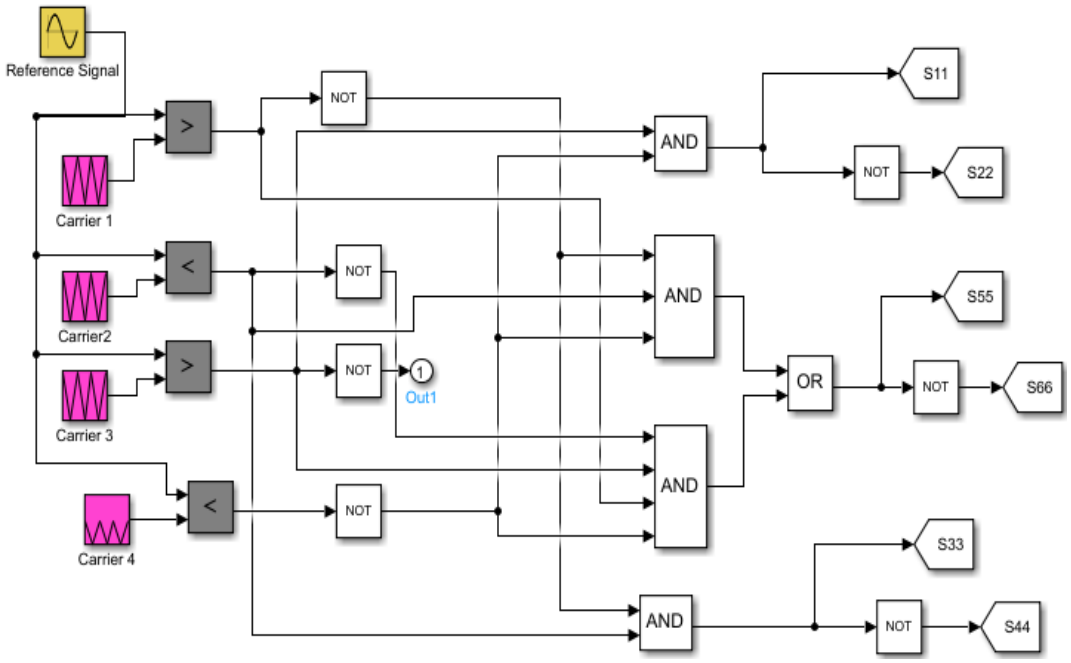


Figure 11. Proposed modified modulation scheme/control circuit

The novelty in the paper is to generate switching pulses obtained from the proposed modified modulation scheme fed to switches compared to symmetrical conventional topology [21]. Each switch is gated by AND and ORed signals to produce required level of voltage output as listed in Table 1. To assess effectiveness of suggested topology a Simulink model is developed in MATLAB/SIMULINK environment [22], [23]. The specifications of the circuit include: DC sources of 150 V each (two), switching frequency of 2.5 KHz at equal levels. Figure 12 shows pulse pattern for modulation scheme. The pulse pattern of recommended inverter circuit with equal voltage stress in all switching pairs of proposed topologies is illustrated in Figure 12(a) and Figure 12(b) that are the result of modified control scheme. The waveforms of load voltage and load current in Figure 13, with their harmonic spectrums, in Figure 13(a) through Figure 13(d) is illustrated. A phase disposition technique results in a THD of 20.68% (R-L Load) for five-level voltage waveform, which has equal steps of 150 V each. In addition, with an R–L load (R = 52 9Ω and L = 0.8 H), corresponding waveforms and its harmonic spectrum for phase-opposition disposition technique illustrated in the arrangement of PsOD PWM are presented in Figure 14(a) and Figure 14(b).

In particular, Table 2 [24] indicates that when voltage levels increase, the recommended structure has fewer components than the traditional topology. Table 3 represents the MLI component comparison with other MLI inverter circuit in terms of total harmonic distortion (Td), maximum blocking voltage (MBV), number of voltage levels (NL) and NR-not reported. It is obvious that quantity of switching devices and gate driver circuit is an important parameter that determines the cost and reliability of the inverter. Table 4, Figure 15(a) and Figure 15(b) displays simulation results for 5-level conventional MLI with proposed PsD PWM & PsOD PWM MLI [25]. These results indicate that the modified configuration uses fewer switches with lower THD at across the load voltage and current. The THD obtained by PsOD PWM technique is lower than that obtained by PsD PWM for diverse types of loads. Furthermore, with the advent of proposed topology, the overall voltage stress on all switches and diodes are same when compared to classical topologies.

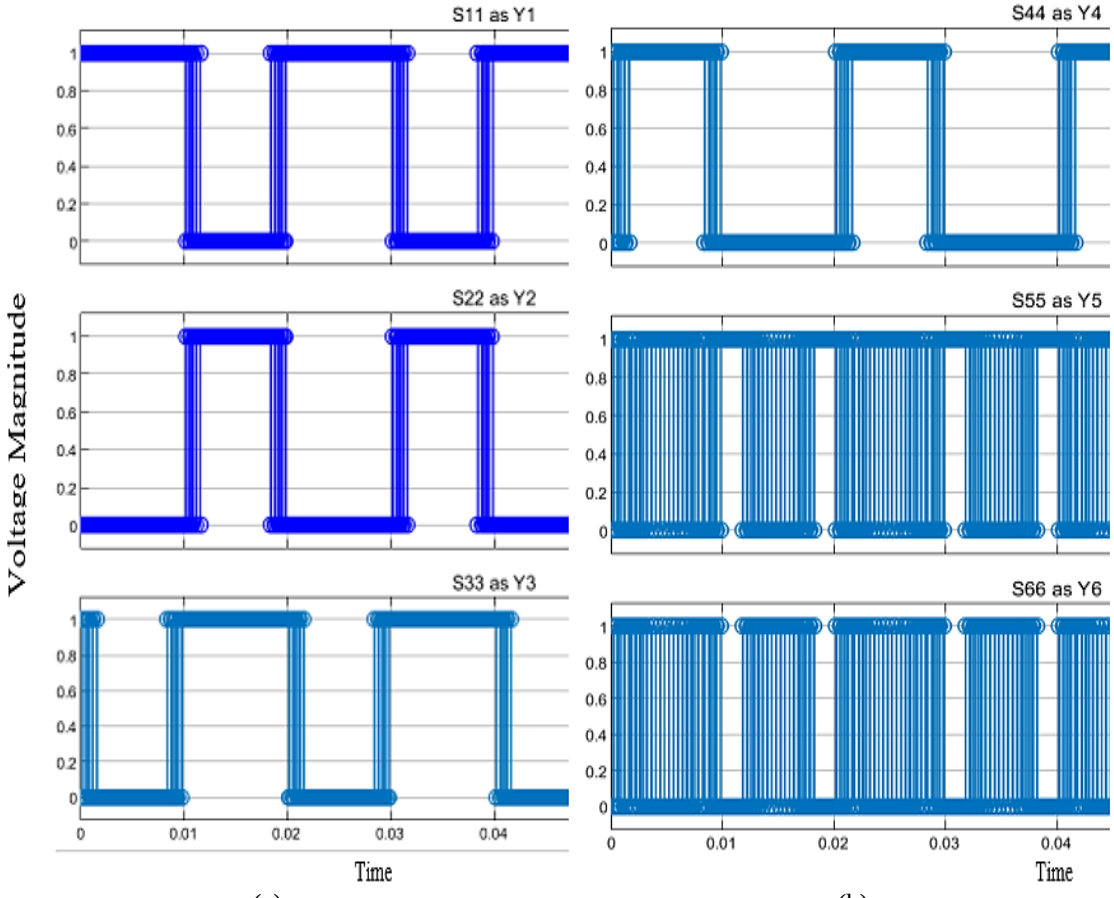


Figure. 12. Pulses generated for the switches: (a)Y1 to Y3 and (b) Y4 to Y6

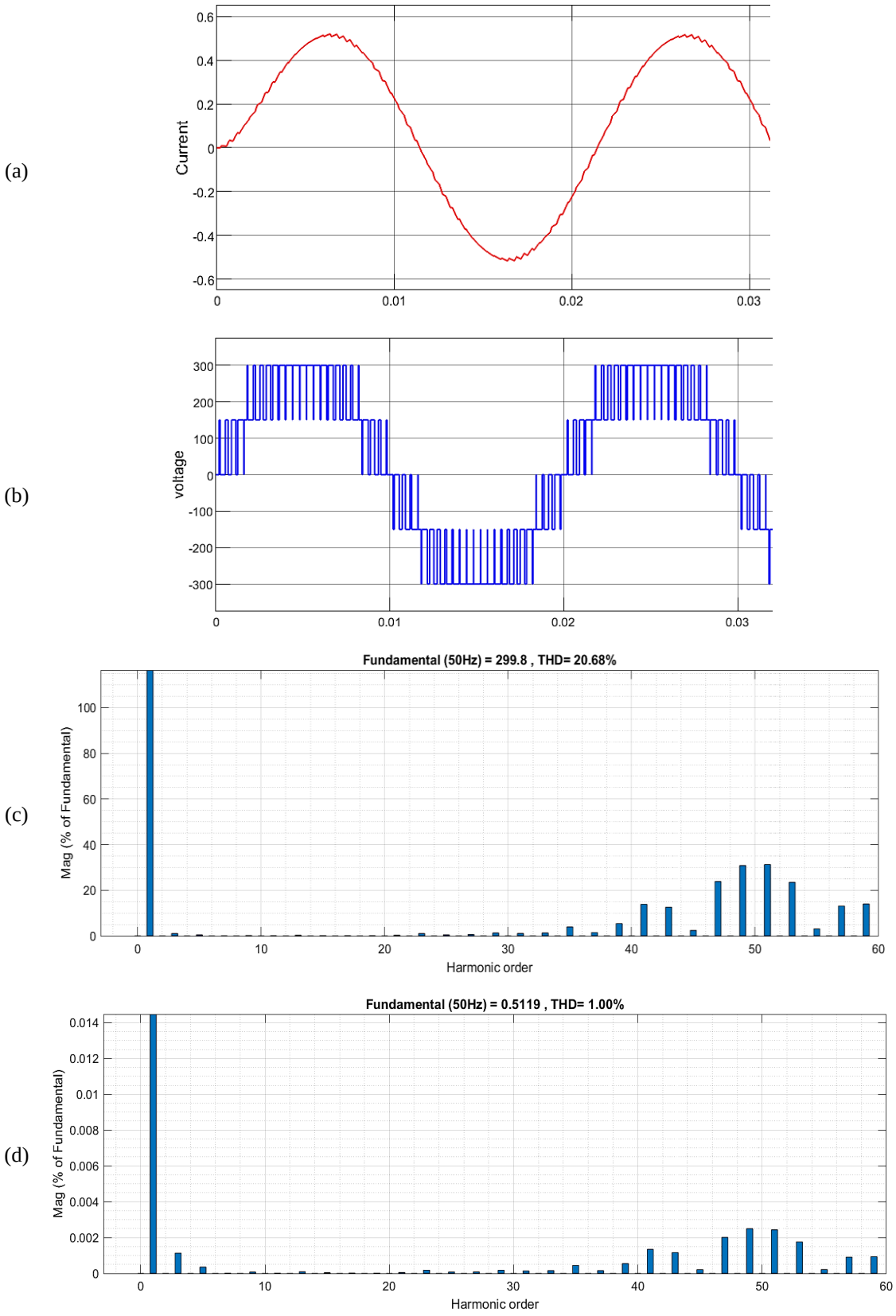


Figure 13. Simulation results of five level PsD PWM: (a) current output, (b) voltage output, (c) voltage harmonic spectrum, and (d) current harmonic spectrum [23]

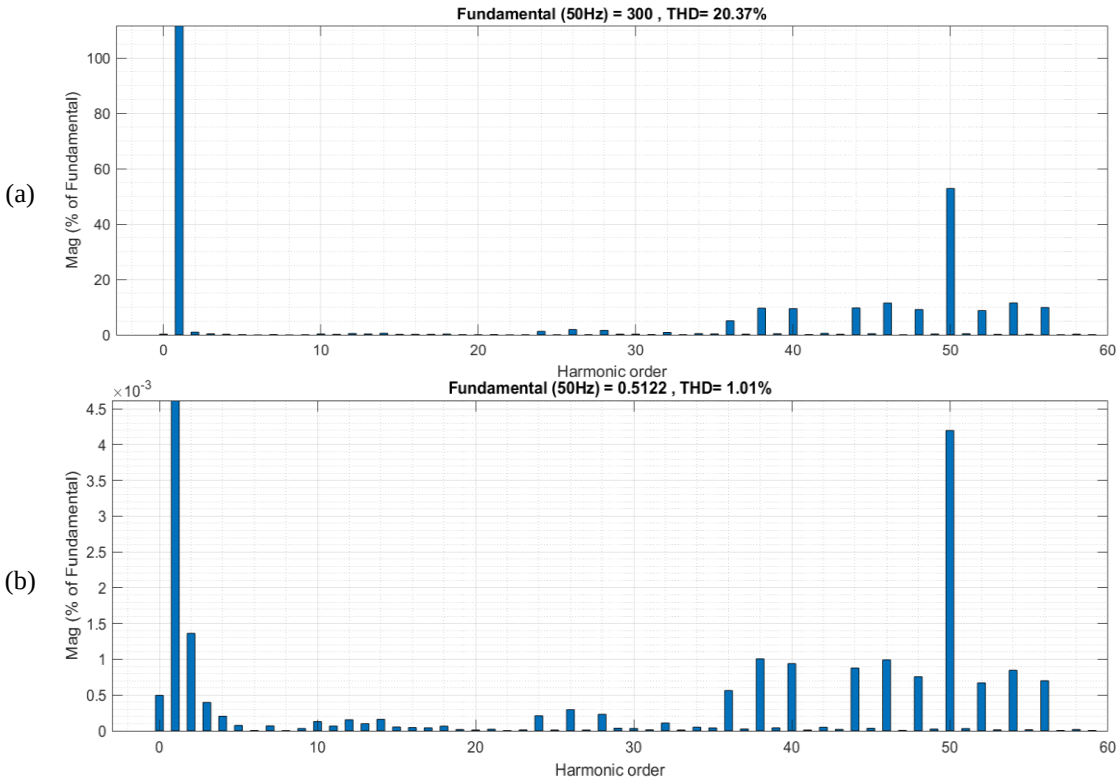
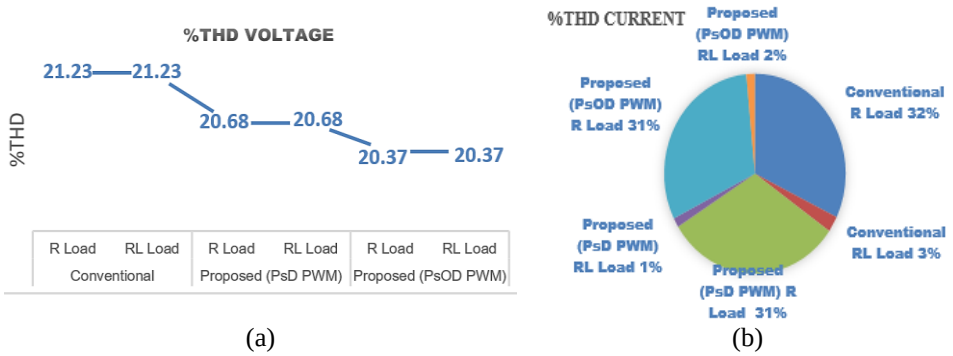


Figure 14. Simulation results of PsOD PWM: (a) harmonic spectrum of voltage and (b) harmonic spectrum of current



(a) (b)

Figure 15. Graphical representation of 5-level conventional MLI with proposed PsD PWM and PsOD PWM MLI in terms of (a) $\%V_{THD}$ and (b) $\%\ I_{THD}$

Table 2. Comparative analysis between conventional and proposed five-level inverter [24]

Parameters	Conventional	Proposed
No. of voltage sources	2	2
No. of switches	8	6
No. of gate drivers	8	6
Circuit complexity	More	Reduced

*No.-Number

Table 3. Five-level MLI component comparisons with other five-level inverter with modulation index 1

Reference	%THD	PWM technique	Symmetrical/asymmetrical
[12]	36.89	Multicarrier	Asymmetrical
[20]	21.02	Multicarrier (PsD)	Symmetrical
[22]	27.62	Multicarrier (IPD, POD, APOD)	Symmetrical
[16]	NA	Multicarrier	Both
Proposed (PsOD)	20.37	Multicarrier (PsOD)	Symmetrical
Proposed (PsD)	20.68	Multicarrier (PsD)	Symmetrical

Table 4. Comparison of THD analysis between conventional and proposed inverter topology for PsD and PsOD PWM [25]

%THD	Conventional		Proposed (PsD PWM)		Proposed (PsOD PWM)	
	R Load	RL Load	R Load	RL Load	R Load	RL Load
Voltage	21.23	21.23	20.68	20.68	20.37	20.37
Current	21.23	1.70	20.68	1.00	20.37	1.01
Output RMS value	218.8	218.8	220.1	220.1	219.7	219.7
Fundamental (50Hz)	296.9	296.9	299.8	299.8	300	300

5. CONCLUSION

Thus, the novel symmetrical reduced switch 5-level inverter has been proposed in this paper with modified modulation scheme of PsD PWM and PsOD PWM and its performance is evaluated in MATLAB environment. The focal aim is to reduce number of switching components compared to conventional topology. Only six switches are well-thought-out to produce the same 5-level output voltage. Just two voltage sources are needed to control the voltage level of output, a novel PWM control scheme with high-frequency carriers are considered and compared against a reference signal (sinusoidal) to produce workable gating pulses. The noteworthy enhancement validates the efficacy of adopting modified modulation scheme. The proposed inverter is less complex and requires fewer gate driver circuits due to its smaller size and lower switch count compared to conventional/ traditional two level or three level multilevel inverters. Thus, lower cost and reduced THD are achieved simultaneously. This is the most widely-used topology in MLI family and is widely utilized in numerous high-power medium-voltage applications; the suggested topology is excellent both technically and commercially**.**

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