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Performance analysis of fifteen level reduced device count asymmetrical multilevel inverter

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ABSTRACT

In this article, a fifteen-level reduced device count asymmetrical multilevel inverter is introduced for electric vehicle applications. This novel multilevel inverter topology minimizes the power switches required. Control of the proposed inverter is accomplished via the nearest-level control method. In a typical multilevel inverter, ten to twelve switches are used to create the fifteen levels. A high number of switches are used in traditional multilevel inverters, which increases the distortion from all harmonics, switching losses, cost, and cost per switch. Only nine switches are needed for the suggested architecture. It significantly minimizes the total harmonic distortion by 5% and lowers the switching losses, low-order harmonics, and complexity. The efficiency of the suggested multilevel inverter (MLI) is 98.35%.

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1. INTRODUCTION

Multilevel inverters have been a major technological advancement during the past decades and offer the output current and voltage waveforms at three or more levels. It synthesizes a desired alternating current (AC) output voltage waveform from a single direct current (DC) source or several DC voltage sources which may be symmetrical or asymmetrical. The multilevel inverter (MLI) uses a variety of sources, including capacitors, solar cells, and batteries. The advantages of the MLI are reduced switching loss, improved electromagnetic compatibility, higher voltage capacity, and lower harmonic [1]-[4]. The conventional multilevel inverter topologies; the most often used being the cascading H bridge, flying capacitor (FC), and diode-clamped (DC) structures [5], [6]. The majority of MLI's are hybrid structures, which are combinations of two or more fundamental multilevel structures, however alternative MLI frameworks have also been suggested [7], [8].

The diode clamped MLI construction still has a significant limitation that limits its usage in high power applications. The series H-bridge design, from which numerous variations have been derived, is the first configuration to be introduced. The most significant drawback of this arrangement is the increased need for separate voltage sources to feed every cell [9]-[11]. A MLI inverter consists of eleven switches, three capacitors, three diodes, one source, and seven levels of switched capacitors. This circuit can sustain reactive power as the capacitors in this arrangement are self-balancing. However, additional switches, diodes, and capacitors mean a

more complicated circuit overall [12]. A contemporary MLI structure that uses very few gate driver circuits and switching components has been presented. It is configured to operate in both symmetrical and asymmetrical configurations for single- and three-phase options [13]. A nine-level MLI has been presented with a reduced maximum standing voltage across the power switches. It contains one DC source, two capacitors, and eleven power semiconductor switching devices [14]. One DC supply, twenty switches, and four capacitors have been used to create a 17-level inverter. The capacitor balancing problem is easily solved by using a parallel and series strategy [15]. Ten power switches, one power diode, and two capacitors are tested in a unique nine-level of switched-capacitor two-output multilevel inverter (SCMLI) [16]. One DC source, ten transistors, four capacitors, and two diodes are needed to generate seventeen different levels [17].

In the recently developed topologies consist of more devices to develop more levels and most of the recent topologies contain capacitors. Voltage balancing problems arise when the capacitors are used to reduce DC sources and raise levels to smooth the output waveform without the need for a filter. The difficulty of sharing voltage among devices connected in series becomes evident as the output levels rise. As the number of levels and components rises, the circuit gets more intricate and costly. To address the aforementioned problems, a circuit configuration with fewer devices and no DC bus capacitors is probably the best option.

In this paper, section 2 deals with the structure of traditional MLIs, describes the operation of the proposed MLI, outlines the calculation of losses and efficiency, and describes the nearest level control technique used to control the operation of the proposed MLI, sections 3 illustrate the results and discussions of proposed MLI and section 4 concludes the proposed work. The recommended MLI structure produces fifteen levels with only nine power switches. Furthermore, for generating every level at the output voltage, a method for determining the necessary DC voltage source is suggested. The switching pulses to the implied MLI in this structure are created using the nearest-level control approach. It significantly reduces the overall harmonic distortion by fifteen levels. It reduces prices, weight, and complexity, and it produces a good quality output voltage with less total harmonic distortion (THD) which is suitable for electric vehicles.

2. METHOD

In this section,, the operations of traditional and proposed MLIs are explained along with their various operating modes. The calculations of switching losses, conduction losses, and efficiency of the recommended MLI were also elaborated. The nearest level control techniques are explained for the suggested 15-level MLIs.

2.1. Conventional multilevel inverters

The structure of the conventional MLI is shown in Figure 1(a). Each cell needs separate asymmetrical voltage sources (A_1, A_2, A_3) linked in series to produce more levels. This configuration involves twelve switches and produces a fifteen-level output voltage. In this structure, three H-bridges are involved. The second topology shown in Figure 1(b) needs ten switches to create the same 15 level output, and in this structure, there are 3 cells, each cell with one DC source and two power switching devices, this give a multilevel DC output. To produce AC waveform in the output before connecting to the load via a H-bridge circuit [18]-[20].

Figure 1(c) is the reduced switch count MLI for producing a fifteen-level output voltage or current waveform. This structure involves twelve power devices and four DC sources [21]. Figure 1(d) shows the reduced switch count MLI with ten switches and three asymmetrical DC sources [22].

2.2. Proposed multilevel inverter

The organization of the recommended MLI is in Figure 2. Three voltage sources are (V_{dc1}, V_{dc2}, V_{dc3}) connected to nine devices (S_1, S_4, S_5, S_8 are unidirectional switches and S_2, S_3, S_6, S_7, S_9 are bi-directional switches). Four are on one side of the source and the remaining five are in the right side of the three series of connected sources. Figure 3 depicts the operating modes of implied MLI for producing both positive and negative half cycles.

2.2.1. Modes of operation during a positive half-cycle

Switches S_4 and S_8 conduct, and it produce zero output voltage. Switches S_2 and S_6 conduct and produces $1V_{dc}$=30 V, it supplies to the load. Switches S_2 and S_5 conduct and produce $2V_{dc}$=60 V. Switches S_3 and S_5 conduct and produce 1 V_{dc}+2 V_{dc}=3 V_{dc}=90 V. Switches S_4 and S_7 conduct and produce 4 V_{dc}=120 V, which it supplies to the load. Switches S_4 and S_6 conduct and produce 1 V_{dc}+4 V_{dc} = 5 V_{dc}=150 V. Switches S_4, S_5, and S_9 conduct and the output voltage is 2 V_{dc}+4 V_{dc}=6 V_{dc} = 180 V. Switches S_4 and S_5 conduct, and the output voltage across the load is 1 V_{dc}+2 V_{dc}+4 V_{dc}=7 V_{dc}=210 V. The same steps will be repeated from 210 V to zero.

2.2.2. Modes of operation during a negative half-cycle

Switches S_4 and S_8 conduct, and it produces zero output voltage. Switches S_2 and S_7 conduct and produce 1 V_{dc}=-30 V, across the load. Switches S_1 and S_6 conduct and produce 2 V_{dc}=-60 V. Switches S_1 and

S_7 conduct and produce 1 V_{dc}+2 V_{dc}=-3 V_{dc}=-90 V. Switches S_3 and S_8 conduct and produce 4 V_{dc}=-120 V, which supplies to the load. Switches S_2 and S_8 conduct and produce 1 V_{dc}+4 V_{dc}=-5 V_{dc}=-150 V. Switches S_1, S_8, and S_9 conduct and the output voltage is 2 V_{dc}+4 V_{dc}=-6 V_{dc}=-180 V. Switches S_1 and S_8 conduct, and the output voltage across the load is 1 V_{dc}+2 V_{dc}+4 V_{dc}=-7 V_{dc}=-210 V. The same steps will be repeated from 210 V to zero.

The main advantages of this structure are that it has 15 levels with nine switches and three asymmetrical DC sources. The proposed MLI produces fifteen levels in the output voltage or current. The structure of the stated system is also compact and produces a lower value of THD. Electrical stresses across each switch are also less and easily controllable and expandable further to produce more levels.

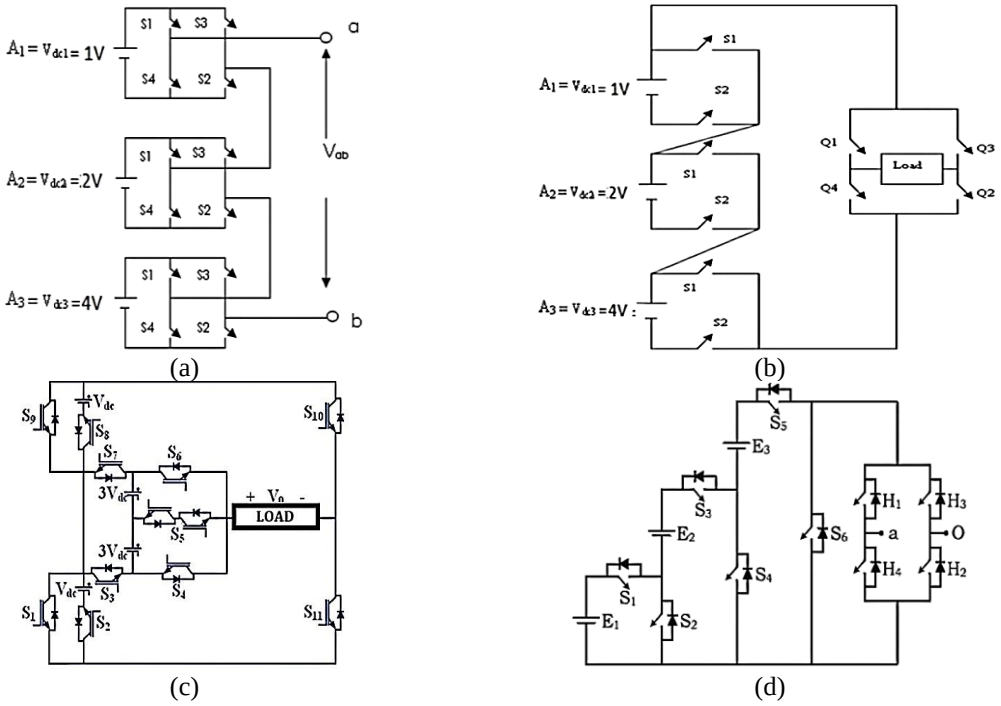

Figure 1. Conventional MLIs: (a) cascaded hybrid H-bridge [18], [19], (b) new cascaded hybrid [20], (c) MLI with twelve switches [21], and (d) MLI with ten switches [22]

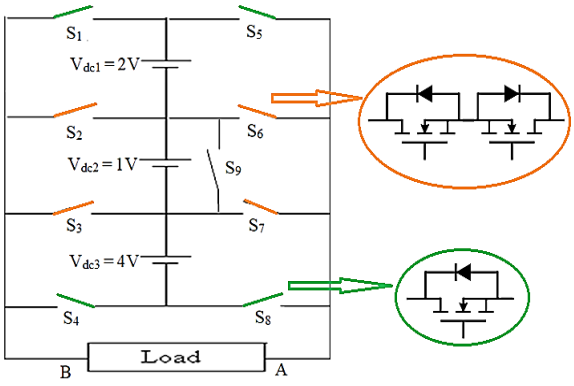

Figure 2. Proposed multilevel inverter

2.3. Estimation of loss and efficiency

This section describes the theoretical calculation of loss used to determine efficiency of recommended inverter. The most significant losses are conduction and switching losses, and its calculation is based on the assumption that load is totally resistive and that voltage available at output is staircase waveform. Conduction loss happens when MOSFET power switches are actuated and conducts electricity in a multilevel inverter. In the proposed inverter design, losses are computed individually to determine total loss during conduction. In this case, loss due to switch conduction period during the basic cycle quarter is calculated, as in (1).

$$P_{CON} = \frac{4}{\pi}\int_0^{\frac{\pi}{2}} {I_R}^2(t)\, R_{ON,}Tdt \quad (1)$$

The MOSFET's on-state resistance and load current are denoted as $R_{on}T$ and $I_R(t)$, respectively. By employing nine power switches, the proposed system provides 15 levels voltage, and the current in the load side is sinusoidal. As a result, the load current is expressed as (2).

$$I_R = I_{P,}sinwt \quad (2)$$

Using (1) and (2), the average loss of single-phase system during conduction is derived as (3).

$$P_{CON} = \frac{4}{\pi}\int_0^{\frac{\pi}{2}} {I_{P,}}^2 sin^2\, wtR_{ON,}Tdt \quad (3)$$

During the changeover from ON to OFF or vice versa, the overlapping of voltage and current produces switching loss in MOSFET power switches. The energy loss of MOSFET power switches is computed as follows throughout them on and off periods, as in (4).

$$E_{ON} = \frac{V_{ON}\times I}{6}\, T_{ON} \quad (4)$$

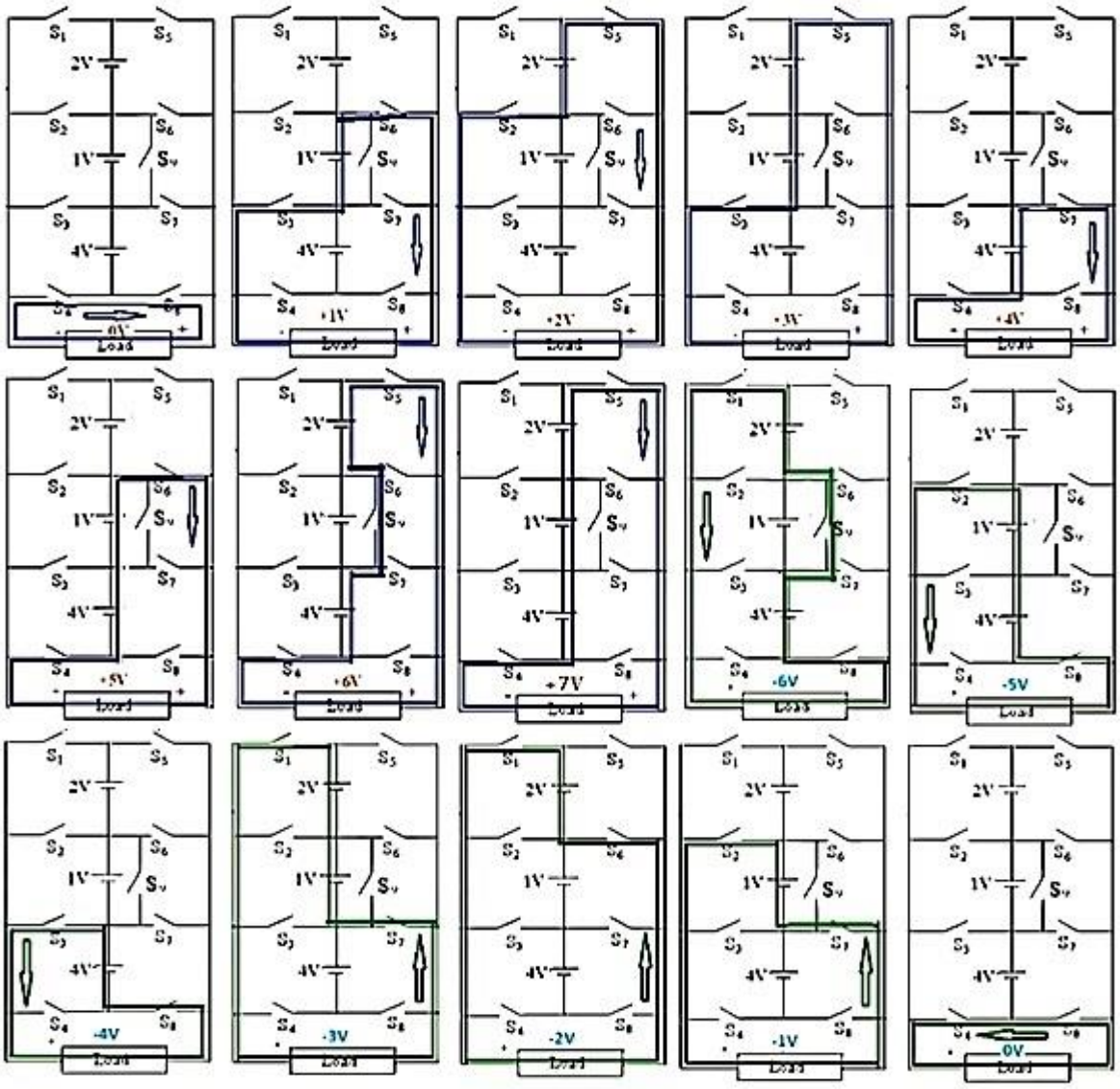

Figure 3. Operation of proposed multilevel inverter

Where V_{ON}, I, T_{ON} are the MOSFET on-state voltage, the MOSFET current after switching on and turn on time respectively, as in (5).

$$E_{OFF} = \frac{V_{OFF} \times I}{6} T_{OFF} \quad (5)$$

V_{OFF}, I_{OFF}, and T_{OFF} are the MOSFET off-state voltage, current passing through the MOSFET before it turns off, and turn-off time, respectively. The typical switching power loss in the projected configuration is find individually for each power switch by using (4) and (5), and the switching loss is determined as (6).

$$P_{SW} = 2 \times f \times (E_{ON} + E_{OFF}) = \frac{1}{3} \times f \times I \times (V_{ON} T_{ON} + V_{OFF} T_{OFF}) \quad (6)$$

The efficiency and total power loss of projected inverter are determined by using (7) and (8).

$$P_{LOSS,,TOTAL} = P_{CON} + P_{SW} \quad (7)$$

The efficiency has been calculated using (8).

$$Efficiency = \frac{P_{OUT}}{P_{out} + P_{LOSS,T}} \times 100\% \quad (8)$$

From the calculations, the conduction losses of MLI is 12.11 W, switching losses of the MLI is 0.39, input power of the MLI is 759.2 W, output power of the MLI is 746.7 W and the efficiency of the MLI is 98.35% for the resistive load of 100 Ω.

2.4. Nearest level control technique

It is possible to regulate multilevel inverters using both low-frequency and high-frequency switching techniques. A fundamental frequency switching process is employed to control the recommended topology [23]. For basic frequency switching, one can employ the selective harmonic elimination (SHE) or space vector modulation (SVM) schemes. The less appealing aspect of SVM is its control complexity. In terms of the SHE strategy, solving the equations to exactly predict the switching angles would get more difficult as the levels grow [24]. The closest level modulation approach is employed in this research [25], [26]. Figure 4 illustrates the control approach. To achieve each switching state in this manner, the fundamental frequency of the reference sine wave is compared with constants. It is necessary to compare "n" constants with the sine wave at six per unit. if the voltage waveform has "n" levels in the positive half cycle. The closest level constant must have a value between 0 and 1. Next, in order to obtain the constant that will be compared with the reference to create the subsequent level, the same constant will be added. The MOSFETs are then activated in accordance with the switching function using the pulses produced by comparing the same constants with the reference. For instance, the selected nearest level constant must be added to zero in order to create the pulses required for the switches conducting at level 1. Many researchers have concluded after study that the optimal nearest level constant will be 0.4 for low THD and lower order harmonics. One may estimate the switching for each level using (9). The nearest level constant is subtracted from 1 in the calculation to get the result of 0.6.

$$M_a = \frac{V_{ref}}{V_o} \quad (9)$$

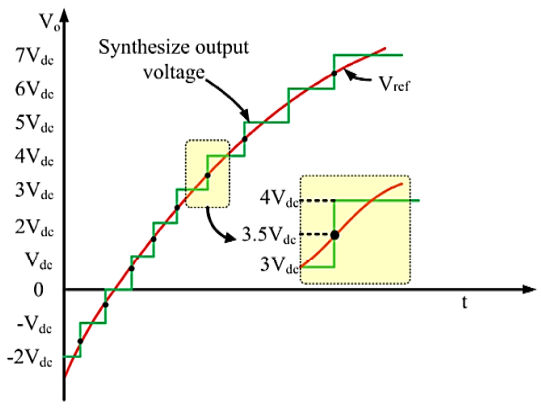

Figure 4. Nearest level control modulation technique

3. RESULTS AND DISCUSSION

The effectiveness of the recommended MLI for R-load is verified through MATLAB simulation. The Simulink model of the suggested MLI is shown in Figure 5. Three separate DC voltage sources 30 V, 60 V, and 120 V are utilized in this configuration. The 15-level output voltage waveform is achieved by using the nearest-level control method. The rms value of 15 level output voltage is 210 V for 10 kW which is shown in Figure 6. It indicates that the output voltage waveform is almost sinusoidal. Figure 7 shows the output voltage and current waveforms for an RL load of 10 kW and 750 VAR. It indicates that the output current waveform is almost sinusoidal and has a magnitude of 50 A. Figure 8 shows THD, its value is 4.89%, and THD is also within the limit of the IEEE standard of 5%.

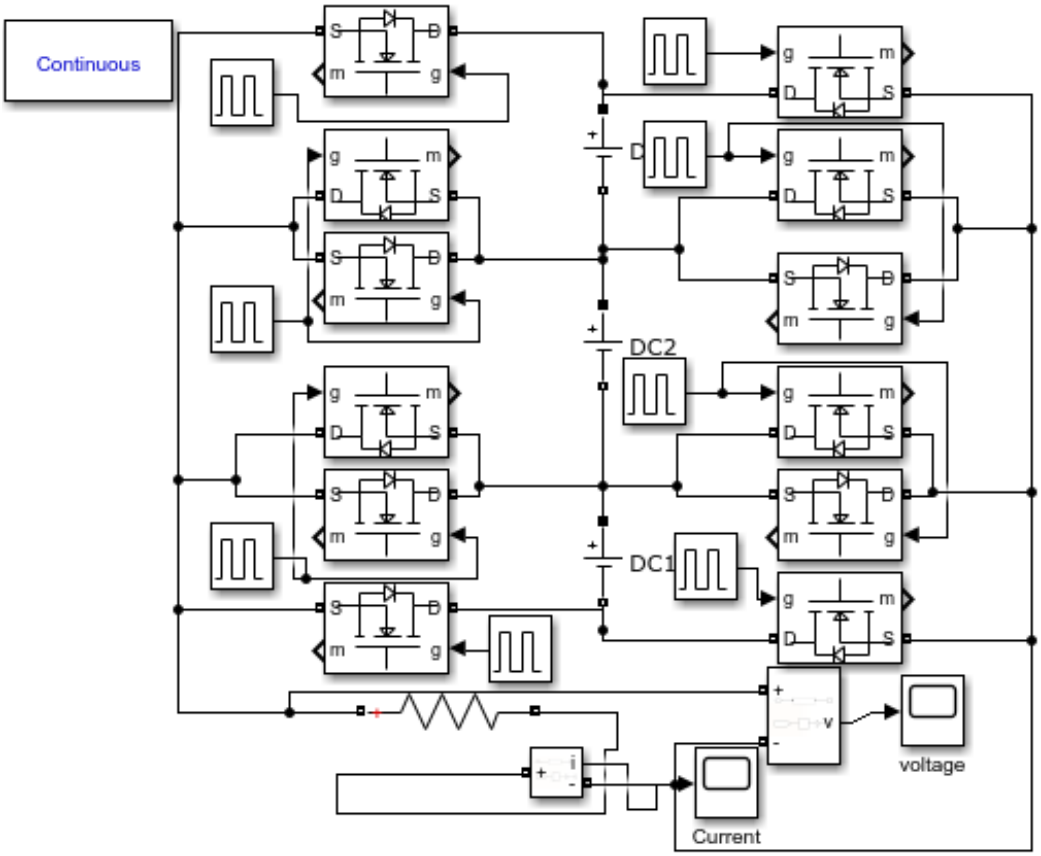

Figure 5. Simulation diagram of proposed 15 level MLI

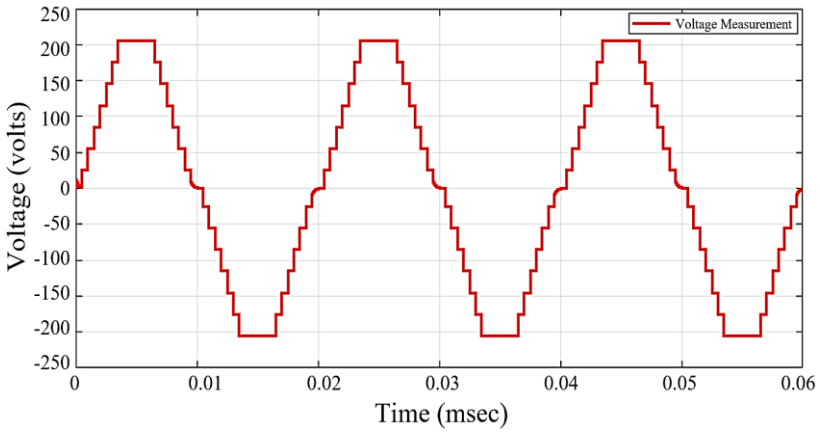

Figure 6. Output voltage waveform for 15-level

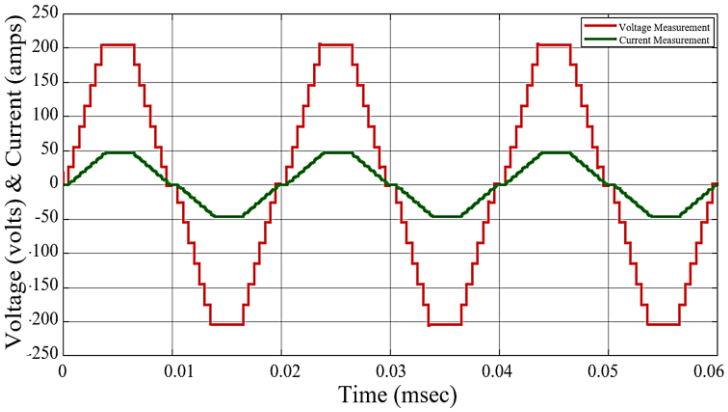

Figure 7. Output voltage and current waveform for RL load

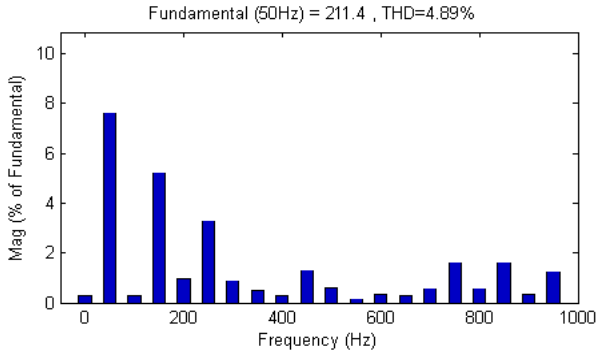

Figure 8. FFT analysis for 15-level MLI

Simulation results are verified through the hardware setup as shown in Figure 9 which consists of nine MOSFETs. There are IRF840 MOSFETs used in the hardware layout. The Arduino microcontroller generates the gate signal for inverter switches. There are three asymmetric DC sources (30 V, 60 V, and 120 V) positioned on the input side of the 15-level inverter. The suggested inverter output powers a resistive load (30 K-0.5 kw). Figure 10 shows the hardware output voltage for resistive load and Figure 11 illustrates the current waveform for the same load. The experimental THD is 4.94 % which is under the THD standard of the IEEE (5%). There are substantially fewer switches employed and a lower overall harmonic distortion when compared to the other four typical inverters shown in Table 1. Figure 12 depicts the comparison of various traditional MLIs. From these comparisons, the proposed MLI is better in terms of device utilization, gate driver circuits needed, total standing voltage per unit, cost function per level, THD, and efficiency.

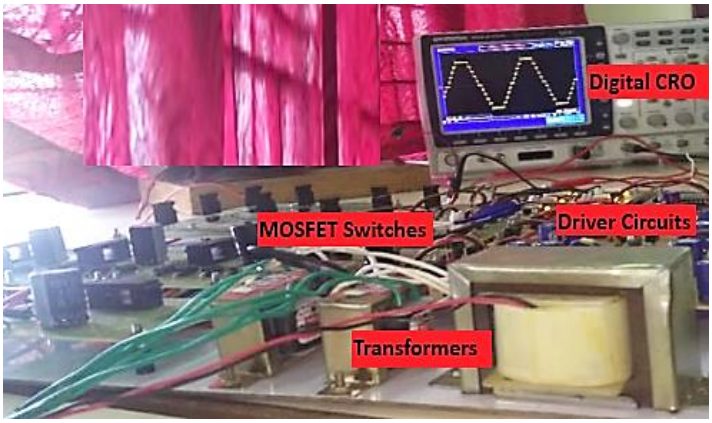

Figure 9. Experiment setup

Table 1. Comparison of traditional and proposed multilevel inverters

S.No.	Topologies	Level	N_S	N_{gd}	N_D	N_C	N_{DCS}	MBV	TSV	TSV_{PU}	$CF_{PU\ (\alpha=1)}$	THD	Efficiency
1	DCMLI	15	14	14	12	7	1	$1V_{dc}$	$28V_{dc}$	28	5.00	12.54	96.78
2	FCMLI	15	14	14	0	16	1	$1V_{dc}$	$28V_{dc}$	28	4.80	11.13	96.70
3	CHMLI	15	28	14	0	0	1	$7V_{dc}$	$28V_{dc}$	4	21.66	12.08	96.05
4	HMLI	15	12	10	0	0	3	$7V_{dc}$	$52V_{dc}$	7.43	5.20	9.12	97.60
6	[21]	15	11	11	0	0	4	$7V_{dc}$	$36V_{dc}$	5.14	7.23	5.50	98.55
7	[23]	15	10	7	0	0	3	$7V_{dc}$	$50V_{dc}$	7.43	4.89	6.3	98.60
8	Proposed MLI	15	9	7	0	0	3	$7V_{dc}$	$46V_{dc}$	6.57	4.51	4.89	98.35

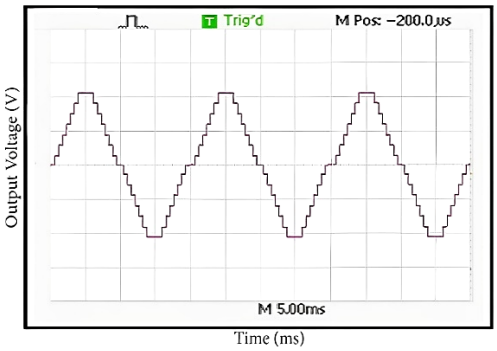

Figure 10. Hardware output voltage waveform

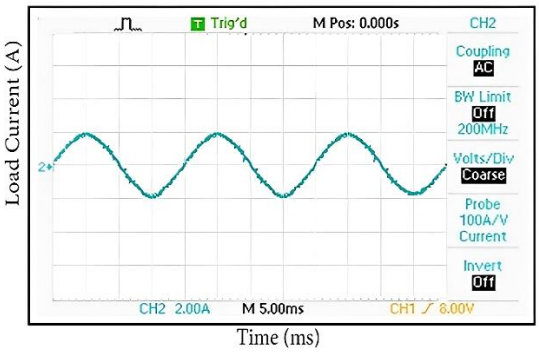

Figure 11. Hardware output current waveform

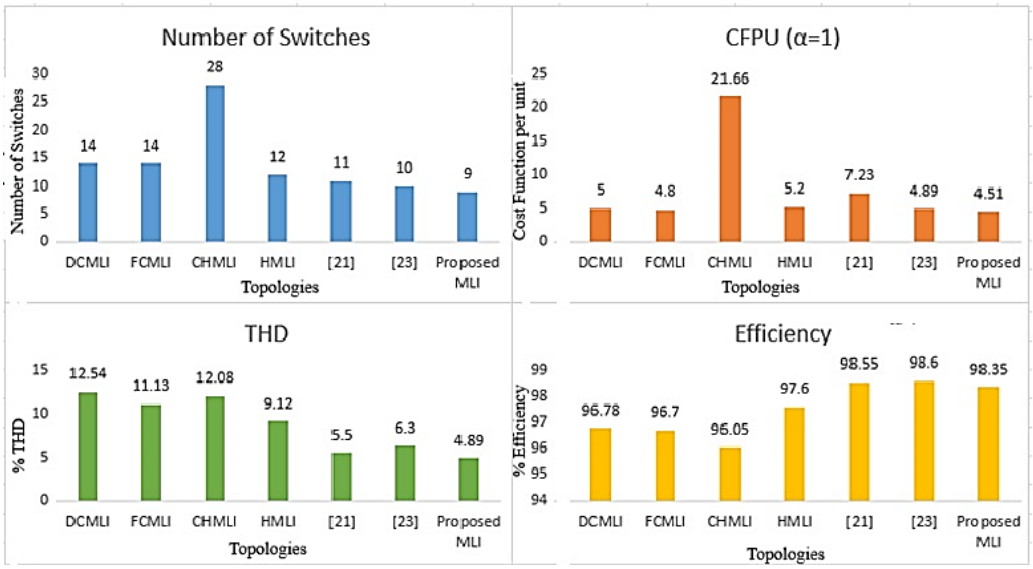

Figure 12. Comparison of various MLIs

4. CONCLUSION

This article has shown how the suggested MLI configuration works with nine switches. This MLI structure and its basic functions have been discussed. A method for calculating the switches required in relation to the necessary output level was also covered. In the traditional system, the number of switches needed rose along with the levels. Because there are a lot of power semiconductor switches involved, there is an increase in harmonics, switch losses, cost, and distortion of all harmonics. For 15 levels, the suggested configuration drastically lowers the power consumption of semiconductor switches, efficiency is 98.35%. The MLI's overall complexity is less, and cost function per level is 4.89 and THD is 4.51% which comes under the standard of IEEE 5%. Hence, this proposed structure is most suitable for EV applications.

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