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Determination of minimal total harmonic distortion for single-phase multilevel inverter

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ABSTRACT

Multilevel inverters (MLIs) offer numerous advantages, such as low voltage stresses on power switches, low switching losses, and high efficiency. Switching angles applied to MLI must be selected carefully to generate an output voltage waveform with low total harmonic distortion (THD). This paper proposes an improved algorithm to determine the switching angles with low THD for MLI. The proposed algorithm has been implemented using a MATLAB script to compute a set of switching angles with low THD from 3-to 31-level cascaded H-bridge MLI (CHBMLI). A PSIM simulation model has been developed to validate the switching angles and the corresponding THDs obtained from the MATLAB script. An experimental prototype has also been developed to validate the simulation results. The results obtained from the MATLAB script, the PSIM simulation, and the experimental measurement are in good agreement.

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1. INTRODUCTION

Multilevel inverters (MLIs) have gained popularity in medium-to-high voltage and power applications [1]. It offers several advantages, such as low voltage stresses on power switches, low switching losses, and high efficiency [2]-[7]. Many MLI topologies have been reported in the literature, such as neutral point clamped MLI, flying capacitor MLI, cascaded H-bridge MLI, switched capacitor MLI, E-cell MLI, and T-type MLI [8]-[11]. Among these MLI topologies, cascaded H-bridge MLI (CHBMLI), which has a better modular structure, is therefore more versatile and has been applied in many applications [12].

Switching angles applied to MLI must be carefully selected in order to obtain an output voltage waveform with low total harmonic distortion (THD). Selective harmonic elimination pulse width modulation (SHEPWM) is one of the switching-angle calculation techniques. In SHEPWM, a set of non-linear transcendental equations is required to be solved simultaneously [13]-[15]. Several techniques can be used to solve these equations such as Newton-Raphson (NR) method, genetic algorithm (GA), and particle swarm optimization (PSO) [16]-[20]. Although SHEPWM is able to eliminate selected undesired harmonics, it may not guarantee to obtain a low THD.

Espinosa [21] proposes an algorithm to determine the minimal THD. However, only up to 15-level MLI results are presented. For applications that require lower THD operations, MLI with a higher number of output voltage levels is desired [22]. Luo [23] presents the minimal THD results up to 31-level MLI. However, the algorithm to obtain those results is not described. To bridge the gap, this paper aims to extend the work proposed

in [21] up to 31-level MLI. As will be pointed out in section 3, the algorithm presented in [21] requires a very high computational time when the number of output voltage levels is high. To address the aforementioned drawback, an improved algorithm is proposed in this work. The results will be compared to those obtained in [21] and [23]. Besides, the results will also be validated through simulation and experiment.

2. CASCADED H-BRIDGE MULTILEVEL INVERTER

CHBMLI can be constructed using a combination of dc sources and power switches [24]. Figure 1 illustrates an 11-level CHBMLI. Each basic cell module consists of one dc source and four power switches. The CHBMLI can be easily extended to a higher number of output voltage levels by adding more series-connected basic cell modules. By way of example, a 21-level CHBMLI can be achieved with an additional five series-connected basic cell modules.

Assume that all dc sources with similar voltage ratings are used in Figure 1 (Vdc1 = Vdc2 = Vdc3 = Vdc4 = Vdc5 = Vdc). Table 1 summarizes the switching states to generate an output voltage waveform of an 11-level CHBMLI [25]. Note that "1" indicates that the power switches are in the ON state, while "0" indicates that the power switches are in the OFF state.

Figure 2 shows the output voltage waveform of the 11-level MLI. A set of switching angles, denoted as α_1 , α_2 , α_3 , α_4 , and α_5 , are required to generate the voltage waveform. It is important that the switching angles need to be selected properly in order to obtain an output voltage waveform with low THD.

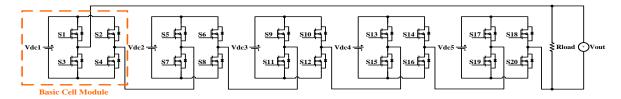


Figure 1. 11-level CHBMLI

Table 1. Out	but voltage and corre	sponding switching	states of 11-level CHBMLI

				0					-	0		0		_						
Output voltage (Vout)										Po	wer s	witch	es							
Output voltage (vout)	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18	S19	S20
+5Vdc	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
+4Vdc	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	1	0	0
+3Vdc	1	0	0	1	1	0	0	1	1	0	0	1	1	1	0	0	1	1	0	0
+2Vdc	1	0	0	1	1	0	0	1	1	1	0	0	1	1	0	0	1	1	0	0
+Vdc	1	0	0	1	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
-Vdc	0	1	1	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
-2Vdc	0	1	1	0	0	1	1	0	1	1	0	0	1	1	0	0	1	1	0	0
-3Vdc	0	1	1	0	0	1	1	0	0	1	1	0	1	1	0	0	1	1	0	0
-4Vdc	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	1	1	0	0
-5Vdc	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
Note: "1" indicates ON	l stat	e an	d "0'	" ind	icate	s Ol	FF st	ate												

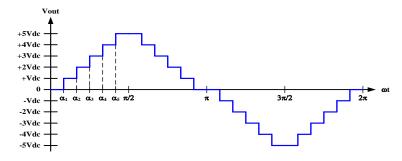


Figure 2. Output voltage waveform of 11-level MLI

3. PROPOSED IMPROVED ALGORITHM

As stated in section 1, Espinosa [21] proposes an algorithm to determine the switching angles with low THD for MLI. The algorithm evaluates the THDs of a series of switching-angle set (e.g. a_1 , a_2 , a_3 , ..., a_k).

It is worth to note that the switching angles must fulfil the condition of $0 < \alpha_1 < \alpha_2 < ... < \alpha_k < \frac{\pi}{2}$, where k is the number of switching angles. Figure 3 shows the flowchart of the algorithm presented in [21]. One of the key parameters in the algorithm is the increment (INC) steps, and in [21], the INC steps are set as 6° , 1° , and 0.1° .

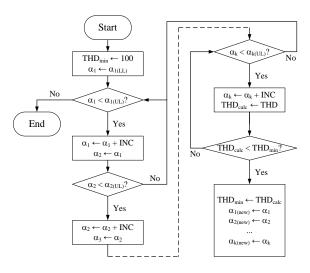


Figure 3. Flowchart of [21] algorithm

While the algorithm is able to determine the switching angles with low THD, only THDs up to 15-level are reported in [21]. Since a higher number of output voltage levels is required to generate an output voltage waveform with lower THD, it is worthwhile to extend the work in [21] to higher numbers of output voltage levels. However, the algorithm proposed by [21] can be very time-consuming when applied to calculate the THD for higher number of output voltage levels.

To address the aforementioned limitation, an improved algorithm is proposed in this paper. Instead of using INC: 6° , 1° , and 0.1° , the proposed algorithm uses new INC steps, which are 14° , 6° , 2° , 1° , 0.8° , 0.4° , 0.2° , and 0.1° , to calculate the THDs of up to 31-level MLI. In this work, the THDs are computed using (1).

THD =
$$\frac{\sqrt{\frac{\pi^2 k^2}{8} - \frac{\pi}{4} \sum_{i=0}^{k-1} (2i+1) \alpha_{i+1} - \left(\sum_{i=1}^{k} \cos(\alpha_i)\right)^2}}{\sum_{i=1}^{k} \cos(\alpha_i)}$$
(1)

The pseudo code of the proposed algorithm is shown in Table 2. As can be seen in the table, THD_{min} is the minimal THD, THD_{calc} is the calculated THD, α_i is the i-th switching angle, $\alpha_{i(new)}$ is the new i-th switching angle that results in minimal THD, $\alpha_{i(UL)}$ is the i-th upper switching angle limit, and $\alpha_{i(LL)}$ is the i-th lower switching angle limit. At the first run of the algorithm, the THD_{min} is set to 100%. For each loop in the first run, a set of switching angles is obtained and is used to calculate the THD using (1). The THD_{calc} is then compared with the THD_{min} , and the lower THD value will be selected as the new THD_{min} at the end of the first run, the switching-angle ($\alpha_{i(new)}$) set that results in the minimum THD will be selected. The new upper and lower limits of switching angles are then computed using (2) and (3), respectively. Note that the obtained upper and lower limits of the switching angles will be used as the boundary of each switching angle in the following run.

$$\alpha_{i(\text{UL})} = \alpha_{i(\text{new})} + \frac{\text{INC}}{2} \tag{2}$$

$$\alpha_{i(\text{LL})} = \alpha_{i(\text{new})} - \frac{\text{INC}}{2}$$
 (3)

Table 2. Pseudo code for proposed algorithm

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No.	Proposed improved algorithm	No.	Proposed improved algorithm
1.	Initialize THD _{min,} $\alpha_{i(LL)}$, $\alpha_{i(UL)}$	6.	$THD_{min} = THD_{calc}$ and $\alpha_{i(new)} = \alpha_i$
2.	For INC = $[14^{\circ} 6^{\circ} 2^{\circ} 1^{\circ} 0.8^{\circ} 0.4^{\circ} 0.2^{\circ} 0.1^{\circ}]$	7.	End If
3.	For $\alpha_i = \alpha_{i(LL)}$: INC: $\alpha_{i(UL)}$	8.	End For
4.	Calculate THD _{calc}	9.	Calculate $\alpha_{i(LL)}$ and $\alpha_{i(UL)}$
5.	$If THD_{calc} < THD_{min}$	10.	End For

4. RESULTS AND DISCUSSIONS

The proposed algorithm has been implemented using a MATLAB script and is executed on a computer with the following specifications: Intel Core i7 3rd Gen, 3.40 GHz CPU, and 16 GB of RAM. Table 3 compares the total number of THD calculations and computational time for 3- to 31-level MLI using the [21] algorithm (denoted as MESP) and the proposed algorithm (denoted as PROPOSED). Figure 4 shows the graph of total number of THD calculations and computational time against the number of output voltage levels. Note that TN-MESP, TN-PROPOSED, CT-MESP, and CT-PROPOSED in Figure 4 represent the total number of THD calculations using the MESP method, total number of THD calculations using the PROPOSED method, computational time using the MESP method, and computational time using the PROPOSED method, respectively. As can be observed in Figure 4, as the total number of THD calculations increases, the computational time of the MESP method increases drastically, especially from 21- to 25-level. As shown in Table 3 and as will be shown in Table 4, the PROPOSED method requires less than 2 seconds to obtain the minimal THD for 25-level, while the MESP method requires more than 3 days. The computational times for 27- to 31-level are not provided because 27-level, for example, is expected to take 32 days to complete the computation, while 29- and 31-level are respectively estimated to take 10 and 100 times that of 27-level. Hence, these computations, which are deemed impractical to implement, are not carried out in this work.

Table 3. Total number of THD calculations and computational time for 3- to 31-level MLI using MESP and PROPOSED methods

	Total number of THD calcula		Computational time (s)	
m	MESP	Proposed	MESP	Proposed
3	33	28	0.01	0.01
5	290	93	0.02	0.02
7	2,354	291	0.02	0.02
9	20,102	860	0.03	0.03
11	189,486	2,652	0.06	0.04
13	1,916,342	7,862	0.32	0.05
15	20,388,234	26,700	2.15	0.05
17	217,856,543	62,499	20.49	0.11
19	2,381,504,315	214,478	217.66	0.14
21	26 billion	571,143	2465.25	0.17
23	286 billion	2,104,852	29068.22	0.40
25	3.142 trillion	6,651,704	282044.23	1.09
27	Estimated to be more than 34 trillion	17,666,992	Estimated to be more than 32 days	2.78
29		44,271,908	-	7.43
31		115,420,731		21.41

Table 4 compares the switching-angle sets and their corresponding THD for 3- to 31-level MLI obtained using MESP, algorithm in [23] (denoted as MFLL), and PROPOSED methods. As shown in the table, the PROPOSED method can obtain a THD that is the same or lower than the MESP (from 3- to 25-level) and MFLL (from 3- to 31-level) methods. Besides, it is worth to point out that the MESP method cannot always guarantee to obtain minimal THD. By way of example, for 21-level MLI, the PROPOSED method obtains a THD of 3.78722 %, which is similar to the MFLL method (3.78734 %), while the THD of MESP is 4.32258 %, which is much higher than the MFLL method as well as the PROPOSED method. Table 5 shows the THDs and the THD difference between each adjacent level from 3- to 31-level MLI computed from the proposed algorithm. The THD difference is computed using (4).

$$THD_{diff} = THD_{m-2} - THD_m; m \neq 3$$
(4)

where THD_{diff} is the THD difference between each adjacent level, and THD_m and THD_{m-2} are the THD of m and (m-2) number of output voltage levels, respectively. As can be observed in Table 5, the THD difference between each adjacent level decreases gradually as the number of output voltage levels increases. By way of example, the THD is reduced by 12.54220 % when the number of output voltage levels increases from 3- to 5-level, and the THD is reduced by 0.17647 % when the number of output voltage levels increases from 29- to 31-level. With the aid of MATLAB curve fitting tool, the relationship between the estimated minimal THD (THD_{est}) and the number of output voltage levels (m), can be estimated using (5).

$$THD_{est} = 72.40e^{-0.45m} + 11.15e^{-0.05272m}$$
(5)

Figure 5 compares the THD data points used for the curve fitting and the THDs computed using (5), while the goodness of fit of the curve fitting are summarized in Table 6. As shown in the table, (5) has the following goodness of fit: SSE = 0.4655, R-square = 0.9993, adjusted R-square = 0.9992, and RMSE = 0.2057.

A PSIM simulation model has been developed to validate the switching angles and the corresponding THDs obtained from the MATLAB script. Besides, an experimental prototype has also been developed to validate the simulation results. Figure 6 shows the experimental setup for an 11-level CHBMLI. The dc source voltages and the resistive load used in both simulation and experimental setup are 10 V and 50 Ω , respectively. The simulation and experimental results of the output voltage waveform and the harmonic spectrum for the 11-level CHBMLI are shown in Figure 7 and Figure 8, respectively.

The theoretical (theo) (obtained from MATLAB script), simulation (sim), and experimental (exp) THD and fundamental voltage (V_1) for 7-, 9-, and 11-level CHBMLI are summarized and compared in Table 7. The percentage errors for THD and V_1 between the theoretical and simulation results, and the simulation and experimental results are also summarized and compared in the table. As can be seen in the table, the percentage errors for both THD and V_1 are less than 1%, suggesting that the theoretical, simulation, and experimental results are in good agreement.

Table 4. Switching-angles sets and corresponding THD for 3- to 31-level MLI using MESP MELL, and PROPOSED methods

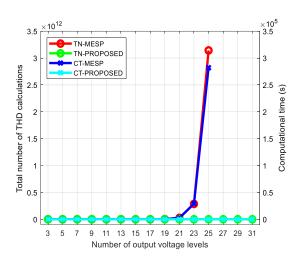
	using MESP, MFLL, and PROPOSED methods																
***	Mathada	THD (0/)						5	Switch	ing an	gles (°	")					_
m	Methods	THD (%)	α_1	α_2	α_3	α_4	α_5	α_6	α_7	α_8	α,9	α_{10}	α_{11}	α_{12}	α_{13}	α_{14}	α_{15}
3	MESP	28.96359	23.2														
	MFLL	28.96359	23.2														
	PROPOSED	28.96359	23.2														
5	MESP	16.42139		41.8													
	MFLL	16.42139	12.8	41.8													
	PROPOSED	16.42139	12.8	41.8													
7	MESP	11.53016	8.9	27.6	50.5												
	MFLL	11.53016	8.9	27.6	50.5												
	PROPOSED	11.53016	8.9	27.6	50.5												
9	MESP	8.90240	6.8	20.8	36.2	55.8											
	MFLL	8.90240	6.8	20.8	36.2	55.8											
	PROPOSED	8.90240	6.8	20.8	36.2												
11	MESP	7.25726	5.5	16.7	28.6	42.1	59.5										
	MFLL	7.25726	5.5	16.7	28.6	42.1	59.5										
	PROPOSED	7.25726	5.5	16.7	28.6	42.1	59.5										
13	MESP	6.12902	4.6	13.9	23.7	34.2	46.3	62.1									
	MFLL	6.12909	4.6	14.0	23.7	34.2	46.3	62.2									
	PROPOSED	6.12902	4.6	13.9	23.7	34.2	46.3	62.1									
15	MESP	5.30621	4.0	12.0	20.3	29.0	38.6	49.7	64.3								
	MFLL	5.30621	4.0	12.0	20.3	29.0	38.6	49.7	64.3								
	PROPOSED	5.30621	4.0	12.0	20.3	29.0	38.6	49.7	64.3								
17	MESP	4.67937	3.5		17.7		33.2			65.9							
	MFLL	4.67937	3.5	10.5	17.7	25.2	33.2	42.0	52.3	65.9							
	PROPOSED	4.67937	3.5	10.5	17.7	25.2	33.2	42.0	52.3	65.9							
19	MESP	4.18606	3.1	9.4	15.7	22.3	29.2	36.7	44.9	54.5	67.3						
	MFLL	4.18610	3.1	9.4	15.8	22.3	29.2	36.7	44.9	54.5	67.3						
	PROPOSED	4.18606	3.1	9.4		22.3					67.3						
21	MESP	4.32258	2.9	8.8	14.7	20.9	27.3	34.0	41.5	49.8	59.9	78.5					
	MFLL	3.78734	2.8	8.5	14.2	20.1	26.2	32.6	39.5	47.3	56.4	68.5					
	PROPOSED	3.78722	2.8	8.5	14.2	20.1	26.2	32.6	39.6	47.3	56.4	68.6					
23	MESP	3.45807	2.6	7.7	12.9	18.2	23.7	29.4	35.4	42.0	49.3	57.9	69.5				
	MFLL	3.45809	2.6	7.7	12.9	18.2	23.7	29.4	35.4	42.0	49.3	58.0	69.5				
	PROPOSED	3.45806	2.6	7.7	12.9	18.2	23.7	29.4	35.5	42.0	49.3	58.0	69.6				
25	MESP	3.18205	2.3	7.1	11.8	16.7	21.6	26.8	32.2	37.9	44.1	51.1	59.3	70.4			
	MFLL	3.18205	2.3	7.1	11.8	16.7	21.6	26.8	32.2	37.9	44.1	51.1	59.3	70.4			
	PROPOSED	3.18205	2.3	7.1	11.8	16.7	21.6	26.8	32.2	37.9	44.1	51.1	59.3	70.4			
27	MESP																
	MFLL	2.94672	2.2	6.5	10.9	15.4	19.9	24.6	29.5	34.6	40.1	46.0	52.7	60.6	71.2		
	PROPOSED	2.94672	2.2	6.5	10.9	15.4	19.9	24.6	29.5	34.6	40.1	46.0	52.7	60.6	71.2		
29	MESP																
	MFLL	2.74431	2.0	6.1	10.1	14.3	18.5	22.8	27.2	31.9	36.8	42.0	47.7	54.1	61.7	71.9	
	PROPOSED	2.74431	2.0	6.1							36.8						
31	MESP																
	MFLL	2.56785	1.9	5.7	9.5	13.3	17.2	21.2	25.3	29.6	34.0	38.7	43.7	49.2	55.3	62.6	72.5
	PROPOSED	2.56784	1.9	5.7	9.5						34.0						72.6
	I VOLOPED	2.30/64	1.9	٥.1	9.3	13.3	1/.2	41.4	۷٥.٥	∠9.0	J4.U	30.7	45./	47.2	JJ.3	02.7	12.0

Table 5. THDs and THD differences between each adjacent level for 3- to 31-level MLI using PROPOSED method

m	THD (%)	THD _{diff} (%)	m	THD (%)	THD _{diff} (%)	m	THD (%)	THD _{diff} (%)
3	28.96359		13	6.12902	1.12824	23	3.45809	0.32913
5	16.42139	12.54220	15	5.30621	0.82281	25	3.18205	0.27604
7	11.53016	4.89123	17	4.67937	0.62684	27	2.94672	0.23533
9	8.90240	2.62776	19	4.18606	0.49331	29	2.74431	0.20241
11	7.25726	1.64514	21	3.78722	0.39884	31	2.56784	0.17647

Table 6. Goodness of fit for curve fitting of (5)

Statistical Analysis	SSE	R-square	Adjusted R-square	RMSE
Values	0.4655	0.9993	0.9992	0.2057



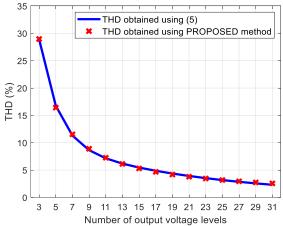


Figure 4. Total number of THD calculations and computational time for 3- to 31-level MLI using MESP and PROPOSED methods

Figure 5. Fitted curve plot for minimal THD

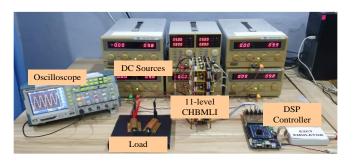


Figure 6. Experimental setup for 11-level CHBMLI

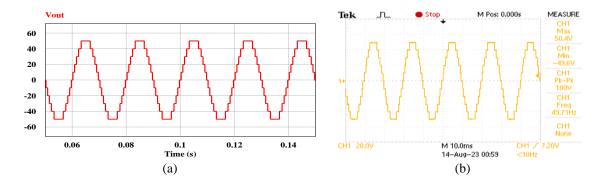


Figure 7. Output voltage waveforms for 11-level CHBMLI: (a) simulation and (b) experiment

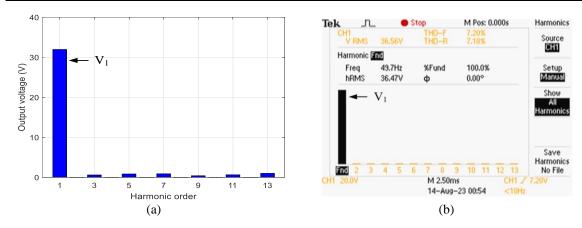


Figure 8. Harmonics spectrum of output voltage waveform for 11-level CHBMLI: (a) simulation and (b) experiment

Table	Table 7. Comparison of percentage error between theoretical, simulation and experimental results										
m		THD (%)	$V_1(V)$								
$\mathrm{THD}_{\mathrm{theo}}$	THD _{sim} THD _{exp}	% Er	ror	$V_{1_theo}V_{1_sim}V_{1_exp}$	% Error						
	·	$ \left \frac{\text{THD}_{\text{theo}} \text{ vs THD}_{\text{sim}}}{\text{THD}_{\text{theo}} - \text{THD}_{\text{sim}}} \right \\ \times 100 $	$\begin{aligned} & \frac{\text{THD}_{\text{sim}} \text{ vs THD}_{\text{exp}}}{\text{THD}_{\text{sim}} - \text{THD}_{\text{exp}}} \\ & \frac{\text{THD}_{\text{sim}} - \text{THD}_{\text{exp}}}{\text{THD}_{\text{sim}}} \\ & \times 100 \end{aligned}$		$ \begin{vmatrix} V_{1_\text{theo}} \text{ Vs } V_{1_\text{sim}} \\ \frac{V_{1_\text{theo}} - V_{1_\text{sim}}}{V_{1_\text{theo}}} \\ \times 100 \end{vmatrix} $	$\begin{vmatrix} V_{1_{\text{sim}}} \text{ vs } V_{1_{\text{exp}}} \\ \frac{V_{1_{\text{sim}}} - V_{1_{\text{exp}}}}{V_{1_{\text{sim}}}} \\ \times 100 \end{vmatrix}$					
7 11.530161	11.53023 11.60	0.0006	0.6051	31.9631.9631.75	0.00	0.6571					
9 8.90240	8.90245 8.90	0.0006	0.0275	41.9841.9841.66	0.00	0.7623					

0.7775

51.9651.9651.58

0.00

0.7313

5. CONCLUSION

11 7.25726 7.25642 7.20

This paper proposes an improved algorithm to determine the switching angles with low THD for MLI. The proposed algorithm has been implemented using a MATLAB script to determine a set of switching angles with low THD for 3- to 31-level CHBMLI. The comparative analysis concludes that the proposed algorithm significantly reduces the total number of THD calculations and the computational time compared to those of MESP method. A PSIM simulation model has been developed to validate the switching angles and the corresponding THDs obtained from the MATLAB script. An experimental setup has also been developed to validate the simulation results. The theoretical, simulation, and experimental results are in good agreement.

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REFERENCES

- [1] M. Jayabalan, B. Jeevarathinam, and T. Sandirasegarane, "Reduced switch count pulse width modulated multilevel inverter," *IET Power Electronics*, vol. 10, no. 1, pp. 10–17, Jan. 2017, doi: 10.1049/iet-pel.2015.0720.
- [2] O. Lopez-Santos, C. A. Jacanamejoy-Jamioy, D. F. Salazar-D'Antonio, J. R. Corredor-Ramírez, G. Garcia, and L. Martinez-Salamero, "A single-phase transformer-based cascaded asymmetric multilevel inverter with balanced power distribution," *IEEE Access*, vol. 7, pp. 98182–98196, 2019, doi: 10.1109/ACCESS.2019.2930230.
- [3] M. D. Siddique, S. Mekhilef, N. M. Shah, and M. A. Memon, "Optimal design of a new cascaded multilevel inverter topology with reduced switch count," *IEEE Access*, vol. 7, pp. 24498–24510, 2019, doi: 10.1109/ACCESS.2019.2890872.
- [4] Y. Li, X. P. Zhang, and N. Li, "An improved hybrid PSO-TS algorithm for solving nonlinear equations of SHEPWM in multilevel inverters," *IEEE Access*, vol. 10, pp. 48112–48125, 2022, doi: 10.1109/ACCESS.2022.3170442.
- [5] M. Sadoughi, A. Pourdadashnia, M. Farhadi-Kangarlu, and S. Galvani, "PSO-optimized SHE-PWM technique in a cascaded H-bridge multilevel inverter for variable output voltage applications," *IEEE Trans Power Electron*, vol. 37, no. 7, pp. 8065–8075, Jul. 2022. doi: 10.1109/TPEL.2022.3146825.
- [6] E. Babaei, S. Alilu, and S. Laali, "A new general topology for cascaded multilevel inverters with reduced number of components based on developed H-bridge," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 8, pp. 3932–3939, Aug. 2014, doi: 10.1109/TIE.2013.2286561.
- [7] R. A. Ahmed, E. D. Hassan, and A. H. Saleh, "A new flying capacitor multilevel converter topology with reduction of power electronic components," *International Journal of Power Electronics and Drive Systems*, vol. 14, no. 2, pp. 1011–1023, Jun. 2023, doi: 10.11591/ijpeds.v14.i2.pp1011-1023.

0.0116

- [8] H. Khoun-Jahan et al., "Switched capacitor based cascaded half-bridge multilevel inverter with voltage boosting feature," CPSS Transactions on Power Electronics and Applications, vol. 6, no. 1, pp. 63–73, Mar. 2021, doi: 10.24295/CPSSTPEA.2021.00006.
- [9] F. Sebaaly, M. Sharifzadeh, H. Y. Kanaan, and K. Al-Haddad, "Multilevel switching-mode operation of finite-set model predictive control for grid-connected packed E-cell inverter," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 8, pp. 6992–7001, Aug. 2021, doi: 10.1109/TIE.2020.3003627.
- [10] A. Sheir, M. Z. Youssef, and M. Orabi, "A novel bidirectional T-type multilevel inverter for electric vehicle applications," *IEEE Trans Power Electron*, vol. 34, no. 7, pp. 6648–6658, Jul. 2019, doi: 10.1109/TPEL.2018.2871624.
- [11] R. R. Kumar and J. Choudhary, "A novel multilevel inverter with reduced components and minimized voltage unbalance," *International Journal of Power Electronics and Drive Systems*, vol. 13, no. 4, pp. 2365–2377, Dec. 2022, doi: 10.11591/ijpeds.v13.i4.pp2365-2377.
 [12] A. Poorfakhraei, M. Narimani, and A. Emadi, "A review of multilevel inverter topologies in electric vehicles: Current status and
- [12] A. Poorfakhraei, M. Narimani, and A. Emadi, "A review of multilevel inverter topologies in electric vehicles: Current status and future trends," *IEEE Open Journal of Power Electronics*, vol. 2. Institute of Electrical and Electronics Engineers Inc., pp. 155–170, 2021. doi: 10.1109/OJPEL.2021.3063550.
- [13] K. Haghdar, "Optimal DC source influence on selective harmonic elimination in multilevel inverters using teaching-learning-based optimization," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 2, pp. 942–949, Feb. 2020, doi: 10.1109/TIE.2019.2901657.
- [14] K. Haghdar and H. A. Shayanfar, "Selective harmonic elimination with optimal DC sources in multilevel inverters using generalized pattern search," *IEEE Trans Industr Inform*, vol. 14, no. 7, pp. 3124–3131, Jul. 2018, doi: 10.1109/TII.2018.2790931.
- [15] G. Krithiga and V. Mohan, "Elimination of harmonics in multilevel inverter using multi-group marine predator algorithm-based enhanced RNN," *International Transactions on Electrical Energy Systems*, vol. 2022, 2022, doi: 10.1155/2022/8004425.
- [16] M. Khizer, U. T. Shami, M. F. Zia, Y. Amirat, and M. Benbouzid, "Selective harmonic elimination in a cascaded multilevel inverter of distributed power generators using water cycle algorithm," *Machines*, vol. 10, no. 5, p. 399, May 2022, doi: 10.3390/machines10050399.
- [17] M. Khizer, S. Liaquat, M. F. Zia, S. Kanukollu, A. Al-Durra, and S. M. Muyeen, "Selective harmonic elimination in a multilevel inverter using multi-criteria search enhanced firefly algorithm," *IEEE Access*, vol. 11, pp. 3706–3716, 2023, doi: 10.1109/ACCESS.2023.3234918.
- [18] R. Salehi, N. Farokhnia, M. Abedi, and S. H. Fathi, "Elimination of low order harmonics in multilevel inverters using genetic algorithm," *Journal of Power Electronics*, vol. 11, no. 2, pp. 132–139, 2011, doi: 10.6113/JPE.2011.11.2.132.
- [19] A. Routray, R. K. Singh, and R. Mahanty, "Harmonic minimization in three-phase hybrid cascaded multilevel inverter using modified particle swarm optimization," *IEEE Trans Industr Inform*, vol. 15, no. 8, pp. 4407–4417, Aug. 2019, doi: 10.1109/TII.2018.2883050.
- [20] V. Satyanarayana and V. Jayasankar, "Modeling and design of PV grid integration for GA-PSO based on fluctuating power quality," *International Journal of Power Electronics and Drive Systems*, vol. 14, no. 3, pp. 1450–1457, Sep. 2023, doi: 10.11591/jipeds.v14.i3.pp1450-1457.
- 10.11591/ijpeds.v14.i3.pp1450-1457.

 [21] C. A. L. Espinosa, "Minimization of THD and angles calculation for multilevel inverters," 2012. [Online]. Available: https://www.researchgate.net/publication/326677762
- [22] S. Sreelakshmi, M. S. Sujatha, J. R. Rahul, and T. Sutikno, "Reduced switched seven level multilevel inverter by modified carrier for high voltage industrial applications," *International Journal of Power Electronics and Drive Systems*, vol. 14, no. 2, pp. 872–881, Jun. 2023, doi: 10.11591/ijpeds.v14.i2.pp872-881.
- [23] F. L. Luo, "Investigation on best switching angles to obtain lowest THD for multilevel DC/AC inverters," in *Proceedings of the* 2013 IEEE 8th Conference on Industrial Electronics and Applications (ICIEA), Melbourne, Australia., 2013, pp. 1814–1818.
- [24] P. S. Gnanamurthy and V. Govindasamy, "Analysis of cascaded H-bridge multilevel inverter with current control methods," *International Journal of Power Electronics and Drive Systems*, vol. 13, no. 2, pp. 998–1006, Jun. 2022, doi: 10.11591/ijpeds.v13.i2.pp998-1006.
- [25] M. Trabelsi, H. Vahedi, and H. Abu-Rub, "Review on single-DC-source multilevel inverters: Topologies, challenges, industrial applications, and recommendations," *IEEE Open Journal of the Industrial Electronics Society*, vol. 2. Institute of Electrical and Electronics Engineers Inc., pp. 112–127, 2021. doi: 10.1109/OJIES.2021.3054666.

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