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Stackable independent power switch cell architecture for isolation voltage summation using WBG devices

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ABSTRACT

Power electronics is a critical driver of innovation in industries like renewable energy, electric vehicles, and consumer electronics. While silicon (Si) devices have been dominant for five decades, escalating demands for higher power density expose limitations in terms of blocking voltage capacity, operational temperature, and switching frequency. Wide band-gap (WBG) materials, such as silicon carbide (SiC) and gallium nitride (GaN), offer compelling alternatives with low input capacitance, reduced losses, and excellent thermal characteristics. In addition, expanding electrical capabilities involves constructing an array of devices, such as series-connected power MOSFETs. This configuration offers advantages like higher blocking voltage, lower conduction losses, and reduced costs. This paper introduces the design of a fast-switching, stackable switching unit cell (SSUC) utilizing SiC MOSFET devices as power components. The SSUC facilitates the creation of versatile compound switches. To protect the power switch from harmful voltages and current spikes, the design incorporates both an active voltage clamp and a snubber with energy recovery. This feature extends the number of stages that can be connected in series. Experiments with a three-stage compound device, successfully tested at 3 kV, validate the practical applicability and flexibility of this concept.

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1. INTRODUCTION

Power electronics play a primary role in driving innovation across various industries, including renewable energy, electric vehicles, and consumer electronics [1]. This evolution requires the improvement of efficiency and the increase in the power density of converters for more compact and lightweight solutions. To achieve these goals, there are several technical challenges to overcome, such as e.g. increasing the blocking voltage of power switches, raising the voltage output of converters, and increasing switching frequencies while minimizing losses.

For the past five decades, silicon (Si) devices have dominated power electronics [2]. However, as demands for higher power density without sacrificing efficiency grow, silicon-based power devices face lim-

itations in terms of blocking voltage capacity, operational temperature, and switching frequency [3], [4]. In recent years, a new generation of power devices based on wide band-gap (WBG) semiconductor materials has become available as commercial-off-the-shelf(COTS) products. WBG semiconductors, such as silicon carbide (SiC) and gallium nitride (GaN), exhibit improved characteristics, positioning them as long-term replacements for Si power devices [5].

Power devices based on WBG materials are appealing due to their low input capacitances, reduced conduction and switching losses, high operating temperatures, and excellent thermal conductivity [6]. SiC, in particular, is a preferred semiconductor for high-voltage and high-power applications when both electrical and thermal limitations are considered [7]. Moreover, extending the electrical characteristics of these devices is achievable by creating a series array of devices. This approach effectively enhances the capabilities of individual power switches by leveraging their combined voltage ratings. Series-connected power MOSFETs offer several advantages, including lower conduction losses and reduced cost. The total on-state resistance and cost of such a switch arrangement are lower compared to a single switch supporting the full blocking voltage [8].

In the traditional approach, each switch within a series array is accompanied by a dedicated drive circuit designed to withstand the maximum possible voltage [9]–[11]. This is challenging because the blocking voltage capability requirement of the gate driver increases geometrically with the number of devices connected in series, forcing the use of bulky and expensive alternative methods, like fiber optics, to transmit the command information [12]. Voltage imbalances in power devices primarily stem from parasitic capacitances, device parameter variations, gate driver delays, and time jitter [13]–[16]. The impact of these factors can be reduced through the power switch selection, aiming for low parameter variation, and synchronizing gate-drive signals.

In this setup, the control system plays a crucial role by ensuring precise gate signal alignment to prevent timing issues that could cause significant voltage differences between the drain and source of the transistor. Not implementing these safeguards could potentially threaten the operation of the composite switch, as discussed in [17]. One method to avoid the overvoltage condition on any power device in the array is the use of active voltage clamps [18]–[20]. Wang *et al.* in [21] proposes a feedback network composed of a string of zenner diodes that are directly connected to the gate of the power switch. In this proposal, an assessment and sizing of the driver is needed because, when the overvoltage condition is triggered, there is a direct current flow path from the drain of the power transistor to the gate driver. Additionally, to address voltage imbalances, passive snubber circuits and active gate control circuits are also employed [19].

Properly turning off the power device is essential to avoid unexpected turn-on in high $\frac{dv}{dt}$ scenarios, and it requires using a bipolar output stage that can provide a negative gate-source voltage during the turn-off phase. Two control approaches are commonly used for this type of composite device. The first approach involves centralizing control by commanding all gate drivers from a single control module, recognizing that it manages a set of power devices acting as a single switch. The second approach is to daisy-chain the command signal through each gate driver within the array.

In terms of power management, each driver must have its dedicated isolated power supply, which can be connected to a shared voltage domain or also daisy-chained. Alves *et al.* proposed a cascade gate driving scheme (AS4) in [13], which reduces the common-mode current injected from the isolation capacitance of the gate driver power supply. While this reduction is substantial, the series arrangement still exhibits notable voltage imbalances that must be addressed externally using a snubber, especially when operating the array close to its maximum blocking voltage. In their approach, the control strategy for each device involves transmitting the drive signal for all devices from a single control logic, with each driver hard-wired to read its respective control signal.

Implementing a cascaded configuration for the isolated power supplies of each gate driver within the array introduces practical limitations on the number of cells that can be stacked. Given that the efficiency of each DC-DC stage plays a significant role in this arrangement, it is important to choose the right number of gate drivers [22]. Utilizing GaN devices for the output stage of each gate driver opens up the possibility of expanding the arrays to multiple stages. In the evaluation conducted in [23], the author investigates the implementation of bipolar gate driver stages for SiC MOSFETs, which exhibit comparable electrical characteristics in terms of current and voltage swing. Notably, GaN devices outperform their silicon counterparts in terms of control power and PCB real estate.

Adding to the above-mentioned issue using energy recovery techniques eases the burden on each driver power supply, improving the overall efficiency of the switching cell and, consequently, the efficiency of

the compound switch. Zhang *et al.* in their work [24] propose a technique to recover energy from the passive snubber created with capacitive and diode networks. However, to achieve energy recovery, an active device is incorporated, adding extra complexity to the control system to enable recuperation.

Additionally, Guerrero *et al.* introduced a cascade scheme in their work [25], to recover a portion of the energy that is typically lost during the snubbering process. This harvested energy is then utilized to power up the gate drivers, further enhancing the overall efficiency of the system. The work claims a reduction in switching losses exceeding 40% compared to hard switching operations.

In this study, we introduce the development of a fast-switching, stackable switching unit cell utilizing SiC MOSFET devices. To enhance switching efficiency and reduce energy losses, an active voltage clamp snubber and a snubber with energy recovery are incorporated. Additionally, GaN high electron mobility transistors (HEMTs) are employed in the driver circuits, to lower the power requirements of the driver itself. To validate the effectiveness of this approach, experiments were conducted with a compound device comprising three stages, based on third-generation state-of-the-art SiC power devices. The results demonstrate the practical applicability and flexibility of this concept.

2. PROPOSED STACKABLE SWITCHING UNIT CELL

This section presents the working principles of the proposed stackable switching unit cell (SSUC), using low-voltage GaN HEMTs to control a Wolfspeed C2M0280120D 1200V SiC MOSFETs selected for cascade operation. Figure 1 shows a simplified schematic of the SSUC. This diagram shows the topology of the stackable cell, the purple box identifies the gate driver, the green box identifies the isolation stage, the red box, the overvoltage clamp, and the blue box contains the snubber with energy recovery.

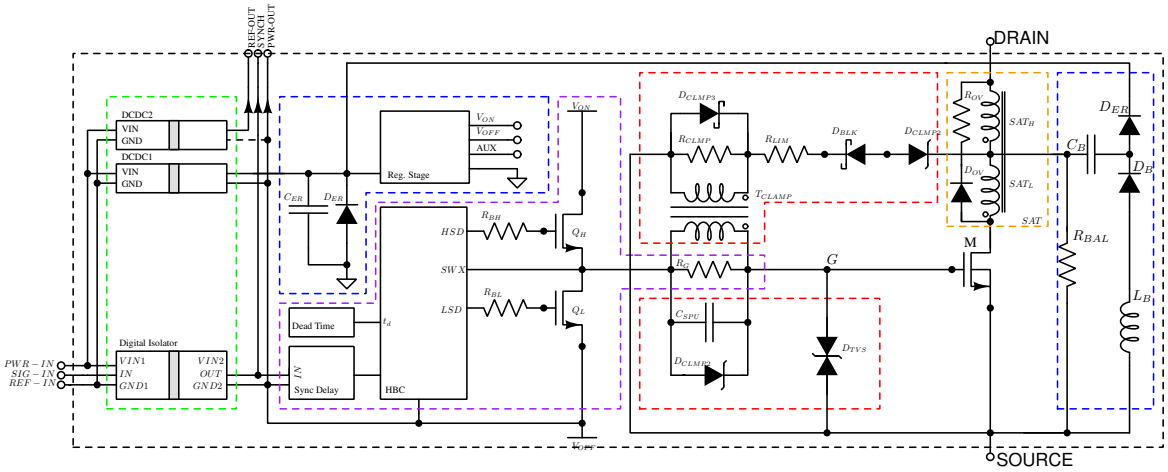

Figure 1. Stackeable switching unit cell (SSUC) block diagram

2.1. Gate driver

To turn on the SiC MOSFET power switch M in Figure 1, a high gate to source voltage needs to be applied. This voltage needs to be not only higher than the threshold voltage (V_{TH}), but it must be as high as possible to reduce the on-series resistance between the drain and the source. Applying this high overdrive gate voltage implies charging the non-linear gate capacitance of the device [2]. To turn off the MOSFET the gate to source voltage must be smaller than V_{TH}, discharging the gate capacitance. In both cases, a gate driver circuit is needed to ensure correct switching.

In Figure 1, the purple box represents a simplified schematic of the proposed gate driver. An inverter leg structure consists of GaN transistors, Q_H and Q_L, which are connected in series between two power rails, V_{ON} and V_{OFF}. The central node of this leg is connected to the gate of the PSW, labeled as 'G', through the resistor R_G. When either Q_H or Q_L is in the 'on' state, the resistor R_G limits the charging current flowing to the gate. This limit in the charging current reduce the rate of change of the gate-source voltage (V_{GS} slew rate), thereby affecting the turn-on/off time of the PSW.

The Gallium Nitride HEMTs GS61004B from GaN Systems have been chosen as the current booster switches (Q_H and Q_L) because they offer a high continuous drain current (I_D), a high blocking voltage rate (V_{DSS}), and a low On-Resistance ($R_{DS}ON$). Furthermore, they exhibit a significantly reduced input capacitance (C_{ISS}) compared to silicon-based alternatives. Their compact footprint also enables a more space-efficient circuit design. Table 1 provides a summary of the key parameters for the GaN transistors.

Resistors R_{BH} and R_{BL} control the current to the gates of transistors Q_H and Q_L, minimizing gate oscillations and reducing electromagnetic emissions. This ensures fast and secure device operation. The voltages of the power rails used for charging and discharging the gate of the PSW were selected to enhance its performance. To turn on the PSW, V_{ON} is set to 20 V, thereby reducing the on-resistance (R_{DS-ON}) and minimizing conduction losses. Conversely, V_{OFF} is chosen as -5 V to enhance the gate's noise immunity when turning off the power device.

Table 1. GS61004B GAN HEMT transistor key parameters list

Parameter		Value
Breakdown voltage	V_{DS-B}	100 V
Rated current (Tc=100C)	I_D	26 A
Gate-source voltage Max	V_{GS-MX}	-10 V / 7 V
Threshold voltage	V_{TH}	1.7 V
Input capacitance	C_{ISS}	260 pF
Output capacitance	C_{OSS}	110 pF
Gate charge	Q_G	3.3 nC
On-state resistance	R_{DS-ON}	37 $m\Omega$

After the signal propagates a digital isolator, it reaches an analog sync delay, which is used to synchronize the gate driver output with the other SSUCs in the array, reducing the voltage imbalance in the V_{DS} of the PSW. Subsequently, the signal is directed to a dedicated controller unit, responsible for reading both the input signal, denoted as IN, and the dead-time configuration, represented as t_D. This controller generates two complementary non-overlapping control signals. These signals, in turn, switch the GaN transistors on and off, using a gate-source voltage (V_{GS}) of 5 V/0 V.

As stated above t_D is an analog input that configures the dead-time injected between state transitions to prevent the undesired shot-through effect in the GaN half-bridge. During the dead time, both Q_H and Q_L are turned off, and the conduction state of the PSW is maintained until the dead time is extinguished. Throughout a complete switching cycle of the PSW, the driver circuit undergoes four distinct stages, as outlined in Figure 2.

- Stage-1 (S1): When the input signal IN is in a low state, the gate-source voltage (V_{GSL}) of transistor Q_L rises to 5 V, effectively turning the device ON. At this point, transistor Q_H remains in the OFF state (V_{GSH} at 0 V), and the voltage across the gate-source of the PSW (V_{GS-PSW}) remains at V_{OFF}. In this stage, the capacitance C_{ISS}, comprised of C_{GD} and C_{GS}, discharges through the resistor R_G, leaving the PSW in an OFF state with no current flow permitted.
- Stage-2 (S2): When the input signal IN transitions to a high state, the dead-time period begins. Transistor Q_L is turned off without affecting the conduction state of Q_H. The voltage across V_{GS-PSW} is maintained by its own input capacitance, C_{ISS}.
- Stage-3 (S3): After the dead-time period concludes, transistor Q_H is activated (V_{GSH} = 5 V), while Q_L remains in the OFF state. As a result, the voltage across V_{GS-PSW} rises to V_{ON}. During this stage, the capacitance C_{ISS} is charged through R_G, effectively turning on the PSW and allowing current to flow.
- Stage-4 (S4): When the input signal IN returns to a low state, the dead-time period starts once again. At this point, transistor Q_H is deactivated, while Q_L remains OFF. The conduction state of the PSW remains unaltered during the dead-time period until stage-1 begins anew, and the sequence repeats.

2.2. Overvoltage clamp

To prevent potentially hazardous voltage levels in the drain-to-source of the PSW, an overvoltage (OV) protection mechanism is employed. The highlighted red-boxed section in Figure 1 illustrates the implementation of this clamp. During the blocking phase, if the voltage V_{DS} across the PSW surpasses the breakdown voltage limit, D_{CLMP2} begins conducting and induces a voltage in the primary winding of T_{CLMP}. Consequently, in the secondary winding, a voltage pulse supplements the gate driver signal responsible for control-

ling the PSW. When this pulse reaches a sufficient magnitude, it overrides the current V_{GS} voltage at the PSW, thereby turning on the switch and reducing V_{DS}.

To prevent electrical overstress on the gate of the PSW, diodes D_{CLMP3} and D_{TVS} control the maximum voltage that the clamp can deliver to the PSW's gate. Conversely, when the voltage across the Drain-to-Source of the PSW falls below the breakdown voltage of diode D_{CLMP2}, the clamp remains transparent to the gate driver's operation. D_{BLK} prevents the establishment of a direct conduction path from the gate driver to the drain while the PSW is in the ON state. During the turn-on phase of the PSW, the parasitic capacitance of diodes D_{CLMP2} and D_{BLK} discharges through the drain of the PSW, creating a negative voltage at the primary of T_{CLMP}. The Schottky diode, D_{CLMP1}, averts this condition by providing an alternate path for the discharge process.

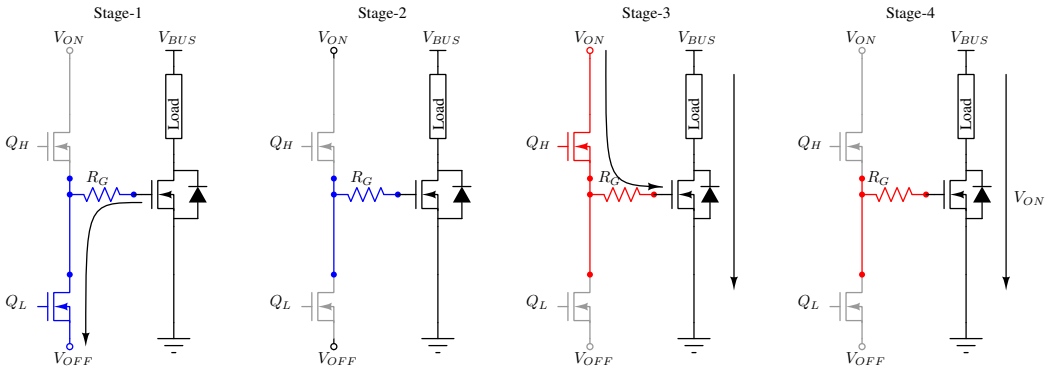

Figure 2. Operation states of the driver and the SiC power MOSFET

2.3. Snubber with energy recover

As stated in previous study [26], a snubber is a circuit that is placed across the PSW to protect it from potential harmful voltage and current spikes, while also shaping the load to keep it within the safe operating area (SOA). During this process, it is possible to recover part of the energy that would otherwise be wasted and use it to ease the load on the power supplies of the gate driver of each SSUC. The blue-box section in Figure 3 shows the implementation of the snubber with energy recovery (ER) capability. Figure 3 presents a simplified diagram depicting the four operational stages of the proposed snubber.

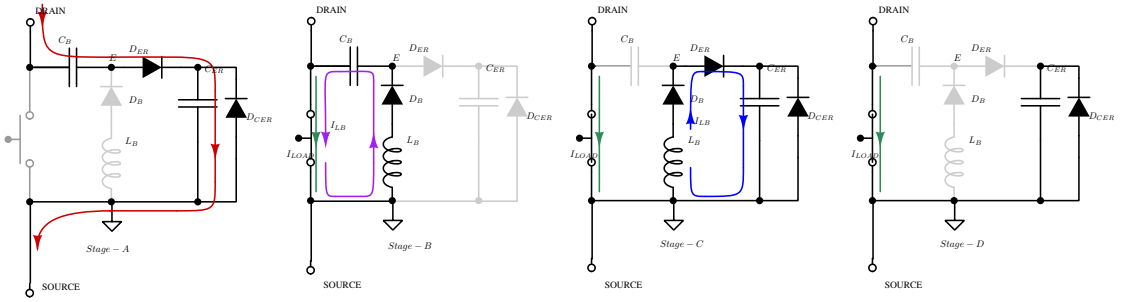

Figure 3. Energy recovery snubber: operation stages

– Stage-A: With the PSW blocking the current conduction, the pathway formed by C_B, D_{ER}, and C_{ER} charges up to the SSCU blocking voltage. The voltage across C_{ER} depends on the load consumption, reaching a theoretical maximum determined by the ratio $V_{DSX} \cdot \frac{C_{ER}}{C_{ER}+C_B}$, where V_{DSX} is the drain-to-source voltage of the SSCU. To prevent the accumulation of unsafe values V_{CER} in the capacitor C_{ER}, the Zener diode D_{CER} safeguards the load by providing a controlled discharge path.
– Stage-B: When the PSW enters in conduction, node E experiences a negative voltage compared to the PSW source, allowing current to build up in inductor L_B. During this stage, diode D_{ER} stays blocked. During this stage, the PSW current load includes both the load current (I_{LOAD}) and the snubber current (I_{LB}).

– Stage-C: Once the voltage across capacitor C_B matches V_{CER}, the current from inductor L_B quickly flows through diode D_{ER}, transferring energy from the inductor to capacitor C_{ER}.
– Stage-D: Once the current across inductor L_B is extinguished, the diode D_{ER} ceases to conduct, and capacitor C_{ER} becomes disconnected from the PSW.

2.4. Smoothing saturable autotransformer

During regular operation, the PSW experiences hard switching, attributed to the parasitic capacitances in the application load, the OV Clamp and the ER Snubber (detailed in sections 2.2 and 2.3 to address this issue, a saturable auto-transformer (SAT) was introduced. The orange-box section in Figure 1 illustrates the SAT, comprising two windings (SAT-H and SAT-L) sharing the same magnetic core. The SAT directly connects to the PSW drain, while both the ER Snubber and the OV Clamp are linked to the middle tap point.

As the PSW begins conduction, the external parasitic capacitances encounter the inductances of the SAT, smoothing the switching process. Once the current surpasses the saturation level of the SAT, the actual inductance becomes negligible, enabling normal SSUC operation. During PSW cutoff process, the drain-source current (I_{DS}) abruptly drops to zero, and the energy stored in the SAT is channeled to the capacitor C_B eliminating the need for an additional bulky RC snubber. An additional local snubber, consisting of D_{OV} and R_{OV}, safeguards against any overvoltage caused by the parasitic inductance L_S in the system.

3. EXPERIMENTAL RESULTS AND DISCUSSION

To evaluate the performance of the proposed stackable switching cell, an array of three SSUCs was utilized to create a composite switch capable of successfully withstanding a blocking voltage of 3 kV with a maximum drain current of 6 amperes. To benchmark the stack of cells, a fully configurable dual pulse tester (DPT) with a adjustable load was employed. The configuration is illustrated in Figure 4. A variable AC source, generated by a variac, ranges from $0V_{RMS}$ to 250 V_{RMS}. The variac output connects to an isolation transformer for safety reasons. Subsequently, the isolated source links to a 9-stage Greinacher multiplier, scaling the voltage to approximately V_{BUS} = 3300 V_{AC}. To deliver a high current peak at this voltage, a high-voltage capacitor bank of 52 μF serves as a DC bus.

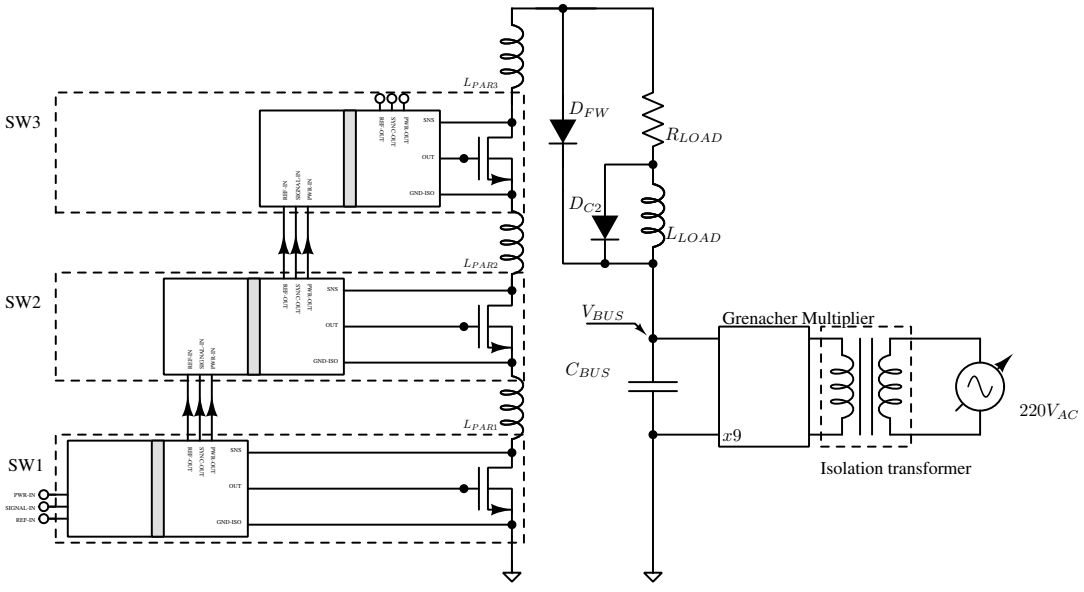

Figure 4. Three stage SSUC composite switch and the test bench simplified schematic

The load consists of a 230 μH air gap inductor (L_{LOAD}) in series with a 440 Ω resistor (R_{LOAD}). To handle the high voltage in the test, the load comprises a series array of 20 cells, each with a resistance of

22 Ω. Due to the elevated voltages in the test, the flywheel diode D_{FW} is implemented with a string of four Wolfspeed C3D10170H SIC Schottky diodes. To protect the DUT in the event of a sudden open load caused by a failure in R_{LOAD}, a high-voltage diode D_{C1} is connected in antiparallel with the inductor to provide a current path in case of failure, thereby safeguarding the DUT.

The PSW employed in the SSUC is the SiC MOSFET C2M0280120D from Wolfspeed. Its essential parameters are detailed in Table 2. Additionally, Table 3 compiles the information on the magnetic components utilized in each SSUC. The test was carried out applying a 1 KHz pulse train to the input control signal of the first stage of the compound switch. The turn on time was T_{ON}=1 μS, and the operation frequency was defined as f_{sw} = 1 KHz with a duty cycle $D \sim 0.1\%$.

All voltage measurements were performed using a Tektronix THS3014 with four isolated floating channels oscilloscope. As a current transducer a pearson electronics current monitor model 2878 was used. During the realization of the measurements all the best practices described in [27] were enforced. A picture of the test bench is shown in Figure 5.

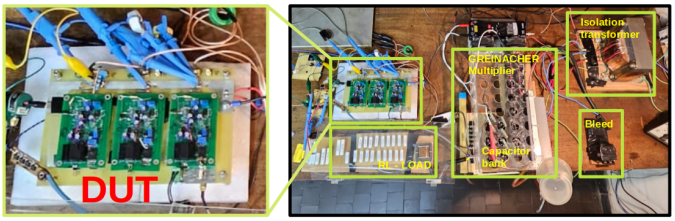

Figure 5. Experimental setup showing the DUT and the auxiliary circuitry needed to obtain 3 kV of test voltage

Table 2. CREE C2M0280120D transistors key parameters list

Parameter ($T = 25°C$)		Value
Breakdown voltage	V_{DS-B}	1200 V
Rated current (Tc=100C)	I_D	11 A
Gate-source voltage Max	V_{GS-MX}	-5 V/+25 V
Threshold voltage	V_{TH}	3.1 V
Input capacitance	C_{ISS}	$267pF@V_{DS} = 800V$ $400pF@V_{DS} = 0V$
Output capacitance	C_{OSS}	21 pF@1000 V
Gate charge	Q_G	19 nC
On-state resistance	R_{DS-ON}	240 $m\Omega$

Table 3. Magnetic component chacateristics

ID	Core	Material	Turns	AirGap(mm)	Wire Gage (mm2)
LS	EF25	N27	30	0.4	0.6
TP	RK 16/9,6/6,3	CF191	N1=4, N2=4	NA	0.6
SAT	2 x RK 16/9,6/6,3	CF191	SAT-H=5 / SAT-L=3	NA	0.6

3.1. Control signals and syncronization

Figure 6 depicts the input signal driving the DUT and the corresponding synchronization signals used to propagate the gate driver commands at each SSUC. This visualization clearly reveals the progressive lag accumulating due to the propagation delay inherent in each digital isolator stage. Figure 7 showcases the V_{GS} of the power switch for each SSUC within the DUT after compensating for the individual synchronization delays.

3.2. Switching characterization

Figure 8, presents the three drain-source voltages of each PSW ($V_{DS}SWi$), and the drain-source current ($DUT - I_{DS}$) and voltage ($DUT - V_{DS}$) characteristics of the DUT with a pure resistive load of $\sim$ 530 Ω. Throughout this test, the V_{BUS} voltage is maintained at 3kV. The figure illustrates the DUT's switching behavior during turn-on, with absence of a turn-on current spike due to the lo parasitic capacitance of the load

reaching a maximum value of 5.8 A. Furthermore, an observed gradual recovery in $DUT - V_{DS}$ at cutoff is attributed to the influence of the RC time constant between the load and the output capacitance of the DUT. A summary of the transient measurements with the resistive load is detailed in Table 4.

A second characterization is presented in Figure 9. In this setup, the load comprises a 230 μH airgap inductor in series with a 450 Ω resistor and a freewheeling diode. To enhance safety for the DUT and the instruments on the bench, an anti-arc protection mechanism is integrated. This prevents excessive voltage in V_{BUS} in case of a sudden load disconnection. The V_{BUS} voltage is maintained at 2.1 kV throughout this test.

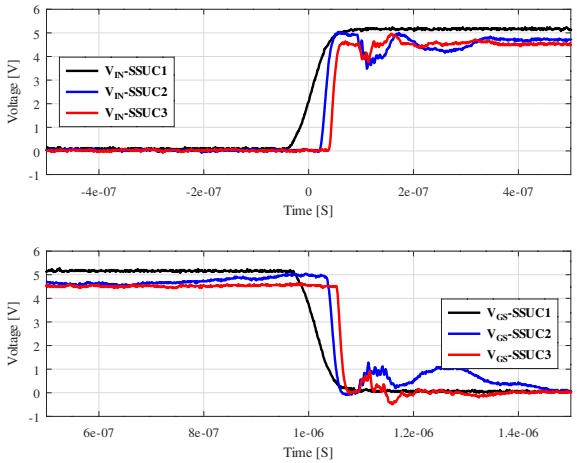

Figure 6. Input control signal lag of each SSUC due to the propagation time of each digital isolator

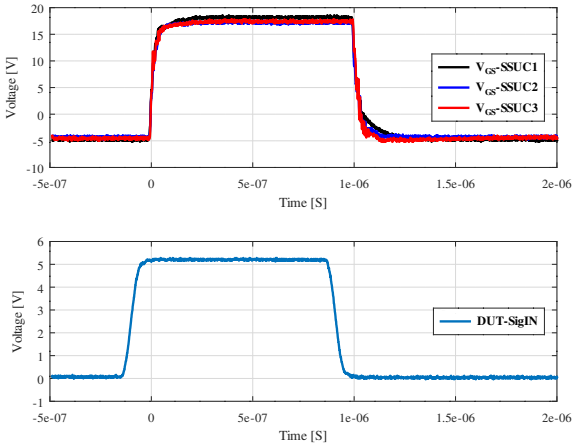

Figure 7. V_{GS} signal alignment after compensation at the gate of the GaN MOSFET in the three SSUC

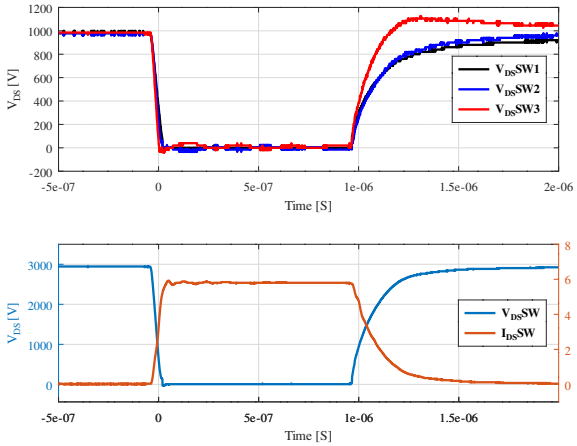

Figure 8. Voltages and current in the PSWs and DUT driving a resistive load operating at 3 kV

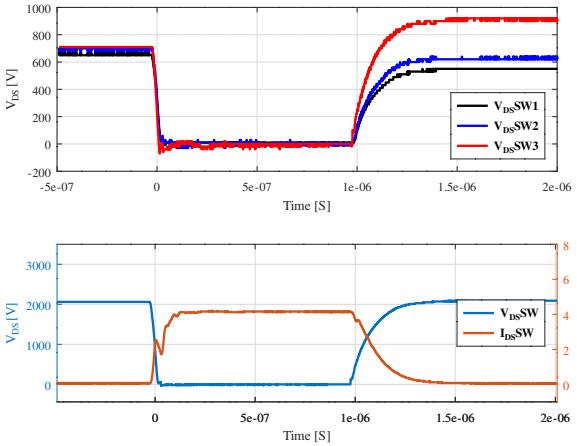

Figure 9. Voltages and current in the PSWs and DUT driving a resistive-inductive load operating at 2.1 kV

Upon initiating the test pulse, the $DUT - V_{DS}$ voltage of the DUT drops and there is an initial $DUT - I_{DS}$ current spike attributed to the parasitic capacitance of the load and the freewheeling diode. Subsequently, the $DUT - I_{DS}$ current begins to increase until reaches it maximum bounded by the load resistance, to approximately $\sim$ 4.5 A. At cutoff the $DUT - I_{DS}$ decreases slowly due to the RC time constant between the load and the output capacitance of the DUT. During this stage the inductor current extinguishes completely, resulting in a turn-on procedure at zero current despite the presence of the parasitic current peak. A summary of the transient measurements with the resistive-inductive load is detailed in Table 5. In both scenarios, an imbalance in the drain-to-source voltage of each SSUC is observed due to the different time constants of each node [16].

Table 4. Resistive load: measurement summary

Measuremet	Value
V_{BUS} Test voltage (V)	3000
$DUT - I_{DS}$ Test current (A)	5.8
$DUT - T_{ON}$ Turn On Time (nS)	50
$DUT - T_{OFF}$ Turn Off Time (nS)	350
$DUT - V_{DS}$ Max Slew-rate $(^{V}/_{nS})$	-80

Table 5. Inductive load: measurement summary

Measuremet	Value
V_{BUS} Test voltage (V)	2050
$DUT - I_{DS}$ Test current (A)	4.5
$DUT - T_{ON}$ Turn On Time (nS)	149
$DUT - T_{OFF}$ Turn Off Time (nS)	350
$DUT - V_{DS}$ Max Slew-rate $(^{V}/_{nS})$	-80

3.3. Overvoltage clamp

A prototype of the clamp circuitry was constructed and subjected to testing as part of the SSUC3, chosen for its role as the fastest PSW within the array. To ensure a secure environment for this block, the clamping voltage is reduced to 800 V (4x P6KE200A). The removal of the passive snubber in SSUC3 causes its PSW to withstand nearly the entire blocking voltage. This approach not only established a secure testing environment for the clamp but also ensured the protection of the DUT during the clamping voltage test. Thruought this test V_{BUS} was setted to 1150 V, with a 230 μH inductive load.

In Figure 10, the drain-source voltage of each SSUC in the array ($V_{DS}-SW_x$) is displayed, along with the $DUT - V_{DS}$ voltage. This plot also verifies that SSUC3 predominantly handles the bulk of the blocking voltage during the cut-off period. Furthermore, Figure 11 of SSUC3's drain-source voltage ($V_{DS}SW3$) and gate-source voltage ($V_{GS}SW3$) during the clamping event. When $V_{DS}SW3$ exceeds 800 V, a spike occurs in the clamp current (I_{DZ}), creating a voltage pulse in the transformer (T_{Clamp}) primary winding (V_{PT}) . This pulse, is transferred to the secondary and adds up to the current driver voltage (VOFF in this case), causing a controlled turn-on of the SSUC3 PSW. This process discharges the drain charge excess while allowing the remaining SSUCs to complete their cutoff process.

Additionally, the introduction of the T_{Clamp} brings a spurious signal to the $v_{GS}SW3$ signal. During turn-on, the discharging process of the parasitic capacitance of the zener array (D_{Clmp2}), connected to the transformer T_{Clamp} terminals, raises the voltage $V_{GS}SW3$ above the current V_{ON} level. Conversely, during cutoff, the charge in the parasitic capacitance of D_{Clmp2} and the extinguishing process of the magnetizing current of the T_{Clamp}, creates a prolonged tail in the V_{PT} and V_{GS}, as illustrated in Figure 11.

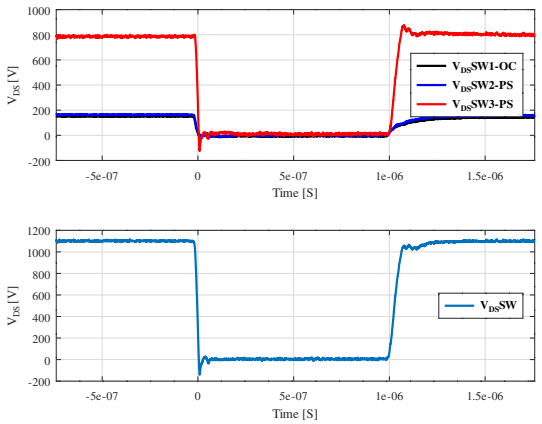

Figure 10. DUT V_{DS} plot of each SSUC stage and $DUT - V_{DS}$ showing the behavior during a high voltage clamp at cut-off

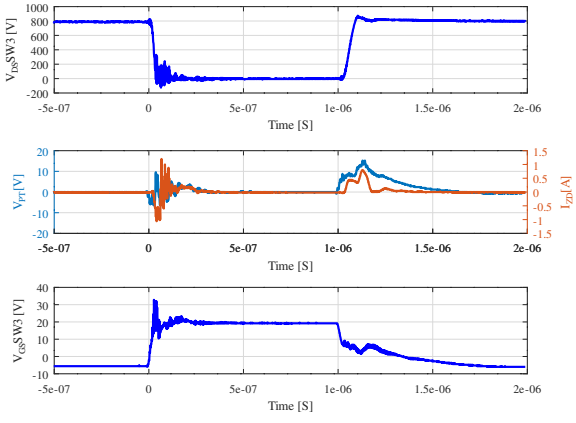

Figure 11. SW3 V_{DS} and V_{GS} plot and clamp current and voltages in the high voltage side during a high voltage clamp at cut-off

3.4. Energy recovery

A prototype of the ER Snubber was constructed and connected to SSUC3, chosen for its role as the fastest PSW within the array. To assess the maximum recovered power ($Power_{ER}$), the recovery capacitor C_{ER} was directly linked to a 220 Ω resistive load. Figure 12 depicts the voltage across C_{ER} during a 1 μS test pulse at a frequency of 1 kHz. The V_{BUS} was systematically increased from 100 V to 1500 V to evaluate the recovered power. Conversely, Figure 13 illustrates the voltage developed in C_{ER} at a constant V_{BUS} of 1000

V, while varying the frequency from 1 kHz to 8 kHz.

In both cases, the results show that, for medium blocking voltages and frequencies, the recovered power is in the range of the power actually consumed by the gate driver of the SSUC module. If the power exceeds the consumption of the driver circuit, using a high-voltage ancillary recovery converter to return the total recovered energy to the primary source, as done previously in [28], or sending back the excess energy to lower voltage levels using bidirectional auxiliary converters, as proposed in [25], would be beneficial.

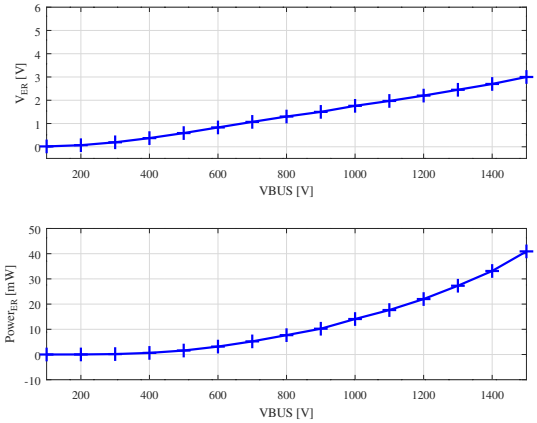

Figure 12. Voltage at C_{ER} and $Power_{ER}$ recovered during the ER Snubber operation versus V_{BUS} voltage

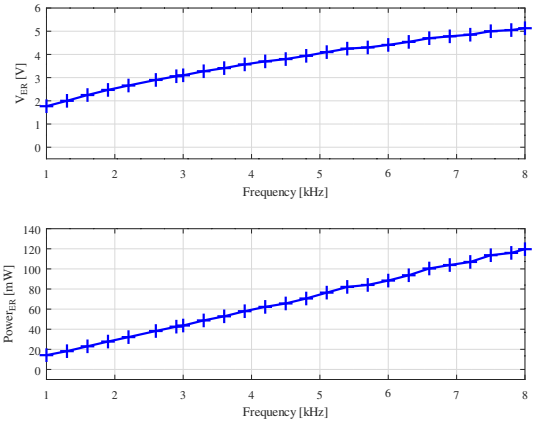

Figure 13. Voltage at C_{ER} and $Power_{ER}$ recovered during the ER Snubber operation versus switching frequency

3.5. PSW switching energy and smoothness

To assess the impact of the ER snubber in conjunction with the SAT on the switching behavior of the PSW, a computation of the switching losses was conducted. Table 6 illustrates the switching energy at turn-on and turn-off under the same load condition outlined in section 3. The results highlight that the Active ER Snubber, with the addition of the SAT, significantly reduces the total switching energy ($E_{ON}^{SW} + E_{OFF}^{SW}$) in the PSW by a factor of approximately 5.6 in comparison with the passive RC snubber.

Table 6. Switching losses comparison with and without ATS

Condition	V_{DS} (V)	I_{DS} (A)	E_{ON}^{SW} (μJ)	E_{OFF}^{SW} (μJ)
Passive RC Snubber	700	3.5	54	1370
Active ER Snubber	700	3.5	12	239

4. CONCLUSION

The proposed SSUC offers a flexible approach to associating SiC power MOS transistors in series, providing built-in static and dynamic compensations without introducing significant power losses in the compensating circuits. This design allows for a smooth switching process, integrating soft dissipative mechanisms that redirect some of the power consumed by the ER Snubber to the auxiliary power supplies of the SSUC. By adopting SiC MOS transistors as the PSW, the system achieves shorter switching times compared to silicon devices, even in scenarios where soft switching is desired. The command for each SSUC follows an isolated signal path, cascading from the lower SSUC to the higher ones. This configuration is mirrored in the ancillary DC-DC converters designed to power the stacked gate drivers.

The presented ER snubber stands out for its simplicity and lack of controlled ancillary devices. Each snubber's primary capacitor (C_B) can be constructed using metallized polypropylene, eliminating the necessity for bulky metal foil capacitors. The design's capability to harness and redirect recovered energy from the soft-switching snubbers back to the auxiliary supplies contributes to a reduction in the required magnitude of auxiliary power transfers from lower to higher voltage levels. Consequently, this enhances the scalability of the system by allowing an increased number of stacked levels. The amount of recovered power is closely tied to the system's operating frequency and voltage. If the ER snubber recuperates more energy than the SSUC actually

consumes locally in the control and gate driving, any excess energy needs local dissipation. Additionally, the inclusion of this snubber significantly reduces switching losses in the PSW, achieving a 5.6-fold reduction compared to a typical RC snubber, as observed in the results.

Additionally, a protection system against dynamic voltage imbalances during switching-off to blocking is proposed, protecting each transistor associated in series against overvoltage caused by speed mismatch between the associated transistors. This protection system, based on small magnetic components, acts on the command circuit without increasing the dissipation requirements of the driver output. While adopting currently available SiC MOS transistors requires associating more PSWs in series than if IGBTs were adopted, it leads to reduced switching times and eliminates the tail current effect. This allows for increased switching frequencies, ultimately reducing the size of passive components, particularly magnetic ones. As future work, to return the excess energy recovered by the soft switching snubbers, we are exploring two approaches: First, using a high-voltage ancillary recovery converter to return the total recovered energy to the primary source, or sending back the excess energy to lower voltage levels using bidirectional auxiliary converters.

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