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Harmonics elimination and reactive power compensation based on novel SDFT-PLL shunt active power filter control approach

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ABSTRACT

Active power filters are used to reduce current harmonics and compensate for reactive power in non-linear loads. This paper compares two approaches for estimating compensated current for a shunt active filter. The synchronous-reference- frame theory d-q and sliding fast Fourier-Transform algorithms are compared in this study. The comparison is based on the outcomes of simulations. For different load conditions, the results achieved by the approaches mentioned differ greatly. The sliding discrete Fourier transform SDFT approach has revealed the optimum choice. Indeed, sliding discrete Fourier transform-phase-locked-loop or SDFT-PLL is a perfect method also for synchronizing the inverter with a weak noisy grid.

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1. INTRODUCTION

Recently, with the diminution of fossil energy and rising environmental problems, clean energy such as photovoltaics (PVs) and wind turbines (WTs) are more popular as the percentage of renewable energy added to the grid expands, the control of them must be more efficient and effective [1]. Most grid-tie systems for example, shunt active power filters (SAPFs), uninterrupted power supplies (UPSs), and flexible AC transmission systems (FACTS) require grid voltage frequency and phase angle to be conveniently connected to the grid (synchronization) [1]. Synchronization is very important for signal processing, control purposes, and monitoring in power and energy systems [2].

Grid synchronization is classified into three methods. The first method is zero-crossing detection (ZCD) which is the easiest way for determining the phase of the grid voltage. However, its performance is not good when the grid voltage is distorted and its tracking speed is slow. The second method depends on voltage grid filtering such as Fourier transform, Kalman filtering, and arctangent function. Each type is based on different technique of filtering [1]. If the grid voltage has inter-harmonics or sub-harmonics, distortion will happen and spectrum leakage will occur. The first and second methods involve complex mathematical calculations which may slow down the system's performance. The third method is phase locked loop or PLL which is simple in implementation and performs well under complex conditions. PLL is classified as single-phase PLL or three-phase PLL. Clark and Park transformations are the most widely used approach in three-phase PLL. In single-phase cases, the grid data is limited which makes the performance of single-phase PLL is challenging. In other way, we can classify synchronization methods into open-loop methods which have no feedback signals and close-loop methods which have feedback signals.

A closed loop is widely used in power applications. Closed loop is classified into two categories, PLL and frequency-locked loop (FLL). Both are non-linear control systems. PLL is used in synchronous reference frames, whereas FLL is used in stationary reference frames [2]. Also, we can say that PLL is used in power applications but FLL is employed in other applications such as power system island detection [3] and flux estimate for electrical motor control [4]-[6].

Figure 1 depicts the basic components of all PLLs: the phase detector (PD), loop filter (LF), and voltage-controlled oscillator (VCO). There are numerous forms of PLLs. A type-1-PLL is the most basic type (a control system of type-N has N poles at the origin in its open-loop transfer function). They are characterized by having one integrator in the control loop, so the stability margins are high. Their main disadvantage is that in the presence of frequency drifts, they cannot attain a zero average steady state phase error. This disadvantage can be solved by employing a quasi-type PLL with fast dynamic response and strong filtering capacity [7]. Golestan *et al.* [7] depict a feature comparison of synchronization algorithms.

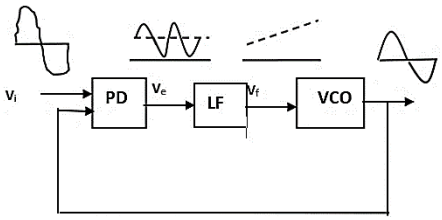

Figure 1. The basic scheme of a typical PLL

One of the first ways to estimate phase angles was the discrete Fourier transform method (DFT). This method provides a high level of harmonic resistance [8]. Sliding discrete Fourier transform (SDFT) is an enhanced version of the DFT that delivers optimal computational power and reduced latency by recursively applying the DFT algorithm. There is a phase shift between the actual grid angle and the estimated angle if the SDFT time window is not the same as the grid period. Some solutions for compensating for this phase error have been reported in [8], for example, time-varying Polynomial regression and Fourier coefficients. These strategies, in reality, are rendered with notable complexity. The undesired qualities of the SDFT in the case of off-nominal frequency include the phase error (which is a function of the frequency deviation) and a high-frequency oscillation apparent in the magnitude and phase angle estimations. In the literature, this high-frequency oscillation is denoted to a double-frequency ripple, and post-processing for frequency and phase angle estimates in the off-nominal mode is proposed. Post-processing can be done with either a basic digital averaging filter or a more complicated resampling filter [9].

Harmonics are produced by the widespread use of nonlinear loads like as personal computers, variable speed drives, UPS systems, and other electronic equipment. Current harmonics are widely used in industrial systems. Voltage harmonics interact with system impedances, resulting in current harmonics that have a significant impact on sensitive loads. Extraction of harmonic current reference (EHRC) is a key aspect of controlling shunt active power filters (SAPFs) used in power systems because any error in reference currents results in erroneous compensation.

Extensive research on EHRC algorithms has recently been conducted, and they have been classified into three major groups: time-domain, frequency-domain, and modern approaches. However, time-domain harmonic extraction techniques are always prevalent because they offer easy implementation features with higher speed and lower computing overhead. A summary of harmonic current extraction techniques is illustrated in Table 1 [10], [11].

Table 1. Harmonic current extraction techniques classification

Traditional methods		Modern methods
Time domain	Frequency domain	Neural network (NN)
Instantaneous active, reactive power (PQ) theory	Fourier series	Adaptive neural network (ANN)
Cross-vector theory	Discrete Fourier transform (DFT)	Adaptive linear neural network (ADLINE)
Direct method (PQR) theory	Fast Fourier transform (FFT)	Neuro-fuzzy
Synchronous reference frame (SRF) or d-q	Recursive discrete Fourier transform (RDFT)	
Filtering load current		
Capacitor voltage control	Kalman filter	
Correlation technique	Wavelet transform	

We will focus on the most crucial aspects. Synchronous reference frame (SRF), also known as d-q in other documents and power PQ theory algorithms are the most commonly applied time-domain approaches [10]. The current generated as a result of a nonlinear load will have both fundamental and harmonic components. When a three-phase abc natural frame is transformed to a two-phase synchronously rotating frame, the harmonic components appear as an AC signal while the fundamental component appears as a DC signal. When using SRF and PQ theory in harmonic extraction applications, the precision of the detected fundamental component is critical. The requisite fundamental components are frequently attained in both algorithms by employing an indirect detection strategy, i.e., a numerical Butterworth-type low-pass filter (LPF). The LPF method's behavior is essentially determined by the used harmonic order. As a result, the numerical LPF must be modified in order to deliver the best fundamental component detection and harmonic extraction performance. Improper tuning might cause considerable time delays and distortions during the harmonic extraction process. SRF technique is shown in Figure 2.

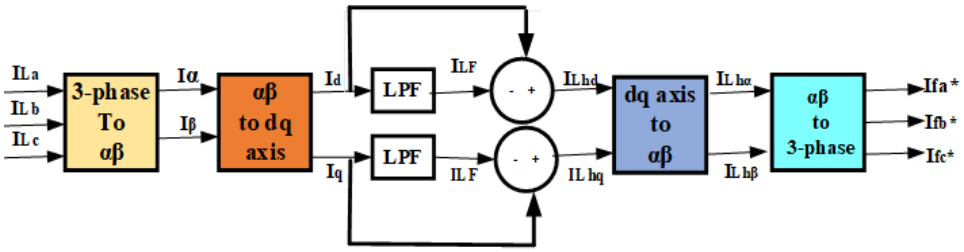

Figure 2. d-q harmonic detection technique

In a three-phase system, the two approaches can control SAPF to reduce current harmonics. However, SAPF using the SRF algorithm consistently succeeds in both dynamic-state and steady-state conditions. This is mainly because of to its simple and rapid processing characteristics, which reduce computational delays [10]. Another method is presented in [12] which is called synchronous detection method (SD). When the voltage source is considerably imbalanced, considerable errors can arise from the calculation formula when using the PQ theory directly. Then, it is difficult to execute reactive and harmonic current correction efficiently with unbalanced three-phase voltage sources. The SD approach is presented to regulate unbalanced three-phase voltage sources. The equal current synchronous detection method is a very valuable notion that should be implemented. Harmonic extraction with the Fourier transform (FT) is a convenient way for adjusting for certain harmonic components. The Fourier transform requires one more cycle of voltage waveform data and associated time to allow for delayed harmonic cancelation [13]. Because of problems in the PLL and passive filters employed in this technique, the SRF technique, which is often used for voltage sag extraction, does not respond rapidly or accurately to voltage harmonics [14]. Researchers from a variety of scientific areas, however, are inventing and designing artificial neural networks (ANN) to response challenges in pattern prediction, optimization, control and recognition. ADLINE is a form of ANN that has the advantages of being easily designed and deployed through hardware and has been successfully applied to harmonic extraction.

This approach may estimate the harmonic terms individually, such as the most damaging 5th and 7th harmonics [15]. To address this issue, the suggested sliding discrete Fourier transform-phase-locked-loop or SDFT-PLL is used to extract the fundamental load current component. Even when connected with a variable grid frequency, SDFT-PLL has an effective ability to isolate the DC-offset. This method can be utilized in synchronization applications like [16], as well as a harmonic extraction technique similar the one proposed in this paper. This paper's contributions can be summarized as follows: i) As an innovative use of such a reliable technique, obtaining the SAPF's reference harmonic current using the SDFT-PLL technique by extracting the fundamental load current. Keeping the capacitor DC voltage constant at its reference value throughout non-linear load instances; ii) Regardless of how nonlinear the load is, delivering a balanced current from the grid with unity power factor and total harmonic distortion or THD within the IEEE-519 standard limitations; and iii) Showing the proposed approach efficiency by comparing it to previously presented adaptive filtering techniques such as the d-q method.

This paper is organized as, section 2 describes the configuration of the SAPF discussing in details all its related control algorithms, focusing on the novel SDFT-PLL control for the synchronization and harmonics current extraction. Section 3 compares the suggested control method to the previous d-q control methodology and provides an evaluation of the proposed system's performance based on simulation results. Section 4 finally presents the conclusions.

2. SHUNT ACTIVE POWER FILTER SAPF CONFIGURATION

Figure 3 depicts the SAPF's block diagram. To efficiently govern the functioning of SAPF, its control system must be built using four different types of control algorithms, each of which serves a specific purpose, as stated in the following:

a) Extraction of harmonics algorithm

The primary purpose of this algorithm is to extract harmonic values from a harmonically polluted grid and use that values to generate a reference current signal $iref$. The non-linear load current signal iL is handled in this way so that its harmonic iH and fundamental $i1L$ elements can be isolated. Following the separation of the elements, $iref$ can be derived using whether the harmonic or fundamental elements, each of which has its own set of derivations. This approach is also known as the reference current generation algorithm in some publications since it generates reference current as its final output.

b) Synchronization algorithm

The primary role of this approach is to follow the angular position of the source voltage signal VS and then construct a phase- synchronization angle to link the generated $iref$. phase to the running power system phase. There are numerous harmonic extraction methods do not include a phase tracking component and instead rely solely on an implicit synchronization mechanism to provide an effective synchronization angle. However, some harmonic extraction techniques inherit phase tracking ability, such as the instantaneous power p-q theory. An explicit synchronization algorithm might be omitted in this scenario.

c) Capacitor voltage regulation algorithm

The fundamental role of the capacitor voltage DC regulation algorithm is to estimate the amount of dc-link charging current idc needed by the SAPF to keep the DC-link voltage Vdc constant at the desired value. Using a voltage control loop and either proportional-integral (PI) or fuzzy logic control (FLC) approaches, this algorithm always compares the measured Vdc to a set point value and minimizes the resulting error.

d) Current control algorithm

The primary function of this algorithm is to convert $iref$ from the harmonic extraction algorithm and idc from the capacitor DC voltage regulation algorithm into gating switching pulses S using a pulse-width modulation method while ensuring that the feedback signal $iinj$ or iS can path $iref$ using the control of current loop. This method is also known as the switching algorithm due to its usage in creating the pulses of switching gate. Sinusoidal - pulse-width modulation (SPWM), hysteresis control and space vector PWM (SVPWM) are a few instances of common approaches for this method. The presented four control algorithms are linked and work in a closed-loop way, with the monitored output (which might be $iinj$ or iS) observed and returned to be compared with the intended $iref$ until the measured output produces the desired outcome. Even when confronted with interruptions such as dynamic conditions, the algorithms have been demonstrated in practice to be capable of responding fast in order to return the monitored output to its desired shape [17]. The four algorithms employed in this study will be thoroughly detailed in the following sections.

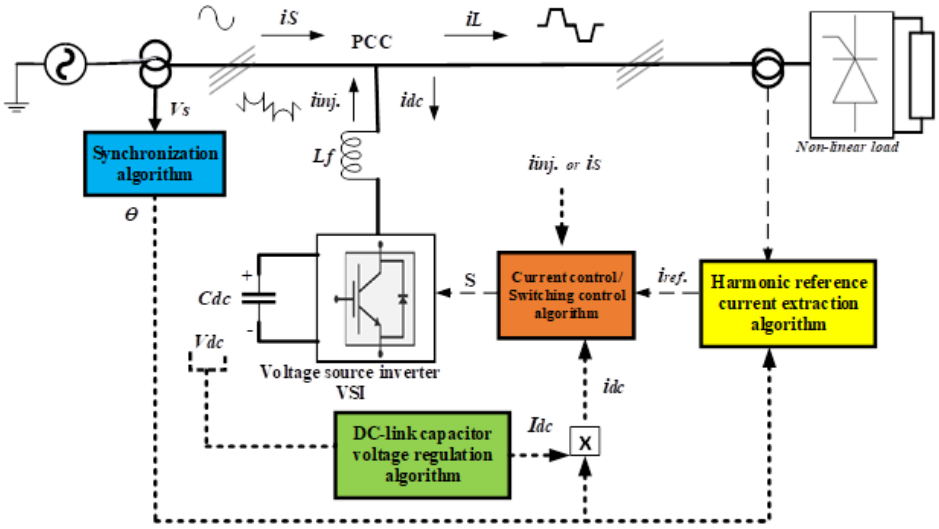

Figure 3. Block diagram of a shunt APF

2.1. Mathematical analysis of SDFT method for harmonic extraction algorithm and synchronization algorithm

The harmonic extraction algorithm and the synchronization algorithm is discussed in this section. The FT concept is revisited in this study, which employs a time-domain analysis to analyze the undesirable qualities associated with off-nominal grid frequency. The FT formulation in a sliding mode is explored in length in [9], as is the mathematical analysis for estimating phase and magnitude errors under off-nominal frequency conditions. The main advantage of the implementation described in [9] is the cancellation of the double frequency oscillation by adding together the sine components of the three phases and the cosine components. Also, the variable window length and the continuous adjustment of the window length to the input period makes the algorithm fully adaptive to frequency variation and enables the generation of accurate phase angle, frequency, and magnitude information of the input three phase signal. Figures 4 and 5 outline the main mathematical manipulations of the algorithm.

We opted SDFT-PLL technique for extracting the fundamental load because this technique is fast and accurate; it involves the cancellation of the double frequency oscillation that can be found in typical implementation of sliding discrete Fourier transform. The PLL component also provides adaptability to frequency variation which can be found in weak microgrids powered be distributed energy resources. Once the fundamental load current is fount, the harmonic reference can be easily obtained and also the displacement angle for controlling reactive power injection.

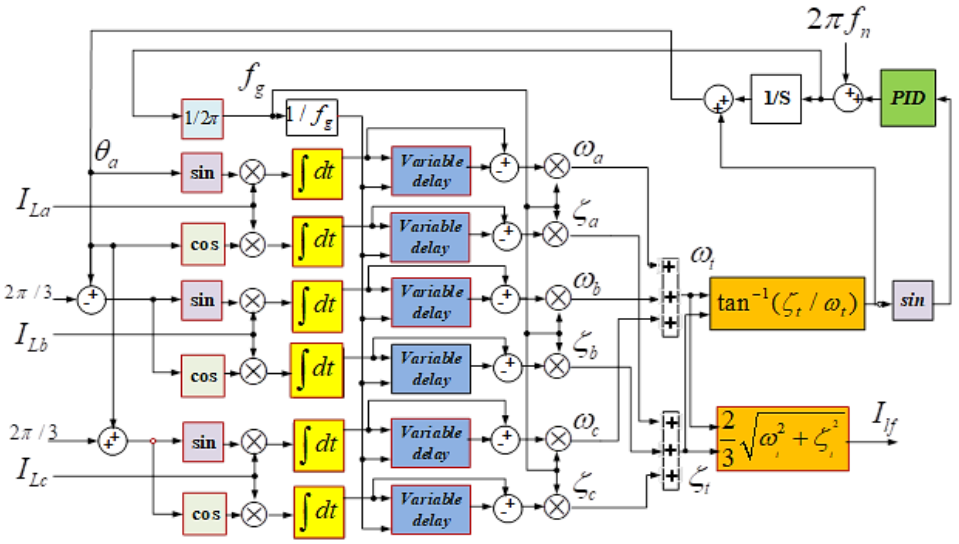

Figure 4. SDFT-PLL based fundamental load current extraction

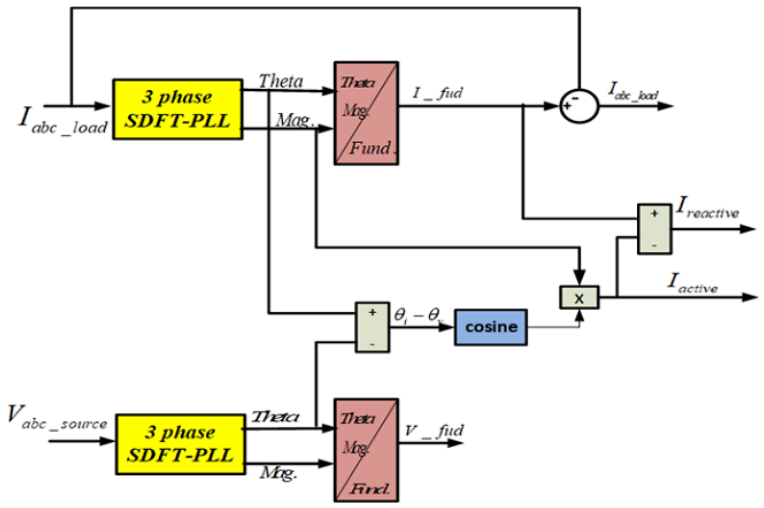

Figure 5. SDFT analyzer

2.2. Algorithm for controlling the voltage of a DC-link capacitor

Shunt PI or a fuzzy logic controller (FLC) can govern the dynamic response of the active power filter (APF). In recent trends, artificial intelligence technologies such as artificial neural networks and genetic algorithms are being applied. Artificial Intelligence has made significant improvements in electrical and electronic engineering with many applications in motion control and power electronics. The actual VDC act. of the DC side capacitor is measured and compared to a reference voltage $V_{DC\ (ref)}$. The error $e = V_{DC\ (ref)} - V_{DC\ act.}$ is used as an input to PI controller. An adequately constructed low pass filter is used to route the erroneous signal. The cut-off frequency of the LPF filter is 50 Hz, which allows it to suppress higher order components while allowing just fundamental components. The link DC voltage can be kept constant at its reference value by losses calculation in the circuit using (1).

$$I_{loss} = K_p\left(V_{DC\ ref} - V_{DC\ act.}\right) + K_i \int \left(V_{DC\ ref} - V_{DC\ act.}\right) \quad (1)$$

Where K_p is the proportional constant which governs the DC-side voltage control's dynamic responsiveness, while K_i is the integral constant which defines its settling time. The PI controller eliminates the inaccuracy of the steady-state in the DC-side voltage. The PI controller output is regarded as the maximum supply current value (I_{max}), which provides the losses component of the APF and the fundamental active power component of load current. To acquire the reference compensating currents, multiply the peak value of the current (I_{max}) by the unit sine vectors in phase with the related source voltages. These estimated reference currents (I_{sa*}, I_{sb*}, I_{sc*}) are added to the harmonics elimination reference currents. The detected currents were then compared to real currents (I_{sa}, I_{sb}, I_{sc}) at a hysteresis band, yielding the APF signals of gating [18]-[22].

2.3. Current control algorithm (pulse width modulation (PWM) technique)

The voltage source inverter (VSI) produces a three-phase voltage source with variable amplitude, frequency, and phase. The VSI is set to ensure that the inverter's output currents are forced to follow their predetermined reference currents. The basic idea is based on a comparison of the real and reference currents produced by different extraction techniques. VSI inverters can be controlled in a variety of ways, including hysteresis current control, sinusoidal pulse width modulation and space vector PWM control (SVPWM) that used in this paper. Many SVPWM designs have been extensively studied in the literature. Each modulation strategy is designed to reduce switching losses, boost bus usage, reduce harmonic content, and maintain precise control [23]-[25].

In the proposed extraction algorithm, there are two modes of reference current calculation. Figure 6 shows a Mode 1 selector for activating/deactivating harmonic cancellation and a Mode 2 selector for activating/deactivating reactive power compensation. Figure 7 depicts the proposed system's inverter gating control block diagram. This system consists of a three-phase source voltage linked to a thyristor converter that powers a DC motor. The SAPF is a VSI with six-switches having the combination of both compensating and filtering component. This active filter is capable of detecting harmonic currents and canceling them by injecting compensating current. As a result, the current flows as a sine wave of fundamental frequency. The PI controller is used to keep the DC voltage constant.

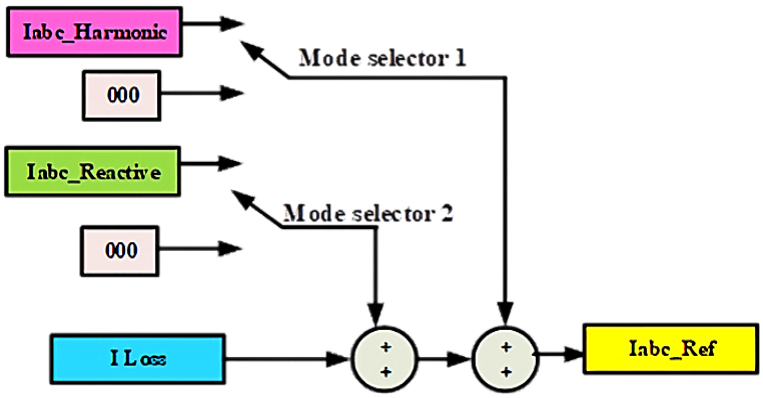

Figure 6. Mode 1 / Mode 2 selector block diagram

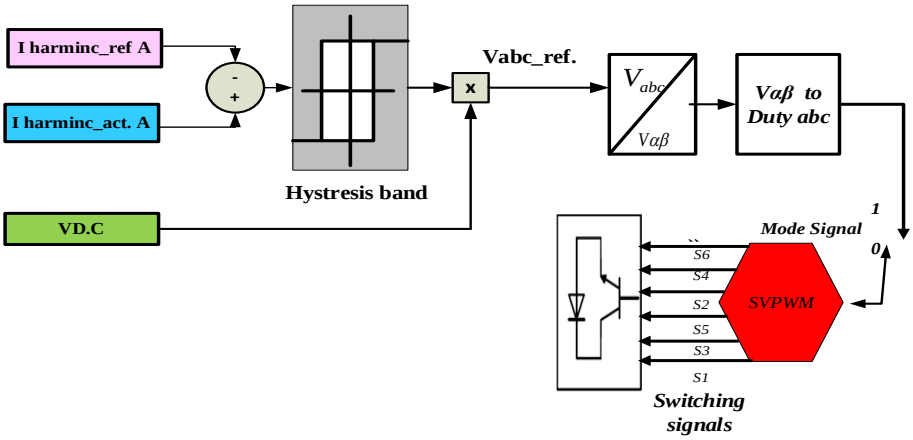

Figure 7. Inverter gating control block diagram for the proposed system

3. SIMULATION RESULTS AND DISCUSSIONS

Simulations using MATLAB/Simulink program verify the new approach's performance in a variety of operational scenarios. The parameters of the system listed in Table 2 are used. The overall simulation system is shown in Figure 8. The charging resistance is used to charge the capacitor for its initial charge. The system is powered by three-phase balanced voltage sources that feed a three-phase thyristor converter coupled to a DC motor. The coupling circuit depicted in Figure 9 connects the filter to the point of common coupling (PCC). The simulation is divided into three scenarios. The first scenario includes SAPF deactivated. The second scenario involves utilizing the d-q algorithm to activate SAPF for harmonics elimination and reactive power compensation. The third scenario is SAPF activated for harmonics elimination and reactive power compensation using the novel SDFT algorithm. Both algorithms are compered to validated the novel algorithm.

The simulation time step is elected so small that a PWM cycle (100 us) can be populated with approximately 100-time step to enable sufficient PWM resolution being captured into system dynamics. The periodic time of the control loops (100 us) and the sampling rate of the feedback analog measurements (10 kHz) is selected to be suitable to the execution speeds of known DSP normally used for such applications (100 us) and for their A/D converters speed. The simulation mode is discrete with fixed step (1 us) to mimic the real system with DSP controllers. The coupling inductor should be sized such that the harmonic component of the compensation current at the switching frequency should not exceed 5% of the fundamental of the load current to limit the high frequency ripple in the source resultant current. The dc voltage should be adjusted so that:
Vdc/2-Vac (peak)>maximum rate of change of load current * coupling filter inductance
According to the choices made here:
Vdc/2 = 450/2 = 225, Vac peak = 208, then Vdc/2-Vac peak = 225-208 = 17 volt. The $L_{coupling}$ = 2e-3, then maximum rate of change of load current should not exceed (1/2e-3) *17 = 17*500 = 8.5 KA/s. If load current was found to have higher rate of change, consider increasing the inductance of the rectifier smoother inductance to slow it down. The capacitor value of the DC link should be sized such that the ripple voltage is within 2% of the DC voltage Vripple = Vmax - Vim, Vripple/Vdc<2%. We use the PID controller and not PI as, a PI controller is used since the D component of the PID has a zero coefficient.

Table.2. System variables

	Parameters	Value
Source	Peak voltage	170 V
	System frequency	50 Hz
	Source impedance	R = 0.01 Ω, L = $1e^{-3}$H
Load	Three phase thyristor converters	Armature resistance R = 1Ω,
		Armature inductance L = $20e^{-3}$ H
		DC motor back EMF = 120
	AC input smoothing filter for thyristor rectifier	R = 0.01 Ω, L = 8 mH
SAPF	V_{DC}	450 V
	DC-link capacitor	2200 µ F
	Coupling circuit	RL coupling: R = 0.01Ω; L = 2e-3 H
	PI controller for d-q	RC coupling: R = 500 Ω; C = 0.5 µF
	PI controller for SDFT-PLL	K_p = 0.7 K_i = 0.999
	Charging resistance	Kp = 1, Ki = 200
	MATLAB simulation time	R = 10 Ω
		1e-6

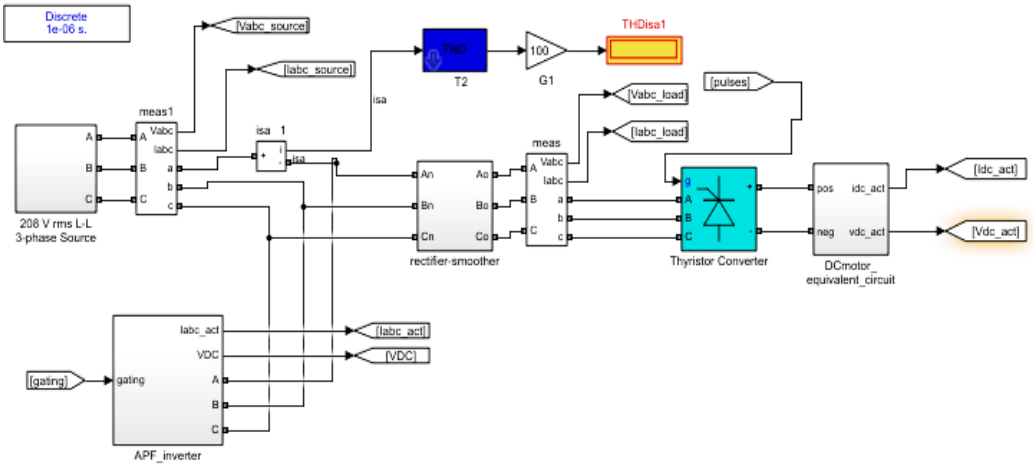

Figure 8. Overall simulation system

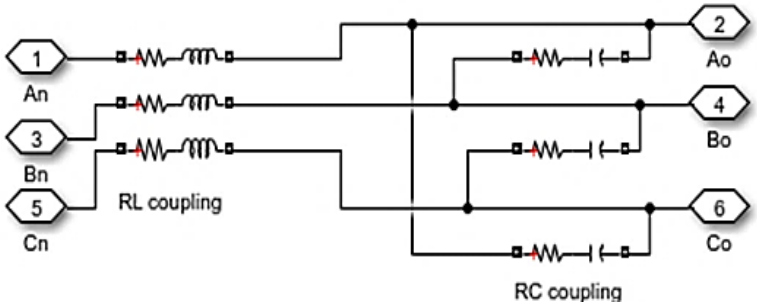

Figure 9. Coupling circuit to PCC

3.1. First scenario: SAPF deactivated

The first simulation scenario examines the, source current, THD and load current when the variable profile of the thyristor bridge rectifier's reference current varies from 10 to 25 A after 0.1 s. Load and source current is fully distorted as shown in Figure 10. Figure 11 depicts the source voltage and current. The source current and voltage are clearly out of phase, indicating a low power factor for the system, while the source voltage is sinusoidal. The THD of the source current is 23.67% and the harmonic spectrum

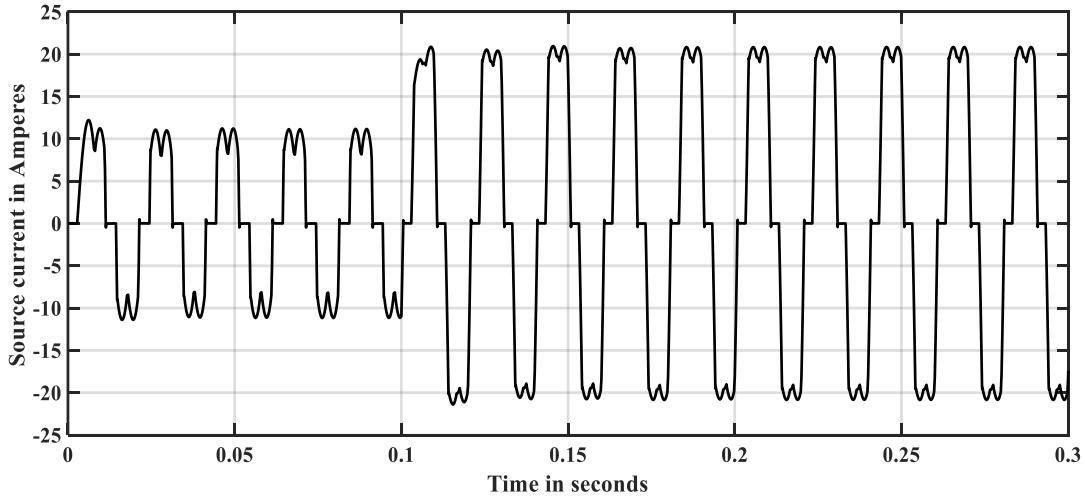

Figure 10. Source current and load current before compensation

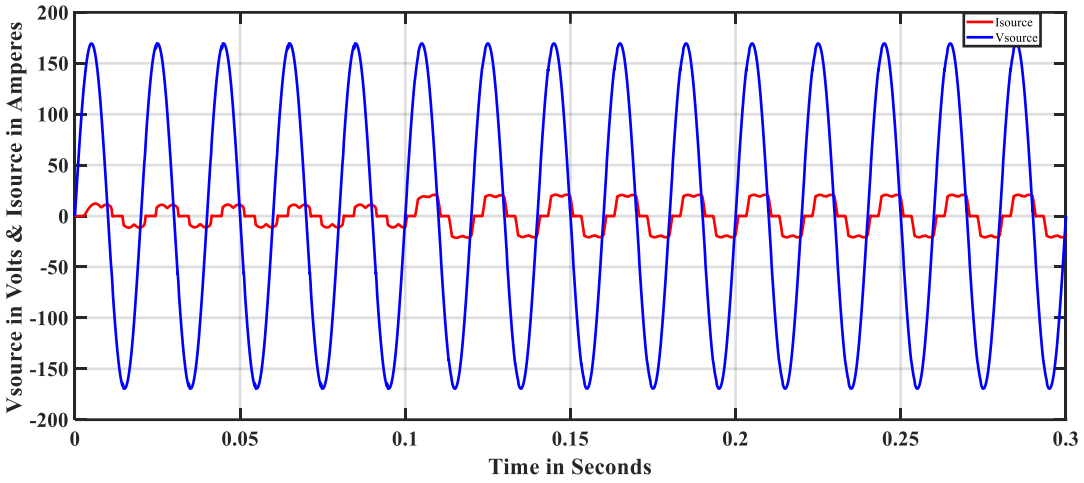

Figure 11. Source current and voltage before compensation

3.2. Second scenario: SAPF activated using d-q for harmonic extraction and reactive power compensation

The second simulation scenario attempts to evaluate the performance of the SAPF via the well-known d-q method for harmonic extraction and a conventional PI controller for the SAPF's DC link. After 0.1 s, a changing profile of the reference current of the thyristor bridge rectifier is applied. Thus, the system performance is observed under sudden load changes. The system is controlled by a traditional PI controller, with the parameters of the "Ziegler Nichols" formula set (KP = 0.7 and Ki = 0.999). The results from Figure 12 show that there is an improvement in the system behavior while utilizing SAPF to mitigate harmonics and compensate for reactive power. From Figure 12 the power factor approximately reached unity. After 0.05 seconds, the SAPF is linked to the system. In this scenario, there is an external circuit for PLL to synchronize the SAPF voltage with the gird voltage.

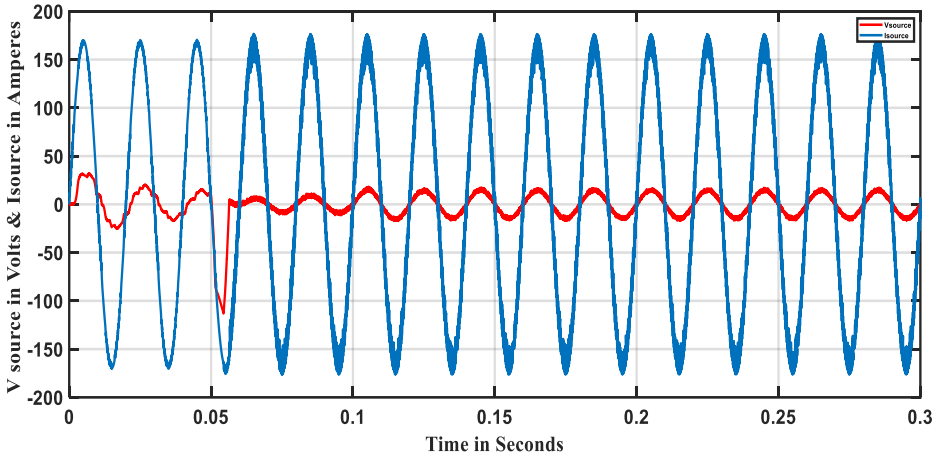

Figure 12. Source current and voltage after dq-SAPF

When the compensating current is injected in the PCC, the source current became completely sinusoidal. The compensation is started after 0.05 seconds. The THD after using SAPF is improved and reduced 8.82% that is outside limits of the IEEE 519-1992 standard [22]. The DC side voltage is maintained constant at 450 volts as a reference value as shown in Figure 13 despite the sudden change at 0.1 second. It immediately achieves the reference value, indicating that the PI controller is performing optimally. A small disturbance happened at 0.1 second when the load increases suddenly and it just takes 0.013 second to attain the steady state value of 450 V. The steady-state error was less than 2 V, or 0.45% of the reference value.

3.3. Third scenario: SAPF activated using SDFT algorithm for harmonic extraction and reactive power compensation

The third simulation scenario aims to examine the performance of the SAPF using the novel SDFT algorithm for harmonic mitigation and classical PID controller for DC link control of the SAPF for the same previous load simulation conditions. The PID controller parameters are (KP = 1 and Ki = 200). The results from Figure 14 show that there is considerable improvement in the system behavior when using the innovative SDFT method to detect harmonics and compensate for reactive power. In this scenario, the PLL for SAPF voltage synchronization with the gird voltage is done by the novel SDFT algorithm selectively and individually without additional PLL. The reference harmonic current and the reactive current can be easily separated using this approach. As a result, the system is capable of performing harmonic mitigation and/or reactive power compensation.

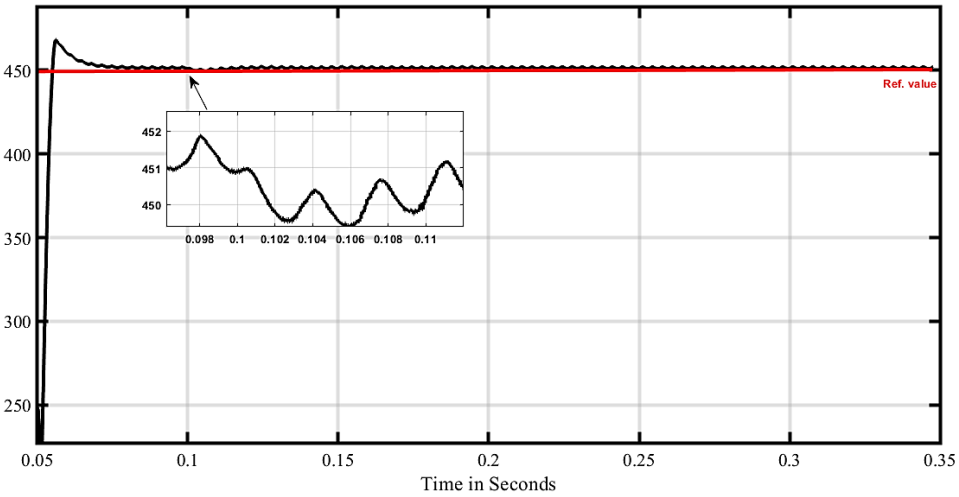

Figure 13. DC link voltage of SAPF

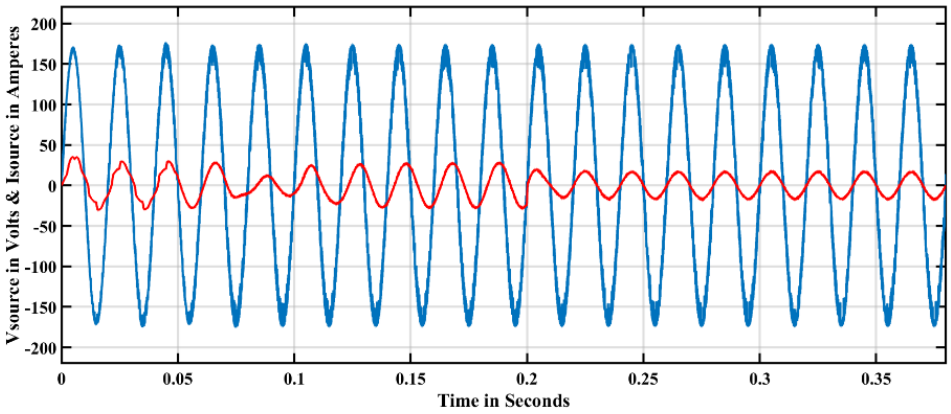

Figure 14. Source current and voltage after SDFT- SAPF

In Figure 14, from 0 sec. to 0.05, the source current is non-linear, from 0.05 to 0.1 seconds. The harmonic mitigation process is initiated, and the source current becomes sinusoidal but out of phase with the source voltage. The rapid shift in load occurred at 0.1 seconds and the current increased. The reactive power adjustment is activated after 0.2 seconds. Thus, the power factor approximately reached unity. Both the voltage and current waveforms looked to be in phase. Figure 15 depicts the reference harmonic current and the reactive current of the load separately. The THD after using SAPF is improved and reduced by 8.82%.

Despite the abrupt change at 0.1 seconds, the DC side voltage remains constant at 450 volts as seen in Figure 16. It immediately achieves the reference value, indicating that the PI controller is performing optimally. A small disturbance happens at 0.1 seconds when the load increases suddenly and it just takes 0.02

seconds to attain the steady state value of 450V. The steady-state error was less than 5 Volts, or 1.1% of the reference value. Table 3 shows the THD for the three scenarios and the difference between the two harmonic mitigation algorithms used. It is clear that before compensation the THD is 23.6% which is high with respect to IEEE standard. After compensation using the d-q algorithm for both harmonics and reactive power compensation the THD is decreased to 8.82%. This value is high which indicated that the d-q algorithm is not effective in our case study. The THD is decreased to 4.37% after using SDFT algorithm for harmonics mitigation only with switching off the reactive power compensation. This THD value is nearly as the IEEE recommended standard value (4%). The THD after switching on reactive power compensation using SDFT algorithm is 5.52%. The last result is effective because it enhances two terms, the harmonics and compensate the reactive power and THD is approximately near the recommended IEEE standard value.

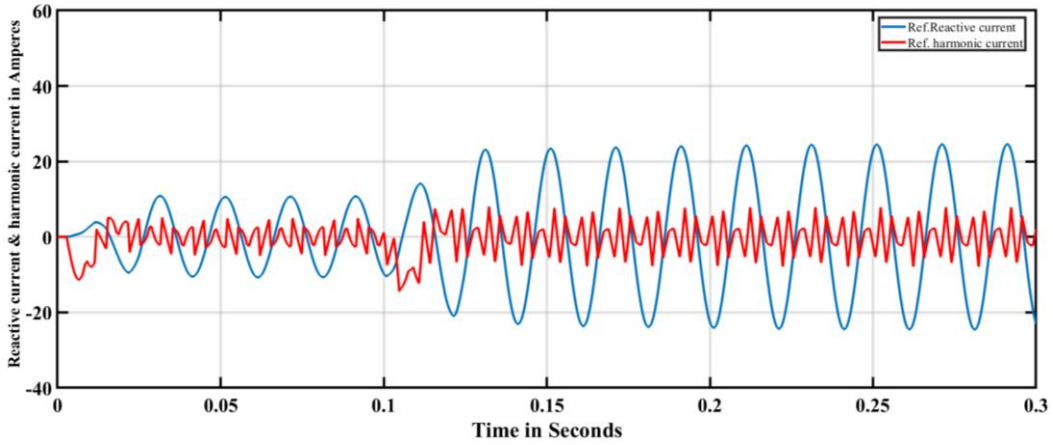

Figure 15. Reference harmonic current and reference reactive currents of phase A

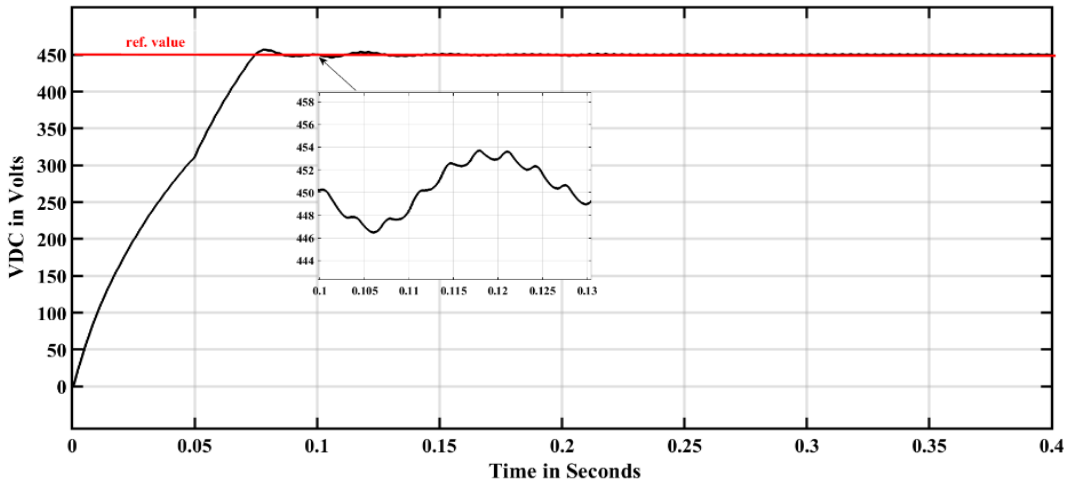

Figure 16. DC link voltage of SAPF

Table 3. THD for the three scenarios

THD%			
Scenarios	Values	Scenarios	Values
Before compensation	23.67%	Using SDFT algorithm for harmonic mitigation only	4.37%
d-q algorithm for both harmonics' mitigation &reactive power compensation	8.82%	Using SDFT algorithm for both harmonic mitigation and reactive power compensation	5.52%

4. CONCLUSION

Various harmonic current extraction approaches, such as sliding discrete Fourier transform (SDFT) and synchronous reference frame (dq-theory), are presented in this paper. The effectiveness of the

recommended SDFT control technique has been validated using computer simulations. According to the simulation findings, the proposed strategy was quite successful and simple to apply. THD decreases from 8.82% using d-q to 4.37% case of using SDFT which means it decreases to nearly half its value and became closer to IEEE standard. It gives a good result for THD in case of both harmonics mitigation and reactive power compensation with THD equals 5.52% which needs more improvement to meet the IEEE standard value. Future work shall include a hardware-in-the loop implementation and a practical implementation of the described technique on a lab scale setup to demonstrate its distinguished performance.

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