International Journal of Power Electronics and Drive Systems (IJPEDS)
Vol. 15, No. 4, December 2024, pp. 2452~2461
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v15.i4.pp2452-2461

Digitally fast synchronization of single-phase grid-tied inverter using FPGA

Afarulrazi Abu Bakar[1], Balarajan Sannasy[2], Hazwaj Mhd Poad[3], Tharnisha Sithananthan[2], Wahyu Mulyo Utomo[2], Nor Farisha Diana Rosli[2]
[1]Centre of Research Electric Vehicle, Faculty of Electrical and Electronic Engineering, Universiti Tun Hussein Onn Malaysia, Batu Pahat, Malaysia
[2]Department of Electrical Engineering, Faculty of Electrical and Electronic Engineering, Universiti Tun Hussein Onn Malaysia, Batu Pahat, Malaysia
[3]Faculty of Technical and Vocational Education, Universiti Tun Hussein Onn Malaysia, Batu Pahat, Malaysia

Article Info

Article history:

Received Jan 3, 2024
Revised Apr 27, 2024
Accepted May 22, 2024

Keywords:

Digital PLL
Digital switching
Grid synchronization
Unipolar SPWM
ZCD component

ABSTRACT

As interest in alternative energy sources grows, grid-connected inverters are getting more advanced. Thus, to synchronize the output waveform of an inverter with the grid supply system, the frequency and phase angle ought to be consistent. This paper presents an enhanced digital implementation controller for a grid-connected inverter using the sinusoidal pulse-width modulation (SPWM) switching technique via an appropriately designed low-pass filter. The main contribution of the proposed digital controller algorithm is to synchronize with the grid for the next half-cycle. The proposed control technique used the integrated response from the zero-crossing detector (ZCD) circuit for every half-cycle to trigger the digital phase-locked loop (PLL) implemented using field-programmable gate array (FPGA). An experimental 100 W single-phase full-bridge inverter prototype tested and validated the proposed control algorithm to prove the switching approach works. From the experimental results, the proposed control algorithm demonstrates synchronization with the grid voltage within 8 ms during startup. Furthermore, it exhibits the ability to adapt to phase changes when subjected to a distorted grid, achieving synchronization within 42 ms. This research also emphasizes synchronization between the grid waveform and the inverter output via the phase angle difference.

Corresponding Author:

Hazwaj Mhd Poad
Faculty of Technical and Vocational Education, Universiti Tun Hussein Onn Malaysia
Batu Pahat, Johor 86400, Malaysia
Email: hazwaj@uthm.edu.my

1. INTRODUCTION

Recently, research on grid-connected systems has increased tremendously in accordance with the rapid development of the use of renewable energy (RE) resources to produce electricity. The massive global transition towards sustainable and green energy is significantly influenced by the ongoing increase in global energy demand and the associated environmental effects, where a significant contributor to carbon dioxide emission is the electrical power industry. As a result, the integration of RE into electricity grids has received economic, environmental, and technical attention recently [1]. Furthermore, the use of electric vehicles (EVs) is also growing tremendously due to the increasing cost of energy from continuously depleting natural resources. Modern technologies, such as vehicle-to-any devices (V2X), vehicle-to-building (V2B), and vehicle-to-home (V2H), are more tightly linked to grid synchronization strategies and are becoming

increasingly popular and growing rapidly. The electricity supply from renewable energy resources is now being spotlighted, and when the stored renewable energy exceeds load requirements, the excess energy can be fed back to the grid via synchronizing grid-tied inverters [2]. Inverter-based resources act as grid-following inverters in the grid-connected mode since the grid controls frequency and voltage [3].

Besides that, grid synchronization is crucial for a system's ability to synchronize with the grid during abnormal conditions, voltage spikes, and frequency variations due to nonlinear loads. Frequency, phase angle, and amplitude of voltage are the most important parameters that need to be measured and controlled during grid synchronization between the grid signal and generated signal [2], [4]. The most critical consideration confronted during grid synchronization is a clear analysis of frequency, phase-angle, and grid voltage magnitude, and as a result, numerous grid synchronization solutions have been published in the literature over the previous few decades [2], [5]-[23]. The use of renewable energy often tops the list of measures that could possibly be taken to mitigate the most severe consequences of the increasing global temperature in any discussion of climate change. This is because the use of renewable energy resources, such as solar and wind energy, can help reduce the emissions of carbon dioxide and other greenhouse gases, which significantly contribute to global warming.

In inverter systems, various switching techniques have been introduced, such as square wave modulation, pulse-width modulation (PWM), sinusoidal pulse-width modulation (SPWM), and space-vector pulse-width modulation (SVPWM), which have their respective advantages and disadvantages. SPWM mechanism compares the reference voltage waveform with the carrier waveform, a triangle waveform, to transform a direct current (DC) power source into an alternating current (AC) power supply. The SPWM switching technique is commonly used due to the ease of implementation, less complexity, and significant reduction in total harmonic distortion (THD) with minimized filtering requirements. This study's research gap analysis describes in depth the comparison between the proposed research and prior models described in previous research works. Table 1 shows the research gap between the proposed research and previous work. The comparison is segregated into the operating phase, type of controller used, filter design, synchronization method, phase difference issue, and settling time of synchronization, which are identified in detail [23]-[26].

Based on Table 1, most of the research employed a low-pass LC filter, instead of the LCL and other types of filters, to decrease the THD of the inverter output due to its simplicity. In contrast to the the zero-crossing detector (ZCD) system, the phase-locked loop (PLL) system can be accurately synchronized with the grid, according to [23]. Table 1 also shows that most researchers used the field-programmable gate array (FPGA) as the controller to trigger the inverter's gates due to its superior performance [25]. The FPGA is often used to perform multiple operations simultaneously, is more versatile, and does extremely well in tasks that require high parallelism and custom logic design. Furthermore, the use of FPGA can also address several issues with the source device's interface, including lower power consumption, smaller circuit size, ease of implementation due to program changes that don't require altering the hardware, and flexibility in terms of switching parameter changes [27]. It is worth highlighting those systems with fewer numbers of converters require multiple clock domains with different frequencies, which can operate independently and simultaneously. However, this system could be applied to PI controllers using SPWM techniques [28], [29].

Table 1. Comparison between the proposed research and previous works

Author	Year	Phase	Grid-tied inverter type	Controller/simulation	Filtering and technique	Settling time for phase matching (ms)
[24]	2015	3-Φ	Microgrid-connected voltage-source inverter (MVSI)	TMS320LF28335 DSP	LC filter	150
[26]	2015	1-Φ	Voltage-source inverter	MATLAB/Simulink	LCL filter & ZCD and PLL	150
[25]	2016	1-Φ	Virtual unit delay (VDU)	dSPACE DS 1103	LCL filter & T/4 delay PLL	100
[23]	2020	3-Φ	Bi-directional inverter	DSP/PI controller	Low-pass filter/ SRF PLL	N/A
Proposed	2024	1-Φ	1-Φ full-bridge inverter	FPGA	Passive low-pass LC filter & ZCD component	8

Aside from that, synchronization issues were observed in terms of the phase angle difference between the inverter output and grid voltage waveforms [23]. Particularly, frequency and voltage matching synchronization during initiation was observed in prior grid synchronization studies and the following research works employing a variety of advanced phase-locked loop (PLL) approaches [24]-[26]. A few grid-tied inverter applications proposed by previous researchers that mainly focused on PLL techniques were studied in detail.

In this research study, a grid-connected inverter is proposed via the digital implementation based on the FPGA. The controller was designed to achieve fast synchronization of the proposed inverter's output voltage with the grid system with minimal THD, as well as producing a pure sine wave via the integration of

the ZCD component and implementing a passive low-pass LC filter to mitigate the third harmonic. It is necessary to determine grid voltage polarity with maximum speed and precision. Also, for grid-tied inverters to be controlled and operated reliably, quick, and accurate tracking of grid voltage properties is necessary [30]. The origins of fast polarity detectors can be traced to ZCDs, which are sometimes the same device. In grid synchronization, the ZCD plays a major role, as zero-crossing methods are more sensitive to the harmonics present in a signal [31]. PLL systems can synchronize two signal phases, give information about signal phase differences, and maintain stable operation and control of grid-connected inverters [32]. PLL systems cannot give precise information about zero crossing. However, zero-crossing detection is necessary in some applications, such as direct AC/AC converters [27] or solid-state relays. The rest of the manuscript was organized as: i) section 2 consists of the research methodology of the proposed system, ii) section 3 consists of the proposed digital switching control strategy, iii) section 4 documents the results and detailed analysis of the experimental output of the research, and iv) section 5 concludes the overall manuscript.

2. NOVELTY AND CONTRIBUTION OF PROPOSED DESIGN

The primary contribution of this paper is developing a fast grid synchronization with the grid system within the next half-cycle. During synchronization initiation, frequency matching was conducted based on a fixed tolerance of 99.5% at a frequency of 50 Hz. The technique for adjusting the phase delay of the inverter output considered the LC filter, which introduced inherent characteristics such as capacitance and inductance. The hardware description language (HDL) was used to digitally program compensation for the delayed time due to delayed filter response time. HDL design analysis and synthesis allow developers to create their designs, analyses timing, look at register-transfer level or RTL diagrams, test how a design responds to various stimuli, and set up the target device using a programmer [33]. The digital implementation of the grid-connected single-phase inverter for fast synchronization was based on the ZCD signal as the input, and the digital PLL was used to trigger unipolar SPWM switching signals. In addition, the use of a suitable LC filter was also proposed to mitigate the THD and produce a pure sinusoidal waveform at the output.

2.1. System configuration

The proposed system configuration consisted of an FPGA board, a gate driver unit, an LC filter, a ZCD circuit, a full-bridge inverter, an isolation transformer, and a step-up transformer. Figure 1 shows the complete block diagram. It is of the proposed fast-synchronization grid-tied inverter.

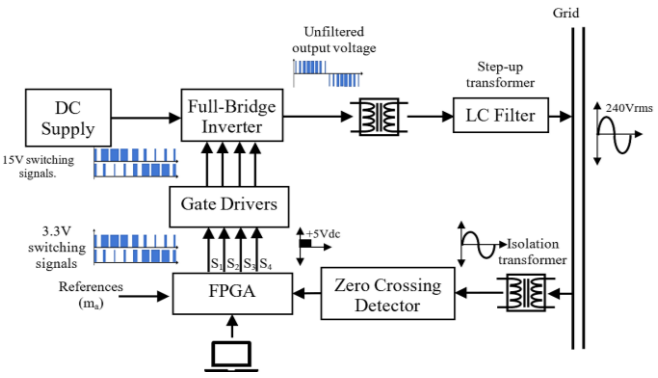

Figure 1. Block diagram of grid-tied single-phase full-bridge inverter using FPGA-based control system for fast synchronization

The SPWM switching signals with the adjustable modulation index, ma, from the FPGA board will be connected to the circuits of the gate drivers' (S_1, S_2, S_3, and S_4) before being connected to corresponding switches. Besides providing isolation, the gate drivers will boost the signal's voltage from the FPGA ($3.3V_{DC}$) to ensure an adequate amount of current passed through from the drain to the source terminal of the MOSFETs. The FPGA board continuously examined the digital signal from the ZCD and generated the SPWM switching signals for every half-cycle. The ZCD was employed to validate the recent status of the grid waveform either in the positive or negative cycle. This condition will ensure that the signal is in an appropriate sequence by detecting the positive half-cycle of the grid and converting it into a square wave ($5V_{DC}$) with the least phase delay between the grid waveform and the ZCD output signal. Thus, based on the ZCD component's input, the FPGA will emit a positive-generating half-cycle SPWM signal to generate a positive sine wave and concurrently emit a negative-

generating half-cycle SPWM signal to generate a negative sine wave. In addition, the unfiltered output from the full-bridge inverter will be filtered by the filter to produce a pure sine wave. Finally, the output waveform will be stepped up to match the magnitude of grid voltage before being distributed to the grid system.

3. PROPOSED DIGITAL SWITCHING CONTROL STRATEGY

Digital switching control is mainly implemented to control switching signals, which can offer greater precision. Thus, the designed digital PLL using the integration of the ZCD is discussed in detail in this section. In digital switching, the binary code refers to two possible states of 1 or 0, which are high and low signals, respectively, allowing for accurate and noise-resistant transmission of the control signal. In this proposed control system, the HDL coding played a significant role in achieving fast synchronization by integrating the ZCD input with the ZCD component of the digital PLL, where the ZCD was used to produce an output with high-precision zero-cross timing of the targeted AC voltage. Then, the selected FPGA board will emit a digitalized unipolar SPWM switching signal for either positive or negative sinusoidal waveform generation based on the ZCD output. As in Figure 2, the ZCD output will be a high signal when a positive sinusoidal waveform is detected and a low signal when a negative sinusoidal waveform is detected. The SPWM switching signals for both the positive and negative sine wave signals will be assigned based on the switching time recorded in the look-up table (LUT). The switching signals will be generated according to the established switch hierarchy (S_1, S_2, S_3, and S_4) for every half-cycle programmed in the HDL code. The generated SPWM switching waveform will be updated for the next half-cycle to achieve fast synchronization. Thus, the digital output from the ZCD will enable the counter to count based on the clock references set earlier.

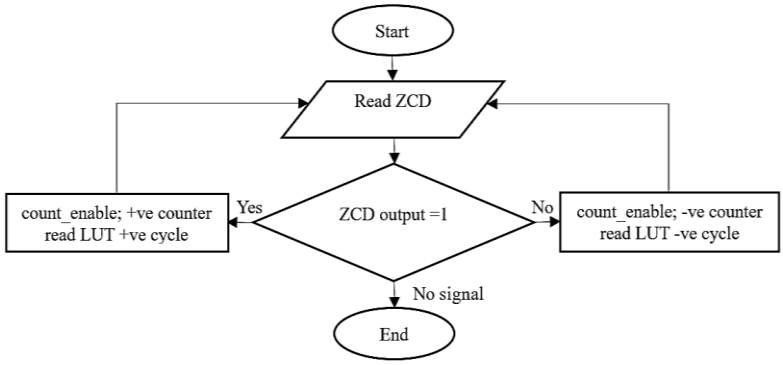

Figure 2. Control algorithm for fast synchronization of grid-tied inverter

3.1. Digitalization of unipolar SPWM switching signals

Generally, switching signals are fundamental to digital circuits and crucial to controlling the whole system. Hence, Table 2 illustrates a digitalized time scale developed for the unipolar SPWM switching signals for S_1 and S_4. The positive and negative for one complete cycle can be represented as 20000 counters (20 ms), where each counter was equal to 1 µs. To realize fast synchronization within half a cycle of the grid, the counters were set to 10000, which equaled 10 ms, corresponding to the signal from the ZCD signal to enable the independent counter assigned for switches S_1, S_2, S_3, and S_4. The signal for S_4 is the opposite of that for S_1, while the signal for S_3 is the opposite of that of S_2. (1)-(3) were employed to calculate the values of the rising edge (α_n) and falling edge (β_n) of the switching signals, as well as the pulse width in terms of time.

$$\alpha_n(t) = \alpha_n(^\circ) \times \frac{T}{180^\circ} \quad (1)$$

$$\beta_n(t) = \beta_n(^\circ) \times \frac{T}{180^\circ} \quad (2)$$

$$Width\ (t) = \beta_n(t) - \alpha_n(t) \quad (3)$$

3.2. Designing FPGA-based controller

Quartus II software digitized the SPWM switching signals obtained from the MATLAB/Simulink logic analyzer. To generate the digital unipolar SPWM switching, the counter would count in microsecond time-series format, which is the suitable FPGA operating clock frequency closely related to the number of bits assigned in the counter. Therefore, the operating clock was obtained based on the number of carrier waveforms

and the reference signal. Figure 3 depicts the block design of the proposed system for the unipolar SPWM generator with fixed parameters (m_a = 0.99 and $f_{carrier}$ = 1 kHz) to provide an output voltage of approximately 240 V_{rms}. In addition, the if-else counter HDL coding format was utilized in this FPGA-based controller to automatically generate the proposed digital SPWM switching signals for either positive or negative sinusoidal waveform generation based on ZCD integration to accomplish fast synchronization of inverter output voltage with the grid voltage. PIN_AD15 was connected to a 25-MHz internal clock connected to the clk_div circuit. The clk_div circuit was programmed to produce multiple output clocks, which were then connected to the lpm_counter function. Besides that, a code was created in VHDL (.vhd) and then converted to a block diagram (*.bdf). It consisted of functions altpll, lpm_counter, and comparator.

Using (4), the clock frequency was calculated to generate clock signal output based on the clock frequency connected to the input of the lpm_counter, which would activate the positive or negative digital SPWM coding of blocks with the ZCD function. In addition, the activation of lpm_counters0 and lpm_counter1 in response to the ZCD input would allow the fast synchronization of the grid-connected inverter, and to prevent communication error during fast synchronization, the ZCD signal required a comparator, which would generate the same signal as that of the ZCD.

$$f_{clock} = \frac{1}{T_{unit}} \tag{4}$$

Table 2. Unipolar SPWM time scale data for m_a = 0.99 and $f_{carrier}$ = 1 kHz

$S_1, \overline{S_4}$		Degree			Time (ms)			$S_2, \overline{S_3}$		Degree			Time (ms)		
		α (°)	β (°)	Width (°)	α (°)	β (°)	Width (°)			α (°)	β (°)	Width (°)	α (°)	β (°)	Width (°)
+ve cycle	1	8.37	19.10	10.73	465	1083	618	-ve cycle	11	9.77	17.01	7.24	543	929	386
	2	25.13	38.09	12.96	1396	2155	759		12	29.20	34.11	4.91	1622	1863	241
	3	42.03	56.83	14.80	2335	3209	874		13	48.35	51.37	3.02	2686	2809	123
	4	59.18	75.26	16.07	3288	4240	952		14	67.12	68.85	1.73	3729	3771	42
	5	76.68	93.37	16.69	4260	5247	987		15	85.46	86.63	1.17	4748	4753	5
	6	94.57	111.15	16.58	5254	6229	975		16	103.36	104.74	1.39	5742	5760	18
	7	112.91	128.63	15.71	6273	7191	918		17	120.85	123.17	2.32	6714	6791	77
	8	131.69	145.89	14.20	7316	8137	821		18	138.01	141.91	3.91	7667	7845	178
	9	150.84	162.99	12.15	8380	9071	691		19	154.91	160.90	5.99	8606	8917	311
	10	170.28	180.00	9.72	9460	10000	540		20	171.68	180.00	8.32	9538	10000	462

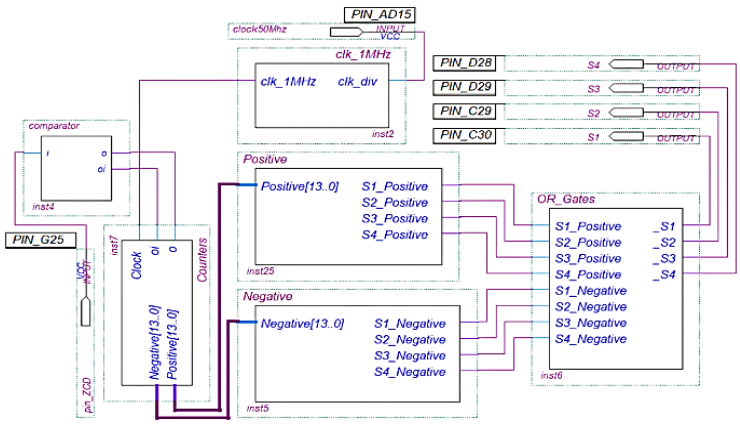

Figure 3. HDL block for synthesized on FPGA (*.bdf)

3.3. LC filter design for THD mitigation

In this analysis, the LC filter was constructed based on a specific inverter output rating, which was a lesser power rating utilized for experimental grid synchronization. Other parameters, including the ripple factor of the maximum output current, are given in Table 3. The parameter values were calculated using (5) to (9) to determine the components' values for experimental analysis. Using (5), the ripple factor of the inductor's current can be calculated based on 20% of the ripple factor.

$$\Delta I_L = \%\, ripple \times I_{o(RMS)} \tag{5}$$

Using (6), it was possible to calculate the inductance value based on the ripple factor of the inductor's current, considering the unipolar SPWM triangular carrier frequency of 1 kHz and DC voltage input of 24 V.

$$L = \frac{V_{DC}}{[4 \times \Delta I_L \times f_{Switch}]} \quad (6)$$

Using (7), it was possible to calculate the capacitance value based on the inductance value derived from (6), while (8) and (9) to calculate the fundamental cut-off frequency which are derived from (7).

$$C = \left[\frac{10}{2 \times \pi \times f_{switch}}\right]^2 \times \frac{1}{L} \quad (7)$$

$$f_{cut-off} \leq \frac{f_{Switch}}{10} \quad (8)$$

$$f_{cut-off} = \frac{1}{2\pi\sqrt{LC}} \quad (9)$$

Table 3. Inverter parameters in filter design

Parameter	Value	Parameter	Value
Input voltage, V_{DC}	24-48 V	I_o (rms)	8.3 A
Switching carrier frequency, f_{sw}	1 kHz	Ripple factor of output current, ΔI_L	20%
V_o (rms)	48 V	Output power, P_o	100-W

3.4. Hardware specification

The effectiveness of the proposed system was validated by using the prototype of a single-phase grid-connected inverter with the LC filter as shown in Figure 4. Meanwhile, Table 4 represents the hardware component parameters utilized in developing the proposed system prototype. The selected values of the components were based on manufacturer specifications for the hardware prototype implementation. Altera FPGA DE2 board served as the controller for driving the inverter gates. When a sinusoidal voltage waveform is detected, the controller receives an input signal from the ZCD-integrated PLL circuit from the isolation transformer to generate unipolar SPWM signals. All the synchronization data for the inverter system's output voltage waveform were collected and analyzed.

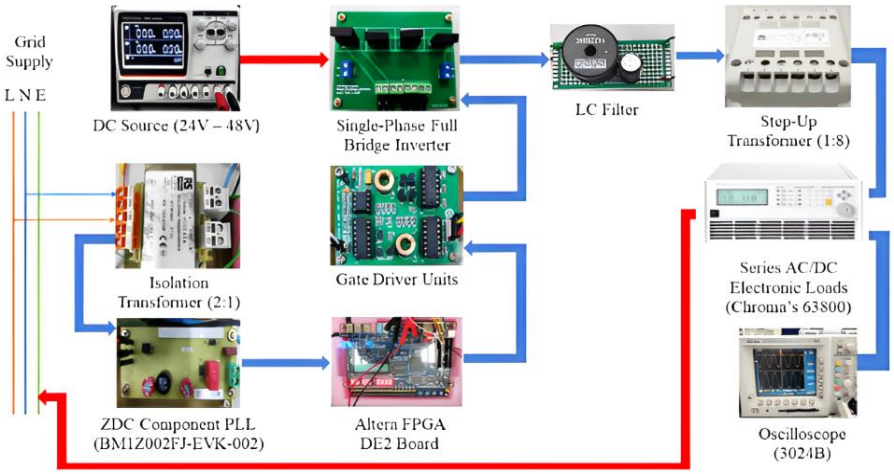

Figure 4. Hardware prototype setup

Table 4. Experimental component parameters

Component	Model/value	Component	Model/value
V_{DC} input	24 V	Isolation transformer	Class 1; 350 VA
MOSFETs	IRFZ44N	LC filter inductor	22 mH
Gate driver unit	3.3–20 V	LC filter capacitor	120 µF
Controller	Altera FPGA DE2	Step-up transformer	Class 1; 350 VA, transformer 1:10
ZCD	BM1Z002FJ-EVK-002		

4. RESULTS AND DISCUSSION

This section presents the results obtained from testing the proposed system. All measurements were recorded using a Tektronix TDS-3024B four-channel digital phosphor oscilloscope. This section includes a comprehensive analysis of the measured signal waveforms such as switching signals, unfiltered signals, and

filtered signals. Mainly, the output of the grid signal should be in-phase with unfiltered inverter output signal to obtain a grid synchronization. Figure 5 presents the grid voltage and the unfiltered inverter output. The unfiltered inverter output exhibits a square-wave-like pattern, which is a common characteristic of inverter systems. The analysis of the results obtained in Figure 5 indicates that both waveforms were in-phase. However, filtering techniques are typically employed to match the inverter output signal with the sinusoidal grid signal. This ensures a smoother power delivery and reduces the negative impacts of harmonics and distortions on the power grid and connected electrical equipment. Figure 6 shows the generated sinusoidal waveforms from inverter and grid. The obtained results demonstrate that the output voltage waveform was synchronized with the grid signal in terms of both voltage and frequency. However, there is a noticeable phase lag between the two waveforms, as seen by the shifted positioning of the filtered inverter output voltage peaks relative to the grid voltage peaks. The phase lag can be measured as approximately 6.84°.

Proper synchronization between the inverter output and grid voltage is crucial for efficient power transfer and grid integration. A phase lag can lead to reactive power flow, reduced power quality, and potential instability issues. Figure 7 depicts the sinusoidal waveforms with phase angle delay correction and the grid supply waveform with a magnitude of 240 V_{rms}. The compensation for phase angle delay was realized through HDL coding in the Quartus II software, with an adjusted phase angle of 6.84°. Figure 8 illustrates the output voltage of the inverter resulting from the proposed digital switching and the grid output voltage waveform. It demonstrates the synchronization of the generated voltage with the grid voltage was within 8 ms. The initial capacitor voltage was zero, and the voltage across the capacitor gradually increased, acting as a temporary energy storage device. The charging time was influenced by the capacitance value, the impedance of the load, and the resistance in the circuit. The capacitance value was initially calculated to be properly sized to handle the startup associated with the circuitry. It is shown that the digital algorithm offered high precision and accuracy with a smooth transition without overshoot. The ZCD signal enabled the counter to count the *n*-bits assigned, which adapted to any incurring phase change in the grid system.

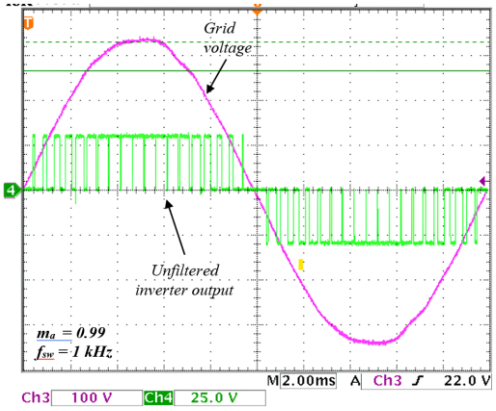

Figure 5. Output voltage waveform of unfiltered inverter signal and waveform of grid voltage

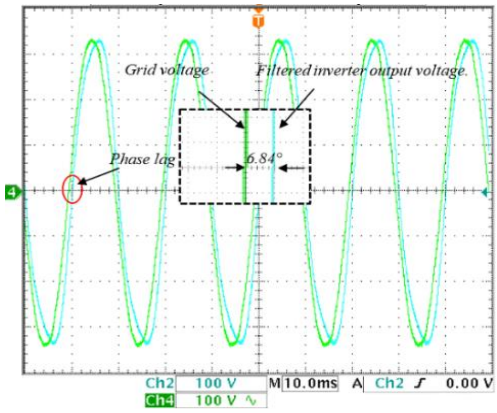

Figure 6. Synchronization of output voltage waveform with 6.84° phase angle delay

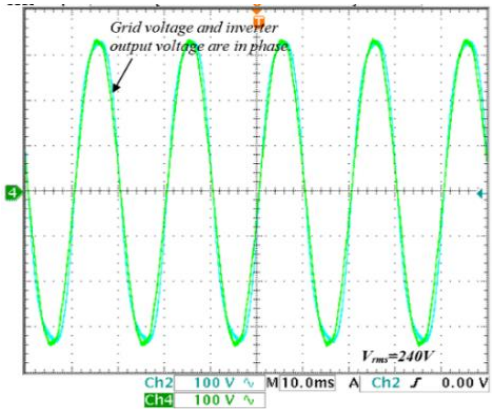

Figure 7. Synchronization of output voltage waveform with compensated 6.84° phase angle delay

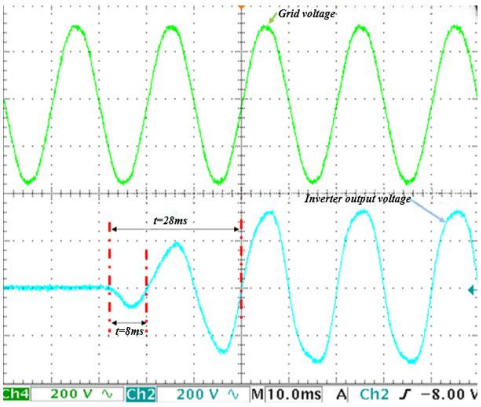

Figure 8. Initiation of grid-tied inverter synchronization with generated voltage

The impact of the inverter output generated by the suggested control method during grid distortion is depicted in Figure 9. As can be seen, the proposed control scheme demonstrated a robust tracking ability to suppress the influence of grid voltage distortion. The generated inverter output took 42 ms to recover to its actual phase value based on the grid voltage waveform. The proposed control algorithm scheme effectively suppressed the influence of grid voltage distortion. The measured THD values of the output voltage and current are 0.16% and 2% respectively. As a result, the THDs of the inverter system's output voltage and current were within the range of power quality standards.

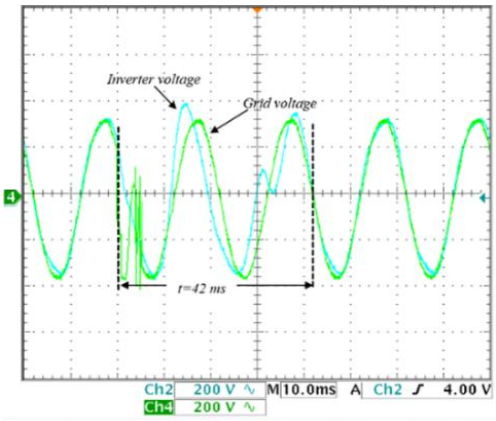

Figure 9. Grid-tied inverter synchronization with the distorted grid voltage

5. CONCLUSION

In conclusion, after the delayed phase angle compensation digitally, the proposed grid-tied inverter successfully synchronized with the frequency, magnitude, and phase angle of the national grid. Moreover, based on testing evaluations, the ZCD component of the PLL for this research functioned with a plus-or-minus tolerance of 0.5% in the frequency variation of the grid-connected inverter's fast synchronization. In terms of frequency and voltage settling time during synchronization initiation, the dynamic performance of fast synchronization was achieved at 8 ms. In addition, the identified settling time for voltage and frequency synchronization after the introduction of grid distortion was 42 ms.

ACKNOWLEDGEMENTS

This research work was supported by Universiti Tun Hussein Onn Malaysia (UTHM) through TIER 1 (Vot Q549) and GPPS (Vot Q325).

REFERENCES

[1] A. Q. Al-Shetwi, "Sustainable development of renewable energy integrated power sector: Trends, environmental impacts, and recent challenges," *Science of The Total Environment*, vol. 822, p. 153645, May 2022, doi: 10.1016/j.scitotenv.2022.153645.

[2] P. Gawhade and A. Ojha, "Recent advances in synchronization techniques for grid-tied PV system: A review," *Energy Reports*, vol. 7, pp. 6581–6599, Nov. 2021, doi: 10.1016/j.egyr.2021.09.006.

[3] D. B. Rathnayake *et al.*, "Grid forming inverter modeling, control, and applications," *IEEE Access*, vol. 9, pp. 114781–114807, 2021, doi: 10.1109/ACCESS.2021.3104617.

[4] T. Sithananthan, A. A. Bakar, B. Sannasy, W. M. Utomo, and T. Taufik, "Fast synchronization with enhanced switching control for grid-tied single-phase square wave inverter using FPGA," *International Journal of Power Electronics and Drive Systems (IJPEDS)*, vol. 15, no. 2, pp. 1105–1116, Jun. 2024, doi: 10.11591/ijpeds.v15.i2.pp1105-1116.

[5] M. J. Mnati, D. V. Bozalakov, and A. Van den Bossche, "A new synchronization technique of a three-phase grid tied inverter for photovoltaic applications," *Mathematical Problems in Engineering*, vol. 2018, no. 1, pp. 1–13, Jul. 2018, doi: 10.1155/2018/7852642.

[6] F. Xiao, L. Dong, L. Li, and X. Liao, "A frequency-fixed SOGI-based PLL for single-phase grid-connected converters," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 1713–1719, Mar. 2017, doi: 10.1109/TPEL.2016.2606623.

[7] B. Liu *et al.*, "A simple approach to reject DC offset for single-phase synchronous reference frame PLL in grid-tied converters," *IEEE Access*, vol. 8, pp. 112297–112308, 2020, doi: 10.1109/ACCESS.2020.3003009.

[8] A. Faro, M. di Benedetto, A. Lidozzi, and L. Solero, "Constant delay-line repetitive control analysis for variable frequency operation," *IEEE Open Journal of Power Electronics*, vol. 3, pp. 481–491, 2022, doi: 10.1109/OJPEL.2022.3190313.

[9] S. Golestan and J. M. Guerrero, "Conventional synchronous reference frame phase-locked loop is an adaptive complex filter," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 3, pp. 1679–1682, Mar. 2015, doi: 10.1109/TIE.2014.2341594.

[10] M. Xie, H. Wen, C. Zhu, and Y. Yang, "DC offset rejection improvement in single-phase SOGI-PLL algorithms: methods review and experimental evaluation," *IEEE Access*, vol. 5, pp. 12810–12819, 2017, doi: 10.1109/ACCESS.2017.2719721.

[11] M. Lakka, E. Koutroulis, and A. Dollas, "Development of an FPGA-based SPWM generator for high switching frequency DC/AC inverters," *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 356–365, Jan. 2014, doi: 10.1109/TPEL.2013.2253216.

[12] T. Binkowski, "Fuzzy logic grid synchronization technique for single-phase systems," in *2018 Progress in Applied Electrical Engineering (PAEE)*, IEEE, Jun. 2018, pp. 1–5. doi: 10.1109/PAEE.2018.8441120.
[13] H. Hassanpour and M. Ehsanian, "Fast grid voltage synchronization using modified frequency-locked loop in single phase grid-connected power systems," *International Journal of Engineering*, vol. 34, no. 6, pp. 1430–1437, Jun. 2021, doi: 10.5829/ije.2021.34.06c.06.
[14] R. Jackson *et al.*, "A comprehensive motivation of multilayer control levels for microgrids: synchronization, voltage and frequency restoration perspective," *Applied Sciences*, vol. 10, no. 23, p. 8355, Nov. 2020, doi: 10.3390/app10238355.
[15] E. H. El-Zohri and M. A. Mosbah, "Comparison and performance analysis of unipolar and bipolar digitally-controlled single-phase inverters," in *2017 Nineteenth International Middle East Power Systems Conference (MEPCON)*, IEEE, Dec. 2017, pp. 1138–1144. doi: 10.1109/MEPCON.2017.8301325.
[16] S. Golestan, J. M. Guerrero, and J. C. Vasquez, "Single-phase PLLs: a review of recent advances," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9013–9030, Dec. 2017, doi: 10.1109/TPEL.2017.2653861.
[17] S. Golestan, J. M. Guerrero, A. Vidal, A. G. Yepes, J. Doval-Gandoy, and F. D. Freijedo, "Small-signal modeling, stability analysis and design optimization of single-phase delay-based PLLs," *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3517–3527, May 2016, doi: 10.1109/TPEL.2015.2462082.
[18] S. R. Sondawale, P. P. Jagtap, and S. G. Tarnekar, "Synchronization of solar inverter with power grid," in *2018 International Conference on Smart Electric Drives and Power System (ICSEDPS)*, IEEE, Jun. 2018, pp. 117–119. doi: 10.1109/ICSEDPS.2018.8536079.
[19] Y. Yang, Z. Xin, K. Zhou, and F. Blaabjerg, "Unified digital periodic signal filters for power converter systems," in *2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017 - ECCE Asia)*, IEEE, Jun. 2017, pp. 286–291. doi: 10.1109/IFEEC.2017.7992052.
[20] X. Chen, Y. Zhang, S. Wang, J. Chen, and C. Gong, "Impedance-phased dynamic control method for grid-connected inverters in a weak grid," *IEEE Transactions on Power Electronics*, vol. 32, no. 1, pp. 274–283, Jan. 2017, doi: 10.1109/TPEL.2016.2533563.
[21] G. A. H. Pawitan, A. Saifullah, A. H. Arofat, and P. D. Sastya, "Transformerless 5kW single phase grid-tied inverter in PT. Len Industri," in *2018 Conference on Power Engineering and Renewable Energy (ICPERE)*, IEEE, Oct. 2018, pp. 1–8. doi: 10.1109/ICPERE.2018.8739694.
[22] A. Kulkarni and V. John, "Design of a fast response time single-phase PLL with DC offset rejection capability," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, IEEE, Mar. 2017, pp. 35–43. doi: 10.1109/APEC.2016.7468172.
[23] S. Shuvo, E. Hossain, and Z. R. Khan, "Fixed point implementation of grid tied inverter in digital signal processing controller," *IEEE Access*, vol. 8, pp. 89215–89227, 2020, doi: 10.1109/ACCESS.2020.2993985.
[24] Y. Cao, Y. Hu, R. Hu, and J. Chen, "Research on the synchronization control strategy for microgrid-connected voltage source inverter," in *2015 IEEE 6th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, IEEE, Jun. 2015, pp. 1–5. doi: 10.1109/PEDG.2015.7223062.
[25] Y. Yang, K. Zhou, and F. Blaabjerg, "Virtual unit delay for digital frequency adaptive T/4 delay phase-locked loop system," in *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, IEEE, May 2016, pp. 2910–2916. doi: 10.1109/IPEMC.2016.7512760.
[26] K. M. S. . Konara, M. L. Kolhe, and W. G. C. A. Sankalpa, "Grid synchronization of DC energy storage using voltage source inverter with ZCD and PLL techniques," in *2015 IEEE 10th International Conference on Industrial and Information Systems (ICIIS)*, IEEE, Dec. 2015, pp. 458–462. doi: 10.1109/ICIINFS.2015.7399055.
[27] A. B. Afarulrazi, M. Zarafi, W. M. Utomo, and A. Zar, "FPGA implementation of Unipolar SPWM for single phase inverter," in *2010 International Conference on Computer Applications and Industrial Electronics*, IEEE, Dec. 2010, pp. 671–676. doi: 10.1109/ICCAIE.2010.5735019.
[28] M. G. M. Abdolrasol, M. A. Hannan, S. M. S. Hussain, and T. S. Ustun, "Optimal PI controller based PSO optimization for PV inverter using SPWM techniques," *Energy Reports*, vol. 8, no. 1, pp. 1003–1011, Apr. 2022, doi: 10.1016/j.egyr.2021.11.180.
[29] S. Burada and K. Padma, "Model predictive current control for maximum power point tracking of voltage source inverter based grid connected photovoltaic system," *International Journal of Power Electronics and Drive Systems (IJPEDS)*, vol. 14, no. 3, pp. 1781–1790, Sep. 2023, doi: 10.11591/ijpeds.v14.i3.pp1781-1790.
[30] M. Kumar *et al.*, "Enhanced PLL-less grid synchronization algorithm amidst unbalanced and distorted three-phase grid conditions," *International Journal of Electrical Power & Energy Systems*, vol. 148, p. 108926, Jun. 2023, doi: 10.1016/j.ijepes.2022.108926.
[31] S. Swain and B. Subudhi, "Grid synchronization of a PV system with power quality disturbances using unscented Kalman filtering," *IEEE Transactions on Sustainable Energy*, vol. 10, no. 3, pp. 1240–1247, Jul. 2019, doi: 10.1109/TSTE.2018.2864822.
[32] J. Yu, B. Yang, P. Zhu, L. Zhang, Y. Peng, and X. Zhou, "An improved digital phase locked loop against adverse grid conditions," *Energy Reports*, vol. 8, no. 4, pp. 714–723, Jul. 2022, doi: 10.1016/j.egyr.2022.01.240.
[33] A. A. Bakar, W. M. Utomo, S. A. Zulkifli, E. Sulaiman, M. Z. Ahmad, and M. Jenal, "DC-DC interleaved boost converter using FPGA," in *2013 IEEE Conference on Clean Energy and Technology (CEAT)*, IEEE, Nov. 2013, pp. 98–101. doi: 10.1109/CEAT.2013.6775607.

BIOGRAPHIES OF AUTHORS

Afarulrazi Abu Bakar was born in Johor, Malaysia, in May 1980. He received his B.Eng. degree in Electrical Engineering from Universiti Teknologi Mara (UiTM), Malaysia, in 2004 and M. Eng. and Ph.D. degrees from Universiti Tun Hussein Onn Malaysia (UTHM) in 2019 and 2007, respectively. He has been working as senior lecturer at the Department of Electrical Power Engineering, Faculty of Electrical and Electronic Engineering, UTHM, since 2007. His current research interests include renewable energy, grid-connected system, DC/DC converters, multiple-input converters, multiphase converters, resonant converters, and advanced controller design. He can be contacted at email: afarul@uthm.edu.my.

Balarajan Sannasy was born in Kedah, Malaysia, in September 1997. He received his B.Eng. degree in Electrical Engineering from Universiti Tun Hussein Onn Malaysia (UTHM), Malaysia, in 2023. He is currently employed as Site Project Engineer at Leapco Sdn. Bhd. His current research interests include power electronics and energy conversion. He can be contacted at email: rajen0174693838@gmail.com.

Hazwaj Mhd Poad is a member of the IEEE and the IEEE Signal Processing Society. He has been working as a senior lecturer at the Department of Electronic Engineering, Faculty of Electrical and Electronic Engineering, UTHM, since 2004. He graduated from Oita University Japan, B.Eng., and M.Eng. in 2002 and 2004, respectively. His research interest is in embedded systems. He can be contacted at email: hazwaj@uthm.edu.my.

Tharnisha Sithananthan was born in Perak, Malaysia, in May 1997. She received her B.Eng. degree in Electrical Engineering from Universiti Tun Hussein Onn Malaysia (UTHM), Malaysia, in 2023. She is currently pursuing a M.Eng. at UTHM since 2023. Her current research interests include power electronics and renewable energy. She can be contacted at email: tharnisha97@gmail.com.

Wahyu Mulyo Utomo was born in Pati, Indonesia, in 1969. He received his B.S. degree in Electrical Engineering from Universitas Brawijaya, Malang, in 1993, M.S. degree in Electrical Engineering from the Institute Sepuluh Nopember, Surabaya, in 2000 and Dr. Eng. degree from Universiti Teknologi Malaysia in 2007. He is currently an associate professor at the Electrical Power Engineering Department, Faculty of Electrical and Electronic Engineering, Universiti Tun Hussein Onn Malaysia. His current research interests include the area of power electronics and motor drives control. He can be contacted at email: wahyu@uthm.edu.my.

Nor Farisha Diana Rosli was born in Labuan, Malaysia, in February 1998. She received a degree in Electrical Engineering in 2022 from Universiti Tun Hussein Onn Malaysia, Johor, Malaysia. Currently, she is a master of Electrical Engineering student at Universiti Tun Hussein Onn Malaysia, Johor, Malaysia. Her areas of interest are power electronics, high-voltage technology, and industrial applications. She can be contacted at email: he220026@student.uthm.edu.my or farishadiana98@gmail.com.