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Switching state vector selection for improved THD performance in multilevel current fed inverters

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ABSTRACT

This paper aims to explore synthesis methods of three-phase multi- level current waveforms by utilizing a configuration of n parallel operating three-phase, three-level current-fed inverters (CFIs). It points out an issue where differences in the DC-link current between inverters cause a distorted space vector diagram and decreased switching state redundancy, this leads to generation of low frequency harmonics in the output current and increased total harmonic distortion (THD). The research suggests a method that chooses the best switching state vectors by considering their closeness to a reference current space vector. This approach aims to decrease switching losses and low-frequency harmonic content. This method improves the quality of the waveform and the efficiency of the inverter by closely matching the switching operations with the intended current path. An analytical model is created to investigate how changes in DC-link current impact inverter performance. Simulations and actual tests confirm the ef-ficacy of the proposed strategy in enhancing total harmonic distortion (THD) and waveform accuracy. The results provide valuable information on improving multilevel inverter designs to enhance power quality and operational efficiency, indicating potential areas for further research in power electronics.

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1. INTRODUCTION

In the field of power electronics, there is considerable interest in the design and optimization of current-fed inverters (CFIs) for efficient energy conversion, especially in applications related to renewable energy sources. This study aims to investigate advanced techniques in order to enhance the efficiency of three-level converters for interface circuits by removing the requirement for current sharing inductors and transformers. To achieve this goal, each CFI unit is equipped with a separate direct current source, enabling parallel connection on the alternating current side. The magnitudes of the DC currents [1]–[4] from the separate sources are consistent.

Yet, a significant difficulty arises in ensuring consistent DC-link currents among CFI units, particularly when they are powered by intrinsically fluctuating renewable energy sources like photovoltaics or fuel cells. The study shows that differences in DC-link currents cause distortions in space vector diagram and result in a loss of switching state redundancy. This phenomenon negatively impacts the output current by introducing low-frequency harmonic [5] components, which leads to a degradation in the system's total harmonic distortion (THD) and compromises power quality.

To address this issue, the paper proposes a new method that focuses on the strategic selection and time-sharing of switching state vectors via space vector modulation techniques [6]–[11]. This technique generates a reference current space vector by utilizing the closest switching state vectors [12]–[18] in order to optimize switching operations and reduce losses. Although it reduces switching losses and harmonic distortion, this technique unintentionally causes low-frequency pulsations in the DC-link voltage of each inverter, with the voltage variation precisely proportional to the imbalance in DC-link current. The study investigates the difficulties of developing a DC-DC converter that can adjust to a large range of output voltage fluctuations [19]–[28],this has an impact on the DC-link voltage's stability.

Line voltage coordinate transformation is used in a new space vector pulse density modulation technique that is presented [6]. For pulse density modulation, it employs three first-order sigma delta modulators (SDM), which simplifies computation by quantifying the reference vector and producing output switching vectors without sector identification. The proposed space vector quantizer (SVQ) constructs Voronoi areas with inverter switching vectors, using a normalized reference vector to designate regions and quantifying SDM's instantaneous error vector (IEV). This method avoids the difficult computations related with sector identification, sub-hexagonal mapping, and lookup table usage, making time calculations easier. Furthermore, in [29], When analyzing switching loss and total harmonic distortion (THD) in diode-clamped three phase multilevel inverters across various resistive loads, space vector pulse width modulation (SVPWM) is utilized to improve.

The multilevel DC-link inverter (MLDCLI) [13] acts as a vital link between solar systems and household AC power supplies. This paper describes an MLDCLI arrangement that uses three asymmetric DC sources to provide a 15-level output voltage. Control is implemented using the simplified gate pulse generation (SGPG) approach. In addition, a modified nearest level modulation (mNLM) method is used to reduce total harmonic distortion (THD) in response to variations in the DC voltage source ratio. The mNLM algorithm adjusts gradient angles dynamically to optimize THD as the voltage in one of the DC sources varies. Continuous use of this technique based on input voltage values improves THD performance in the output voltage, especially when the DC voltage sources vary.

Shang and Li [1] proposed a new approach, a decreased common mode voltage (CMV) space vector modulation (SVM), that is specifically developed for current source converters. Unlike typical nonzero-state reduced common mode voltage (RCMV) SVMs, this strategy provides significant CMV reduction without ignoring zero-state vectors, resulting in greater performance above standard algorithms. This RCMV SVM approach also applies to the converter side interface (CSI), where zero-state vector selection is guided by motor stator voltages rather than grid voltages as in the converter side rectifier (CSR) application. When compared to existing approaches, the proposed method considerably reduces CMV peak value. Furthermore, when compared to the standard three-segment SVM, the suggested RCMV SVM shows lower CMV and improved harmonic performance.

Using a space vector modulation (SVM) approach on a five-level current source inverter based on interphase transformers was recommended by Dupczak *et al.* [4]. A new SVM technique has been presented that lowers the requirements for the used passive components, such as the coupled magnetic components, while enabling the interphase transformer-based five-level CSI to provide high-quality output voltages. As a result, the volume of the passive components might be decreased, resulting in higher power density levels and improved inverter performance. A quick comparison with a traditional 3L-CSI demonstrates that the 5L-CSI using the suggested SVM can reduce the requirements for passive components.

Distortion of the space vector diagram complicates precisely recognizing the sector of the reference space vector in the 5-level CFI system, which is crucial for optimal performance and efficiency, concludes with a thorough assessment of the 5-level CFI's performance, using MATLAB simulations to confirm the efficacy of the suggested solutions in reducing THD and improving system efficiency and reliability. This study makes a substantial contribution to the power electronics profession by offering essential insights and approaches for optimizing CFI designs to enhance power quality and efficiency in renewable energy applications. The primary objectives of this study are:

- Develop a configuration for three-level current-fed inverters (CFIs) that removes the necessity for cur- rent sharing inductors and transformers by employing separate DC current sources for each CFI unit, enabling parallel connections on the ac side.
- To address the issue of uneven DC-link currents in CFI units, particularly when coming from variable renewable energy sources such as photovoltaics or fuel cells, which may cause distortion in the multilevel space vector diagram and a loss of switching state redundancy.

– By addressing the introduction of low-frequency harmonic components produced by the DC-link current inequality, reduce total harmonic distortion (THD).
– Develop and confirm an advanced switching strategy that includes choosing and time-sharing switching state vectors using space vector modulation techniques. By generating a reference current space vector from the closest switching state vectors, this aims to lower switching losses and improve waveform quality.
– Design a versatile DC-DC converter that can adjust to wide variations in output voltage to maintain stability of the DC-link voltage, allowing inverters to run at consistent switching rates even with fluctuations in DC-link current.
– Evaluate a 5-level CFI system's performance using sophisticated simulation tools like MATLAB to confirm that suggested solutions are successful in lowering THD, minimizing switching losses, and enhancing overall system reliability and efficiency in renewable energy applications.

2. PROPOSED METHODOLOGY

The direct current balance optimization between two current source inverters (CSIs) using space vector modulation is closely examined in this research methodology. This method entails a thorough examination of the present space-vectors within the dual-CSI system that correlate to various switching states. In Figure 1 the four numbers that indicate these switching states are named using a method where the first two digits stand for the on-state switches in inverter-1, and the final two digits stand for those in inverter-2.

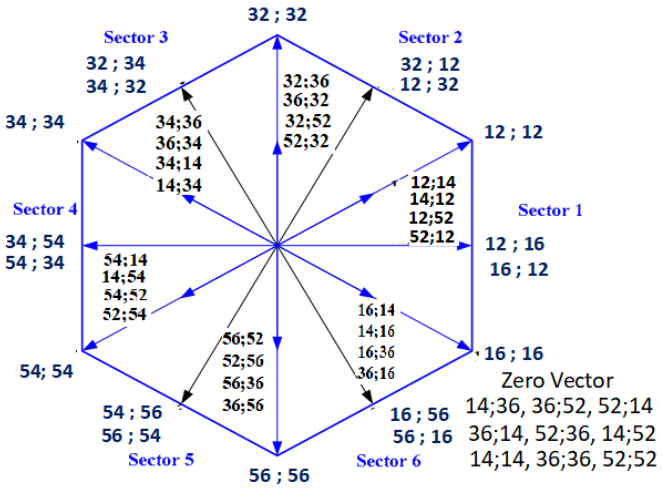

Figure 1. Switching states of five-level SVPWM

The process comprises dividing the vectors into four categories, as shown in Figure 2 - large, medium, small, and zero vectors. This classification is the foundation for the development of a novel switching scheme intended to enhance the two inverters' DC current balance. Through the reduction of energy losses and enhancement of system efficiency, this technique offers enhanced operational performance.

The new switching pattern is based on specific design ideas that are expressed through important directives.

– Prohibition of small and zero current vectors: The approach clearly does not allow the use of small and zero current vectors. This exclusion is based on the vectors causing a 'shoot-through' circumstance, where two devices in the same leg are activated simultaneously. This scenario increases the switching frequency and causes substantial energy losses, which ultimately reduces system efficiency.
– Exclusion of large vectors: Large vectors are not suited for DC current balancing management. This is due to the operating characteristic of activating the identical devices in both inverters, which does not modify the DC current in the inverters and so does not achieve current balancing.
– Using medium vectors for DC current balance control: The core of the suggested approach relies on the

strategic use of medium vectors. The vectors' inherent redundancy in switching states makes them ideal for enabling direct current balance control. Separate control of the DC currents in the two inverters is made possible by utilizing the redundant switching states connected to the medium vectors, which permits the proper distribution of DC current balance.

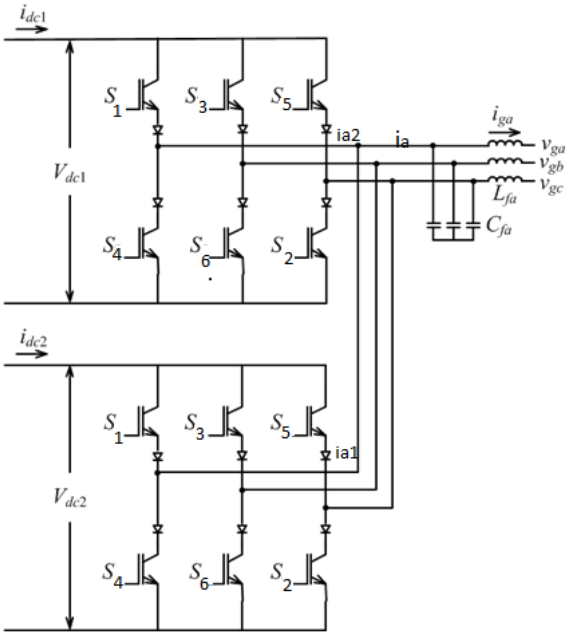

Figure 2. Five-level SVPWM

2.1. Equal DC-link currents in a five-level current-fed inverter

The creation of switching states and their use in building a five-level space vector diagram necessitates a thorough understanding of power electronics and space vector modulation (SVM) techniques. Specifically, the switching states (S_1, S_1'), (S_2, S_2'), and (S_3, S_3') are designated as i_{0a}, i_{0b}, and i_{0c}. These notations represent the zero-switching state vector, indicated as i_0, which serves as the foundation for the five-level space vector diagram shown in Figure 2. This diagram is the result of the combination and expansion of three-level space vector diagrams, demonstrating a sophisticated modulation strategy designed specifically for current fed inverters (CFIs).

The five-level space vector diagram is organized into six main sectors, S_I through S_{VI}, each of which has four minor sectors, S_1 - S_4. This segmentation enables a detailed control strategy, which allows for exact adjustment and enhancement of the inverter's performance. This segmentation permits a sophisticated control strategy, allowing for precise adjustment and improvement of the inverter's performance. This system contains 49 repeating switching state vectors, yielding 19 distinct state vector places. Table 1 organizes the locations and their corresponding switching state vectors.

The modulation system uses redundancy in switching states to give flexibility and robustness when operating the inverter. A specific switching state sequence can be produced by repeatedly varying the switching states in three-level CFI units. Table 1 lists the combinations that could be used to accomplish the intended switching states.

Change the state vector positions I_6, I_1, and I_0 in minor sector S_1 of major sector S_I. To reach state vector position I_6, use one of the redundant switching state vectors I_{6-1}, I_{6-2}, I_{6-3}. The switching state vector I_{6-1} can be obtained using any of the combinations (i_6, i_{0a}), (i_6, i_{0b}), or (i_6, i_{0c}). This demonstrates the systematic use of redundancy to achieve accurate control over the inverter's output. A reference space vector crucial for the modulation method can be created by utilising any of the surplus switching states in a specific sector. Space vector modulation demonstrates versatility and efficiency in optimizing the operational dynamics of CFIs, leading to higher power quality, reduced harmonic distortion, and improved system performance.

Table 1. Classification of current space vectors

Type	Vectors
Zero vectors	52;14, 36;14, 14;36, 36;52, 52;36, 14;52, 14;14, 36;36, 52;52, 12;54, 54;12, 32;56, 56;32, 34;16, 16;34
Small vectors	56;36, 36;56, 56;52, 52;56, 54;16, 16;54, 16;14, 14;16, 16;36, 36;16, 56;12, 12;56, 32;36, 36;32, 32;52, 52;32, 12;34, 34;12, 54;14, 14;54, 54;52, 52;54, 34;56, 56;34
Medium vectors	12;16, 16;12, 32;12, 12;32, 32;34, 34;32, 34;54, 54;34, 54;56, 56;54, 16;56, 56;16
Large vectors	54;54,56;56, 16;16, 12;12, 32;32, 34;34

2.2. Calculation of duty cycles by projections

Multi-level current fed inverters (MCFI) that use space vector modulation (SVM) create a desired reference current vector, $\dot{i}^*$, by carefully sampling the static current vectors of the inverters during a designated switching interval. The procedure relies on the inverter maintaining a specific switching state for a sufficient duration to produce the desired vector, which signifies a particular direction and amount of current that the inverter has t o provide. This modulation strategy is primarily concerned with computing duty cycles for each of the MCFI's current vectors. Duty cycles are critical in determining how long each vector is active during a switching period, which impacts the overall shape and qualities of the output waveform. The current reference angle (θ) and modulation index (Mi) related to related to $\dot{i}^*$ are crucial factors in this computation. The modulation index measures the ratio of the reference vector's magnitude to the maximum achievable vector magnitude based on the inverter's setup. The reference angle θ indicates the direction of $\dot{i}^*$ in the $\alpha - \beta$ plane, guiding the modulation process.

The methodology provided in literature [25] describes how to compute duty cycles for neutral-point clamped Multi-Level Voltage Source Inverters (MVSI). This method focuses on strategically determining specific projections of the reference vector onto the $\alpha - \beta$ plane. These projections are essential for simplifying the SVM process by decomposing the intricate vector manipulation into simpler geometric and algebraic operations.

Figure 3 demonstrates a situation in which three vectors, $\overrightarrow{i_a}$, $\overrightarrow{i_b}$, and $\overrightarrow{i_c}$, form a triangle area in the $\alpha - \beta$ plane. The goal is to place the reference vector $\dot{i}^*$ (see (1) and (2)) inside the triangle using its vertices as the basic vectors for modulation. The method provides insight into achieving the reference vector's projection onto the plane by analysing the contained region defined by the vertices and combining fundamental vectors. The triangle's sides and the area it encompasses with the reference vector serve as a geometric foundation for determining the duty cycles of the vectors, allowing for the accurate generation of $\dot{i}^*$ by combining the inverter's switching operations.

$$i^* = \overrightarrow{i_c} + \overrightarrow{p_a} + \overrightarrow{p_b} \tag{1}$$

$$i^* = |\overrightarrow{p_a}| l_a \overrightarrow{i_a} + |\overrightarrow{p_b}| l_b \overrightarrow{i_b} + (1 - |\overrightarrow{p_a}| l_a - |\overrightarrow{p_b}| l_b) \overrightarrow{i_c} \tag{2}$$

The modules of $\overrightarrow{p_a}$ and $\overrightarrow{p_b}$ are the projections of i^* on the triangle sides and l_a , l_b are the distances between the adjacent vectors. The duty cycles for generic vectors are given in (3).

$$\begin{aligned} d'_a &= |\overrightarrow{p_a}| l_a d'_b \\ &= |\overrightarrow{p_b}| l_b d'_c \\ &= (1 - d'_a - d'_b) \end{aligned} \tag{3}$$

The normalized reference vector i^* is rotated to the first sextant. Now the angle of i^* is now represented by θ', which is defined as given in (4).

$$\theta' = \theta - (N_s - 1)\frac{\pi}{3} \tag{4}$$

Where, $N_s \in 1, 2...6$, using the edges that define the sextant in Figure 3, two axes where the projections of the reference vector lie are defined with angles equal to $\pm\frac{\pi}{6}$. The values of the projections are determined using (5) and (6).

$$|\overrightarrow{p_a}| = M_i[\sqrt{3}\cos(\theta') - \sin(\theta')] \tag{5}$$

$$|\overrightarrow{p_b}| = M_i[\sqrt{3}\cos(\theta') + \sin(\theta')] \tag{6}$$

Where, the modulation index ranges from 0 to 1 for the MCSI linear modulation range. Each sextant of the vector plane can be divided into four smaller regions; nevertheless, each side of the triangles has a length $l_T = \frac{1}{\sqrt{3}}$. This represents the normalized distance between two adjacent vectors. Using this distance, as well as (5) and (6) in (3), the five-level CSI generic duty cycles are (7) and (8).

$$d'_a = M_i[\cos(\theta') - \sqrt{3}\sin(\theta')] \tag{7}$$

$$d'_b = M_i[\cos(\theta') + \sqrt{3}\sin(\theta')] \tag{8}$$

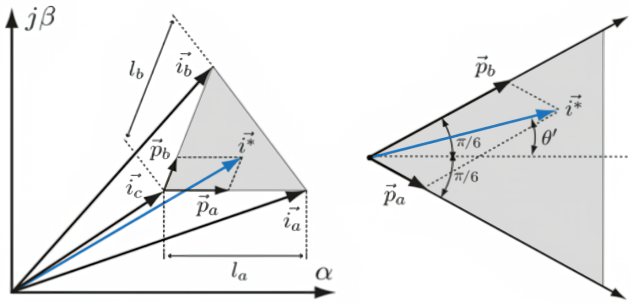

Figure 3. Projections and composition of the reference vector from three arbitrary and projections of current reference vector in the $\pm\frac{\pi}{6}$ axis at first sector

3. RESULTS AND DISCUSSION

3.1. Configuration and simulation of the converter

The inverter is designed to transform direct current (DC) into a five-level alternating current (AC) output, allowing for the generation of five unique voltage levels in the output waveform. Having fine granularity in output levels enables a more accurate representation of a sinusoidal waveform, which decreases harmonic distortion and enhances power quality. Each phase of the inverter typically consists of two converters connected either in series or parallel, depending on the design. It is essential to have this setup in order to achieve the five-level output, as each converter plays a role in increasing the voltage levels by sequential switching.

IGBTs are selected for their high efficiency and rapid switching abilities, which are crucial for handling high currents (100 A) and the precise control needed in multi-level inverters. Their durability in managing high power levels and their ability to be controlled make them perfect for this specific use. Each converter consists of six IGBT switches organised to enable the production of a five-level output. The positioning of these switches is crucial for the inverter to control the DC current and produce the intended AC waveform. The switches are probably arranged in either a full-bridge or half-bridge setup, where each leg of the bridge plays a role in determining the final output voltage levels.

The inverter's control approach probably use PWM methods to control the IGBT switches' opening and closing. This technique enables accurate voltage level adjustments by regulating the duration (width) of the pulses directed to each switch. Space vector modulation (SVM) can be used to optimise the switching pattern for a five-level inverter. This sophisticated modulation method determines the most efficient switching states needed to provide the voltage vector closest to the desired reference, reducing switching losses and harmonics. The Simulink model shown in Figure 4 demonstrates the implementation of control methods by integrating IGBT models, control logic for PWM or SVM, and the system's setup. The diagram visually represents how the inverter operates by showing the current flow through the switches and the modulation mechanism. The simulation aims to confirm the inverter's capacity to generate a five-level AC output from a 100 A DC current source. This includes analysing the waveform quality, quantifying harmonic distortion, and examining the efficiency of the inverter. Switching strategy optimisation involves using simulation to attain peak performance in efficiency, reduced harmonic distortion, and stability across different load circumstances. The parameters used for simulation is give in Table 2.

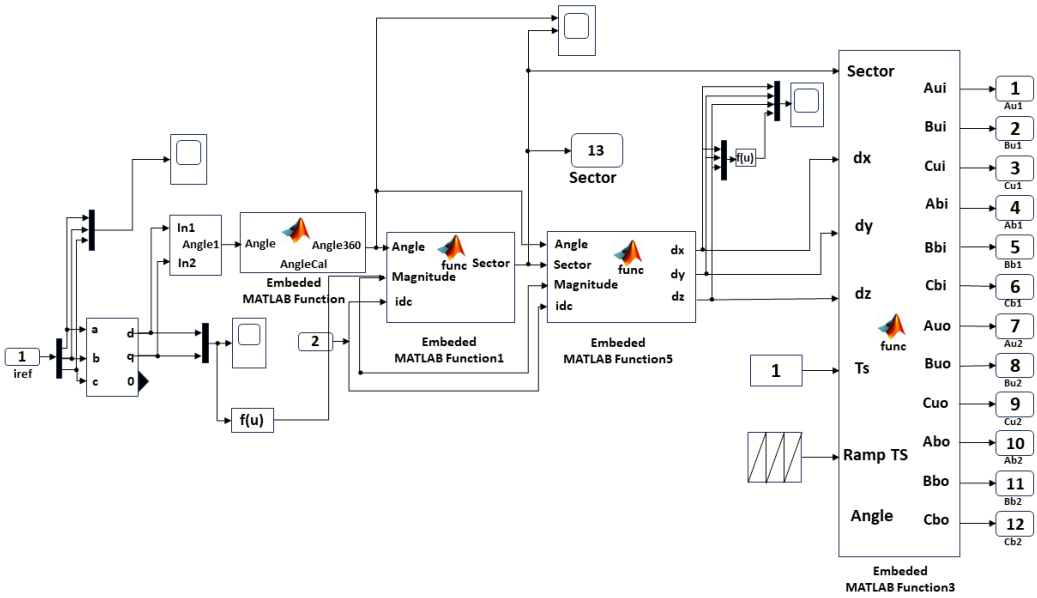

Figure 4. MATLAB simulink model diagram

Table 2. Classification of current space vectors

Parameter	Value
Simulink time setup	1e-6
Inductor filter Lf	1.1258 mH
Capacitor filter Cf	10e-6
Power	111 KW
Sampling frequency(fs)	5 KHZ
Max phase voltage	340 V
Modulation index	0.866

The DC-link voltage in a power conversion system shows harmonic distortion with a ripple at a frequency of 300 Hz, serving as a connection between the input power source and the inverter. Ripple is an oscillation that is not desired and is added on top of the DC voltage. It can cause inefficiencies, higher heat production, and may interfere with the functioning of the load or the power conversion system. To remove the 300 Hz harmonic component, the proposed solution is to install an LC-filter on the DC side of the link. An LC-filter is comprised of an inductor (L) and a capacitor (C) linked either in series or parallel, with the purpose of functioning as a low-pass filter. This filter efficiently reduces high-frequency elements, permitting just the intended DC component and low-frequency changes to go through.

The inductor slows down quick changes in current, while the capacitor creates a channel with low impedance for the ripple frequency, which helps stabilise the DC-link voltage by reducing oscillations. The mean value of the DC-link voltage (VDC) is around 555 V as shown in Figure 5. This value is important because it establishes a reference point for the operating voltage level in the system, which can be used to evaluate the performance of the LC-filter in reducing ripple. The consistent average voltage value observed at various points in the DC-link suggests that the ripple frequency harmonic component has minimal impact on the average voltage. The LC-filter effectively stabilises the voltage throughout the system. The graphs in Figure 6 showns the output phase-a current of inverters 1 and 2. The top waveform have more consistent pulse widths across the cycle, whereas the bottom waveform shows slightly more variation in the width of some pulses. This variation can affect the harmonic content and the quality of the output waveform. Both waveforms oscillate between similar amplitude levels, suggesting that the current magnitudes are approximately the same.

The FFT window and THD analysis of output phase current of converter-1 are represented in Figures 7 and 8 respectively. Due to the square nature of the waveform (Figure 7), it is expected to contain a series of odd harmonics in its frequency spectrum. This means that the FFT analysis will show significant fre-

quency components at odd multiples of the fundamental frequency. An LC filter on the DC side, as mentioned earlier, could smooth out the ripple to protect sensitive loads and reduce electromagnetic interference (EMI). A high peak-to-RMS current ratio indicate a waveform with significant harmonic content, as suggested by the FFT analysis. Figure 9 shows the Five-level output currents of combined control of inverters at fundamental frequency (50 Hz). Five level output phase currents are $I_{a_0} = I_{b_0} = I_{c_0} = 210.9A$. The FFT window and THD analysis of output phase current of converter-2 are represented in Figures 10 and 11 respectively. The phase voltages and phase currents are at the grid and grid phase voltage set to 240 V rms.

The THD analysis of converter-2's output phase current in Figure 12 shows a significant harmonic distortion with a THD of 12.39%, primarily concentrated below 1000 Hz. The fundamental frequency is 50 Hz with notable harmonic peaks reaching up to 16% of the fundamental's magnitude.

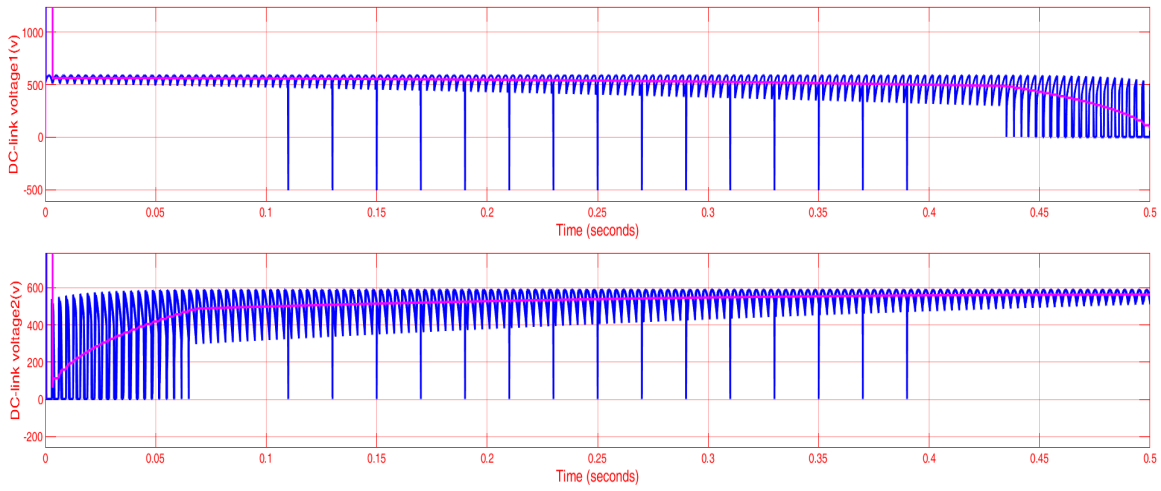

Figure 5. Input DC link voltage

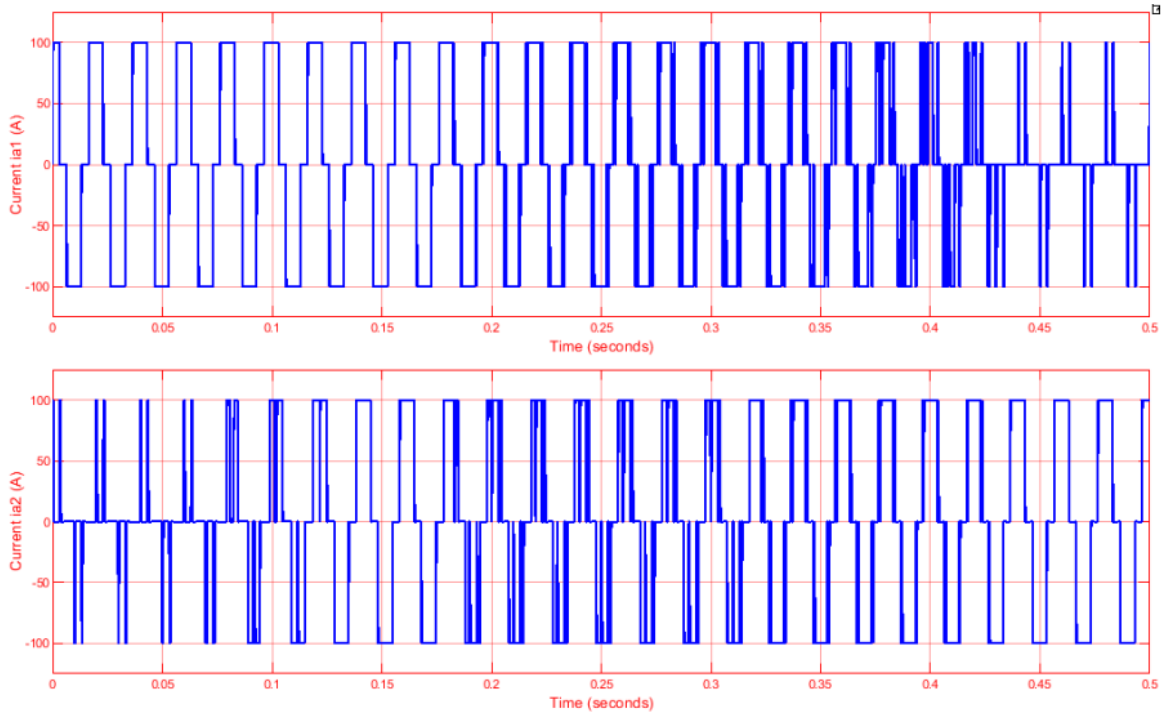

Figure 6. Output phase-a current of inverters 1 and 2

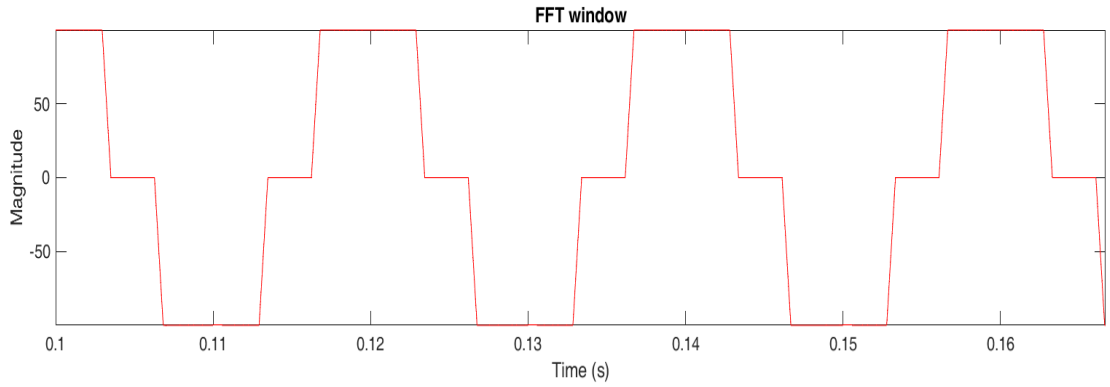

Figure 7. The FFT of output phase current of converter-1

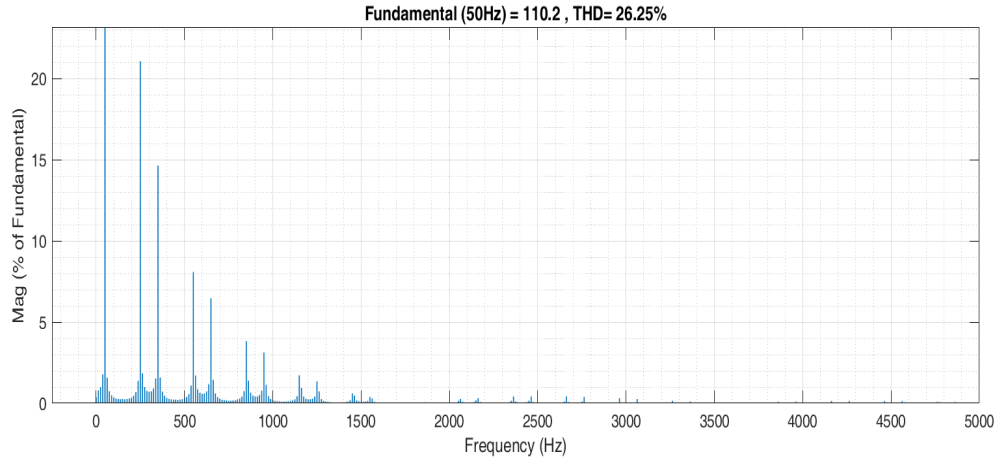

Figure 8. The THD analysis of output phase current of converter-1

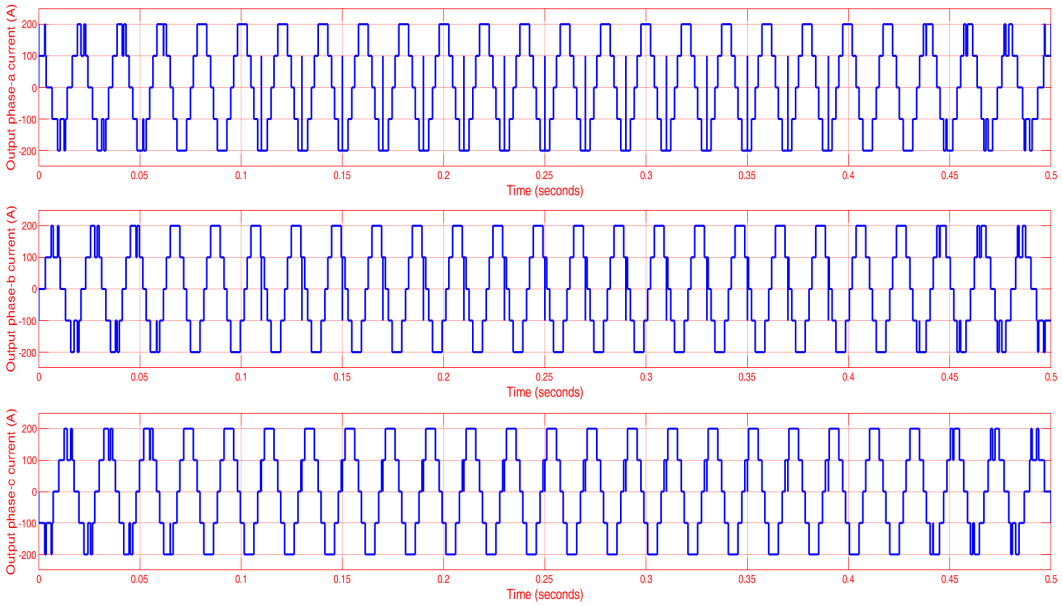

Figure 9. Five level output current vs time

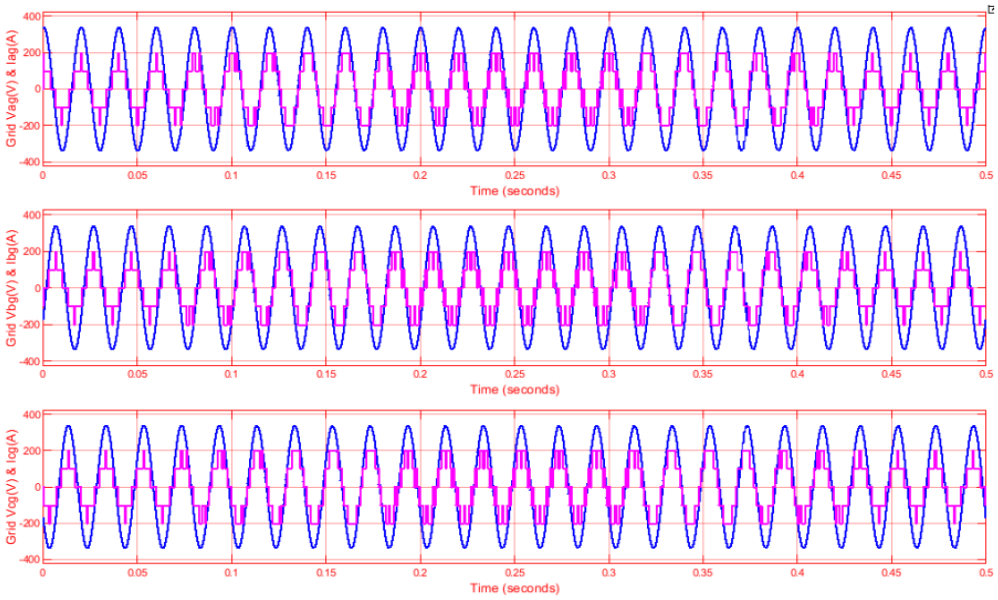

Figure 10. Grid voltage (V_{ag}) and current (I_{ag}) vs time

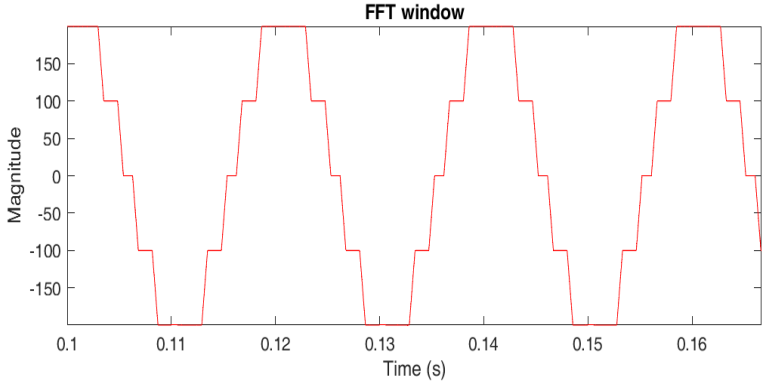

Figure 11. The FFT of output phase current of converter-2

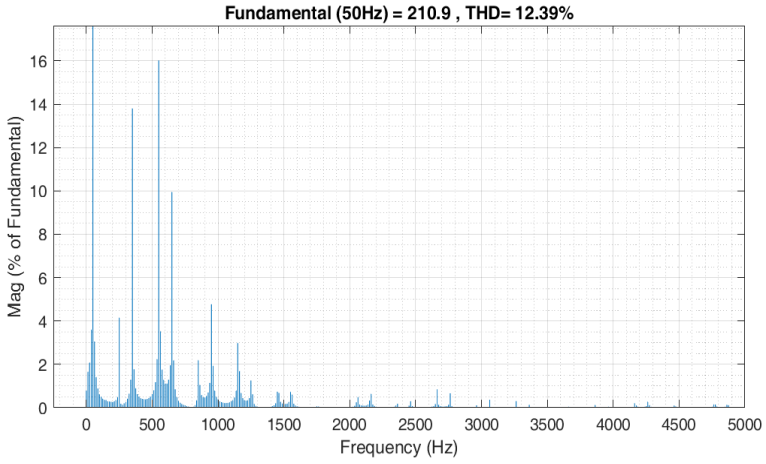

Figure 12. The THD analysis of output phase current of converter-2

4. CONCLUSION

The system considered comprises two three-phase, three-level current-fed inverters (CFIs). These inverters are connected in parallel on the alternating current (AC) side. This parallel configuration enables the combination of output currents from each inverter, facilitating an increase in the number of available output levels. Each CFI is powered by an independent current source on the direct current (DC) side. The parallel connection of the CFIs allows for the generation of five-level current waveforms. These additional levels are achieved by coordinating the switching actions of the two inverters to superimpose their individual three-level outputs, effectively creating a more refined five-level waveform. The multilevel current waveforms reduce the total harmonic distortion (THD) in the output current, improve power quality, and facilitate operation at higher voltages with lower electromagnetic interference (EMI). The control strategy for the five-level CFI employs space vector modulation, which is a sophisticated technique used to control the output voltage and current of inverters by determining the optimal switching state for each time interval. The SVM technique is specifically developed to manage equal DC-link currents from each inverter. Ensuring equal DC-link currents is crucial to maintaining the balance of power among the phases and achieving the desired multilevel waveform without distortions. In future work adaptive control algorithms that dynamically adjust SVM parameters in real-time to optimize for varying load conditions and power supply fluctuations can be developed. Machine learning algorithms can be incorporated to predict system behavior and automating the selection of switching states could enhance efficiency and reliability.

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