

# LCL filter based high power density AC/DC converter for fast charging applications

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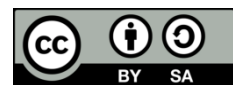
Power factor correction

Total harmonic distortion

## ABSTRACT

This paper introduces a LCL filter design tailored for a 40 kW three-phase grid-connected converter utilized in electric vehicle onboard fast chargers. In contrast to conventional filters, the LCL filter finds extensive application in AC/DC converters for power factor correction, thanks to its enhanced harmonic reduction and improved stability of the system. The parameters of LCL filter are devised based on considerations such as the system's power, the frequency of the alternating current (AC) input, and the PWM frequency, determined through simulation and comprehensive theoretical analysis. By implementing a dual-current closed-loop control strategy, the system ensures a robust response for both the current on the AC side of the converter and the voltage on the direct current (DC) side. The analysis of the system's performance includes rapid dynamic response, system efficiency, AC current harmonic, and DC ripple voltage. Both simulation and experimental results are presented to validate the proposed design for the LCL filter.

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## 1. INTRODUCTION

In recent years, there have been significant developments in the electric vehicle (EV), with major automakers like Nissan, Tesla, and Chevrolet introducing groundbreaking models such as the Nissan Leaf, Tesla Model 3, and Chevrolet Bolt EV. These vehicles not only meet high-performance standards and offer convenience but also prioritize sleek design and an enhanced driving experience. Tesla, renowned for its advanced technology and impressive range per charge, has been particularly influential in shaping the EV landscape. Figure 1 illustrates substantial investments by major car manufacturers in the development of electric vehicles. Established automakers like BMW, Nissan, Hyundai, Toyota, and Ford have adapted their production lines to introduce hybrid and electric vehicles with modern features, catering to the evolving preferences of consumers.

In line with these developments, the charging infrastructure has evolved significantly. As of 2020, most charging stations could achieve power outputs ranging from 6 kW to 10 kW, with select models reaching up to 22 kW, exemplified by the Renault Zoe. The power density reached approximately 3.3 kW/L, with the highest efficiency estimated to surpass 97%. Looking ahead to 2025, the United States has set ambitious targets, aiming for power output and specific power density of 4 kW/kg and 4.6 kW/L, respectively, accompanied by the highest efficiency reaching 98% [1]. This trajectory underscores the dynamic and competitive nature of the

electric vehicle industry, providing consumers with diverse choices and propelling technological advancements to minimize the environmental impact of transportation.

On-board chargers as shown in Figure 2, are becoming increasingly important in a world transitioning towards renewable energy sources and electric vehicles. However, a significant hurdle in their widespread adoption is their size and weight, often attributed to the bulky cores used in transformers and L-filters [2], [3]. These cores are essential components, but they contribute significantly to the overall footprint of the charger. This study tackles this challenge by investigating the potential of replacing conventional L-filters with LCL filters.

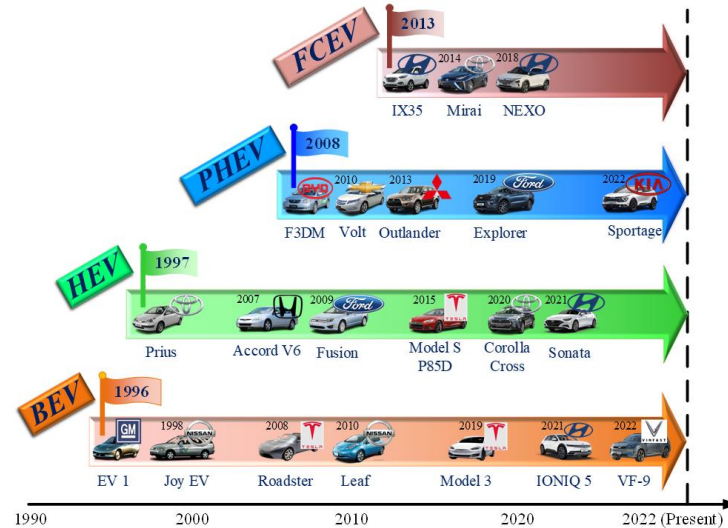


Figure 1. Milestone of EV from 1990 to present

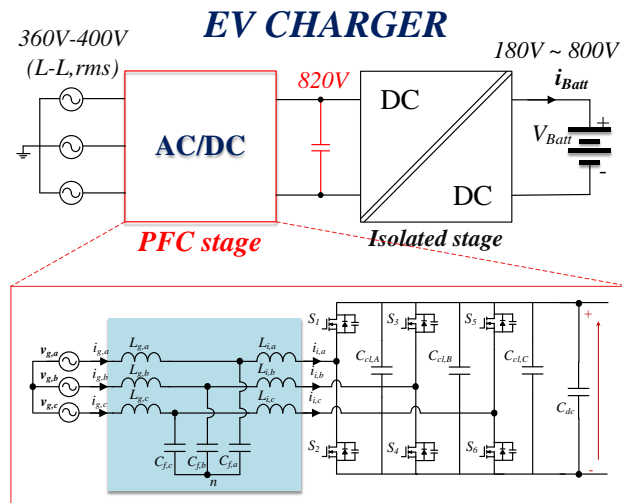


Figure 2. Three-phase two-level active rectifier using LCL filter

LCL filters offer the potential for significant size and weight reduction compared to L and LC filters, while still maintaining adequate filtering performance. Additionally, the LCL filters can compensate for reactive power and improve the system's power factor. So, the power factor correction is improved in case of LCL filter as compared to the L or LC filter. By focusing on this specific area, this study contributes to the development of more compact, more efficient, and sustainable future [2]. However, careful design is necessary to achieve consistent power factors and avoid resonance issues. Previous literature [4]–[17] has proposed LCL designs, but none of them provide an easy way to design optimal values for LCL parameters. In [4]–[9], passive damping methods were suggested for the LCL filter to reduce the resonance peak, but this method increases

the cost and reduces efficiency. Active damping methods were proposed in [10]–[14], but these methods require additional feedback signals, introducing sensors that increase system complexity. To overcome this, a sensorless damping method was proposed in [14]–[17], but it increases processing time and does not provide high efficiency. Liserre *et al.* [18] highlighted that the LCL filter can operate effectively even without damping methods. Some LCL filter design methods have been presented in recent years [19]–[27], taking into account other factors and using software support for inputs. In particular, Wang *et al.* [23] use intelligent control algorithms to determine filter parameters.

This paper proposes a simple LCL filter design procedure, focusing on achieving the desired power factor (PF) and total harmonic distortion (THD) while optimizing filter size and losses. By neglecting passive damping [18], this method allows for a smaller and lighter LCL filter compared to L filters in the power factor correction (PFC) stage. LCL filters offer inherent advantages: their third-order nature provides superior harmonic attenuation, enabling smaller inductors and capacitors for the same level of filtering. The proposed method will reduce the overall filter size and weight. The effectiveness of the LCL filter in the PFC stage will be validated through simulations and experiments.

## 2. MATHEMATICAL MODELLING OF CONVERTER

This section presents the converter's mathematical modeling. This model is used to make the process of character analysis and control system design [24]. To simplify the analysis and calculations, this paper assumes that the LCL filter at low frequencies responds as a conventional L filter. This assumption will also be examined in the implemented results. In Figure 2, the average model in the three-phase coordinate system is established as (1).

$$\begin{cases} \begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix} = L_T \frac{d}{dt} \begin{bmatrix} i_{ga} \\ i_{gb} \\ i_{gc} \end{bmatrix} + \begin{bmatrix} S_a - \frac{S_a+S_b+S_c}{3} \\ S_b - \frac{S_a+S_b+S_c}{3} \\ S_c - \frac{S_a+S_b+S_c}{3} \end{bmatrix} v_{dc} \\ C \frac{d}{dt} v_{dc} = [S_a \quad S_b \quad S_c] \begin{bmatrix} i_{ga} \\ i_{gb} \\ i_{gc} \end{bmatrix} - i_{load} \end{cases} \quad (1)$$

Where,  $S_x$  stands for the state-switching equation, with a value that changes 1 or 0 depending on the switching state (on or off);  $v_{gx}$  represents the grid voltage,  $i_{gx}$  denotes the alternating current (AC) phase current, and the abc subscript indicates the three-phase system.  $i_{load}$  is the direct current (DC) output current,  $v_{dc}$ : the DC voltage;  $L_T$ : the total inductance, and  $C$ : the capacitance at the DC output.

By combining the state (1) and the Clarke transformation, the state-average model in the DQ coordinate system of the rectifier is presented as (2).

$$\begin{cases} \begin{bmatrix} (v_{gd})_{T_s} \\ (v_{gq})_{T_s} \end{bmatrix} = L_T \cdot \frac{d}{dt} \begin{bmatrix} (i_{gd})_{T_s} \\ (i_{gq})_{T_s} \end{bmatrix} + L_T \cdot \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \cdot \begin{bmatrix} (i_{gd})_{T_s} \\ (i_{gq})_{T_s} \end{bmatrix} + \begin{bmatrix} (d_d)_{T_s} \\ (d_q)_{T_s} \end{bmatrix} \cdot (v_{dc})_{T_s} \\ C \frac{d}{dt} (v_{dc})_{T_s} = \frac{3}{2} \cdot \begin{bmatrix} (d_d)_{T_s} & (d_q)_{T_s} \end{bmatrix} \cdot \begin{bmatrix} (d_d)_{T_s} \\ (d_q)_{T_s} \end{bmatrix} - (i_{load})_{T_s} \end{cases} \quad (2)$$

From small-signal model in DQ references in (2) can be written as DC in (3) and the disturbances in (4).

$$\begin{cases} V_{gd} = -\omega L_T I_{gq} + D_d V_{dc} \\ V_{gq} = \omega L_T I_{gd} + D_q V_{dc} \\ I_{load} = \frac{3}{2} (D_d I_{gd} + D_q I_{gq}) \end{cases} \quad (3)$$

$$\begin{cases} \hat{v}_{gd} = L_T \frac{d}{dt} \hat{i}_{gd} + D_d \hat{v}_{dc} + V_{dc} \hat{d}_d - \omega L_T \hat{i}_{gq} \\ \hat{v}_{gq} = L_T \frac{d}{dt} \hat{i}_{gq} + D_q \hat{v}_{dc} + V_{dc} \hat{d}_q - \omega L_T \hat{i}_{gd} \\ C \frac{d}{dt} \hat{v}_{dc} = \frac{3}{2} (D_d \hat{i}_{gd} + I_{gd} \hat{d}_d + D_d \hat{i}_{gq} + I_{gq} \hat{d}_d) - \hat{i}_{load} \end{cases} \quad (4)$$

Assuming stable grid voltage and load conditions, noise from load current, grid voltage can be neglected. Furthermore, the DC-link voltage is considered constant because the response time of the current control loop is much faster than the voltage control loop. Therefore, (4) can be expressed to (5).

$$\frac{d}{dt} \begin{bmatrix} \hat{i}_{gd} \\ \hat{i}_{gq} \end{bmatrix} = - \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \cdot \begin{bmatrix} \hat{i}_{gd} \\ \hat{i}_{gq} \end{bmatrix} - \frac{1}{L_T} \begin{bmatrix} \hat{d}_d \\ \hat{d}_q \end{bmatrix} V_{dc} \quad (5)$$

Figure 3 depicts the steps required to create a small signal model as well as a static operating point. The necessary mathematical equations and formulas are also provided in detail.

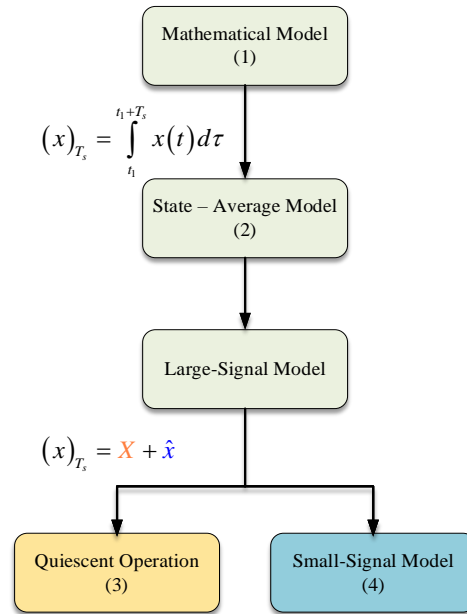


Figure 3. Small-signal modeling diagram

Based on (5), the converter is presented as a system with two inputs and two outputs. In which,  $\hat{d}_d$  and  $\hat{d}_q$  are input signals and  $\hat{i}_{gd}$ ,  $\hat{i}_{gq}$  are output signals. When controlling  $\hat{d}_d$  will affect both  $\hat{i}_{gd}$  and  $\hat{i}_{gq}$ . Similarly,  $\hat{d}_q$  will also affect both  $\hat{i}_{gd}$  and  $\hat{i}_{gq}$ . To simplify the system control design, a decoupling part will be added as shown in Figure 4. Assume that, the output of the current loop in d-q frame:  $\hat{d}_d = G_{PI} \cdot (\hat{i}_{gd}^* - \hat{i}_{gd})$  and  $\hat{d}_q = G_{PI} \cdot (\hat{i}_{gq}^* - \hat{i}_{gq})$ , respectively.

$$\begin{cases} \hat{d}_d = G_{PI} \cdot (\hat{i}_{gd}^* - \hat{i}_{gd}) - \frac{\omega L_T \hat{i}_{gq}}{V_{dc}} \\ \hat{d}_q = G_{PI} \cdot (\hat{i}_{gq}^* - \hat{i}_{gq}) + \frac{\omega L_T \hat{i}_{gd}}{V_{dc}} \end{cases} \quad (6)$$

Hence, (5) can be simplified as (7).

$$\frac{d}{dt} \begin{bmatrix} \hat{i}_{gd} \\ \hat{i}_{gq} \end{bmatrix} = - \frac{1}{L_T} \begin{bmatrix} \hat{d}_d \\ \hat{d}_q \end{bmatrix} V_{dc} \quad (7)$$

Now the converter can be controlled as a one-input and one-output system. In this way, the current controller for the d and q axes may have discretely controlled the d and q axes. The transfer function of the current duty cycle is reduced to (8).

$$\begin{cases} \frac{\hat{i}_{gd}(s)}{\hat{d}_d(s)} = - \frac{V_{dc}}{s L_T} \\ \frac{\hat{i}_{gq}(s)}{\hat{d}_q(s)} = - \frac{V_{dc}}{s L_T} \end{cases} \quad (8)$$

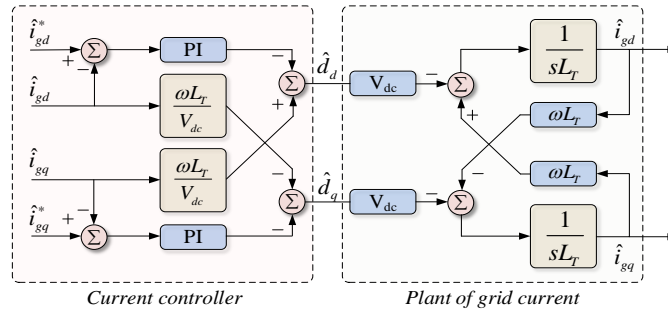


Figure 4. Block diagram of the current controller in the d and q axes

It is observed that changes and disturbances in the DC output voltage are related to variations in the duty cycle and grid current as in (9).

$$\frac{d}{dt} \hat{v}_{dc} = \frac{3}{2C} \cdot [\hat{d}_d \quad \hat{d}_q] \cdot \begin{bmatrix} I_{gd} \\ I_{gq} \end{bmatrix} + \frac{3}{2C} \cdot [D_d \quad D_q] \cdot \begin{bmatrix} \hat{i}_{gd} \\ \hat{i}_{gq} \end{bmatrix} \quad (9)$$

The active power in the system is directly determined by the d-axis current. This relationship exclusively links the DC voltage to the d-axis, playing a crucial role in balancing both AC and DC power in the converter, with the assumption of neglecting losses. The output capacitor's substantial capacitance contributes to high inertia, providing stability to the DC voltage. Additionally, when the power factor reaches unity, signifying a perfect balance between real and reactive power, the q current remains at zero. Consequently, the relationship between the DC voltage and the d current can be expressed as (10).

$$\frac{\hat{v}_{dc}}{\hat{i}_{gd}} = \frac{3}{2sC} D_d = \frac{3V_g}{2sV_{dc}C} \quad (10)$$

In practice, the controller needs to consider the transmission delay caused by PWM techniques. The converter employs symmetric waveforms as shown in Figure 5. Two common sampling methods are illustrated in Figure 5, where Figure 5(a) represents single sampling - meaning one sample per cycle, and Figure 5(b) represents double sampling. For the data transmission delay  $T_{dtr}$  is the interval time between the PWM conversion and the data sample. Regarding the sampling period  $T_{sa}$  is related to the sampling delay  $T_{dsa}$ . The delay time is in the range of hundreds of microseconds, it can be expressed as a first-order inertial stage as in (11).

$$G_d(s) = \frac{1}{T_d s + 1} \quad (11)$$

where  $T_d$  is the inertia time of the PWM converter and has a value of  $1.25T_{sw}$  for single sampling and  $0.75T_{sw}$  for double sampling. Additionally, another crucial point during sampling at points such as in Figure 5 will help avoid many  $dV/dt$  when the switches are closed.

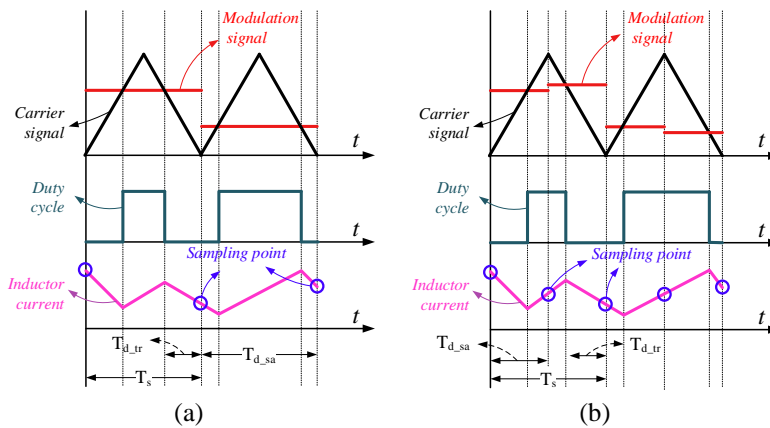


Figure 5. Time delay in sampling delay and transmission in digital control: (a) single-sample and (b) double-sample

Based on the Bode plot in Figure 6(a), it is observed that at low frequencies, the amplitude and phase responses of both the LCL filter and the L filter are similar. However, the LCL filter exhibits a resonance peak. This resonance peak can potentially destabilize the system if the filter or control system is not well-designed. The performance of the controller will be verified through simulation and experimentation results.

To control the DC voltage, a PI controller is used to regulate the DC voltage error to zero. The control scheme includes a low-pass filter in the control loop to separate high-frequency harmonics from the measured signal. To design the voltage control loop in Figure 6(b), the current control loop can be treated as a closed-loop system which controls the reference signal entirely within its bandwidth and helps mitigate its impact on the outer loop design.

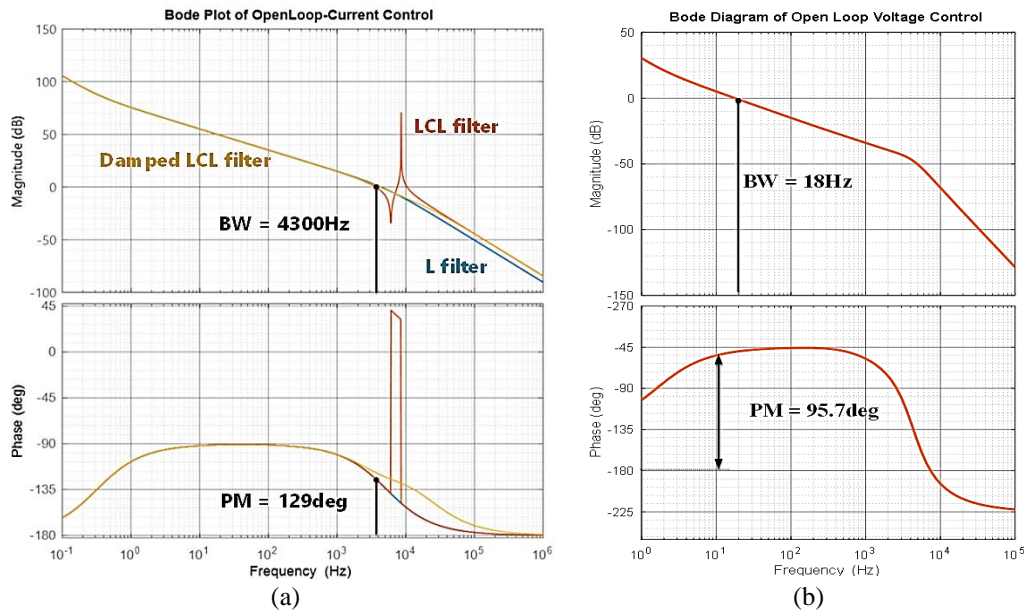


Figure 6. Comparison of bode diagram: (a) the open-loop current control with a conventional L-filter model, LCL filter model, LCL filter with damping resistor and (b) open-loop of the voltage control

### 3. LCL FILTER DESIGN PROCEDURE

The active rectifier employs a three-phase inverter capable of supplying bidirectional power and sinusoidal current with a unity power factor. Achieving standard sinusoidal waveforms is challenging with power electronic converters, so standards often limit the total harmonic distortion (THD) to around 5% and the amplitude of each harmonic component of the grid-fed current. Considering these harmonic limits, an L filter (inductor) connecting the converter may require an excessive inductance value. This makes the L filter bulky, heavy and expensive. It can increase the losses in the converter due to high voltage drop. While the LCL filter allows for a lower inductance value, making it more compact and lower losses. To ensure a well-designed LCL filter meets the key criteria, the criteria are presented:

- Control of current harmonic distortion: Harmonics other than the fundamental harmonic should be controlled to ensure their amplitudes are sufficiently small, reducing the total harmonic distortion (THD) ratio of the grid current. Ensure compliance with the IEEE 519-1992 standard [28], as shown in Table 1, to guarantee quality and adherence to standards in power systems.
- Calculation of maximum reactive power: Calculate the maximum reactive power on the LCL filter capacitor to ensure operation at a unit power factor.
- Control of total impedance: Maintain the total impedance of the filter below 10% of the output impedance to avoid voltage drop issues across the filter.
- Elimination of resonance issues and maintenance of stability: Ensure that the resonance frequency is between ten times the fundamental frequency and half of the switching frequency to eliminate resonance issues and maintain system control stability. In summary, adhering to and implementing these criteria will help ensure stable performance and quality of the LCL filter in the power system.

As shown in Figure 7, the equivalent circuit diagram represents a single-phase system for analysis and design of the LCL filter. Here,  $v_g$  represents the phase grid voltage and  $v_i$  represents the switching voltage. In this

configuration, the LCL filter is intended to filter out all harmonic sources from the inverter  $v_i$ . To achieve the four criteria mentioned above, the LCL filter design process proposed in this paper consists of the following steps:

- Step 1: Calculate the maximum capacitance value of the LCL filter capacitor based on the reactive power that the filter needs to absorb, as in (12).

$$Q_{C_f} \leq \frac{P}{3} \frac{\sqrt{1-PF^2}}{PF} \quad (12)$$

In which,  $Q_{C_f}$  is the reactive power value [Var] that capacitor  $C_f$  [F] needs to absorb. PF is the desired power factor. P is the input power consumption. In this case, the required capacitance value  $C_f$  can be calculated as (13).

$$C_f \leq \frac{P\sqrt{1-PF^2}}{3PF\omega_1 V_{g,rms}^2} \quad (13)$$

- Step 2: Assume the grid voltage is sinusoidal. In this case, at high frequencies, specifically at the frequency of the switching harmonics  $h_{sw}$ , the grid source is considered short-circuited. Applying Kirchhoff's law, as in (14).

$$i_i(h_{sw}) = \frac{v_i(h_{sw}) - v_{C_f}(h_{sw})}{L_i \omega_{sw}} \quad (14)$$

Where,  $i_i$  is the converter-side current;  $v_{C_f}$  is the LCL capacitor voltage;  $L_i$  is the converter-side inductor;  $\omega_{sw}$  is switching frequency [rad/s];  $v_i$  is switching voltage. At the switching frequency,  $v_i(h_{sw})$  can be expressed as (15).

$$v_i(h_{sw}) = \frac{1}{\sqrt{2}} m_{a,sw} \frac{V_{dc}}{2} \quad (15)$$

Where,  $m_{a,sw} = \frac{v_i(h_{sw})}{0.5V_{dc}}$ : the ratio voltage between switching and fundamental harmonic. The converter-side current can be written as (16).

$$I_i(h_{sw}) = \frac{m_{a,sw} V_{dc}}{2\sqrt{2}\omega_{sw}} \quad (16)$$

Assumed  $\gamma_{Li} = \frac{i_i(h_{sw})}{i_i(h_{\omega 1})}$  is the amplitude ratio of converter-side current at switching frequency and fundamental harmonic. The inductance of converter side is calculated as (17).

$$L_i = \frac{3m_{a,sw} V_{dc} V_{g,rms}}{2\sqrt{2}\omega_{sw} \gamma_{Li} P} \quad (17)$$

Based on the single phase equivalent circuit in Figure 2, the grid current in the s-domain can be written as (18).

$$I_g(s) = I_i(s) \frac{1}{s^2 L_g C_f + 1} \quad (18)$$

At fundamental harmonic (50 Hz), the current of LCL capacitor can be neglected. Hence, grid current can be approximately equal to converter-side current  $I_g(\omega_g) \approx I_c(\omega_g)$ . Assumed  $\gamma_{Lg} = \frac{i_g(h_{sw})}{i_g(h_{\omega 1})}$  is the ratio of the amplitude of the short-circuited harmonic current to the fundamental harmonic. As a result, grid side inductance is calculated as (19).

$$L_g = \frac{\gamma_{Li} - \gamma_{Lg}}{\omega^2 \gamma_g C_f} \quad (19)$$

- Step 3: Utilize constraints in the LCL design: Concerning the resonance frequency, it must ten times between the grid and half of the switching frequency to avoid resonance issues as is (20) [16].



$$\begin{cases} 10f_g < f_{res} < 0.5f_{sw} \\ Z_{LT}(p.u) < 0.1 \end{cases} \quad (20)$$

With  $f_{res} = \frac{1}{2\pi} \sqrt{\frac{L_i + L_g}{L_i L_g C_f}}$  is the resonant frequency of the LCL filter and  $Z_{LT}(p.u) = \frac{Z_{LT}}{Z_{in}} = \frac{\omega_1(L_g + L_i)P}{3V_{g,rms}^2}$  is the total impedance of the LCL filter.

Table 1. Current limits based on IEEE 519-1992 standard

Maximum odd harmonic current distortion in percent of grid current for general distribution systems (120 V - 69 kV)					
$h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h$	TDD
4.0	2.0	1.5	0.6	0.3	5.0

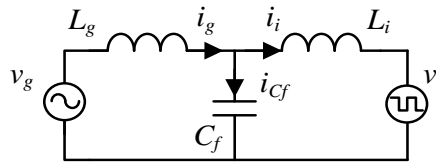


Figure 7. The single-phase equivalent circuit of LCL filter

Figure 8 illustrates the influence of  $\gamma_{Li}$  and  $\gamma_{Lg}$  on the inductance values of the converter-side, grid-side inductors. In this case,  $\gamma_{Li}$  not only affects  $L_i$  but also alters  $L_g$ . Meanwhile,  $\gamma_{Lg}$  only affects  $L_g$ . It can be observed that as  $\gamma_{Lg}$  gradually approaches 0 (meaning the amplitude of the short-circuit harmonic is much smaller than the fundamental amplitude), the required value of  $L_g$  becomes significantly large. Conversely, a larger value of  $\gamma_{Li}$  results in smaller  $L_g$ . Similar observations apply to  $\gamma_{Li}$ . Therefore, to design an LCL filter with minimal total impedance, avoiding losses, and reducing costs, the  $L_g$  value should be equal to  $L_i$ .

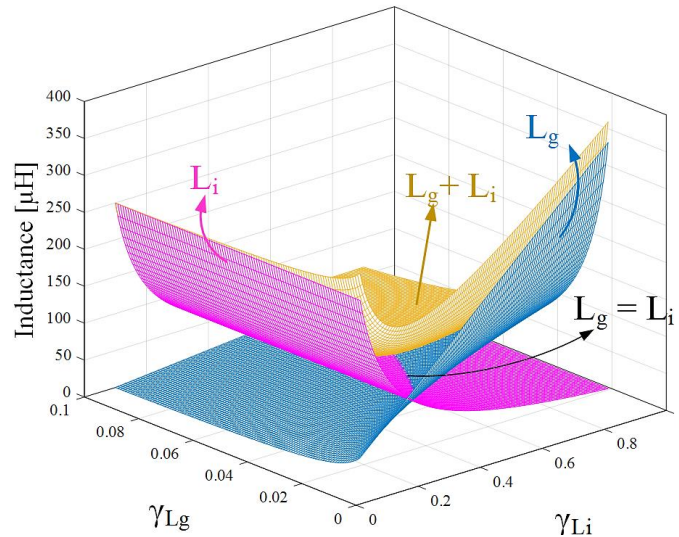


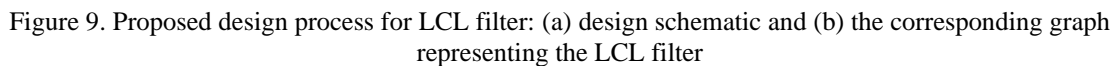
Figure 8. The impact of choosing the power factor on the LCL filter inductance

Most power factor standards require a power factor above 0.85. In this paper, a power factor of 0.999 is chosen. Consequently, the maximum capacitance  $C_f$  is calculated to be 125  $\mu$ F. The chosen  $C_f$  value will affect  $L_g$  and  $L_i$ . Typically, this value is selected to be between one-third and one-tenth of the maximum value. The final chosen value for  $C_f$  is 10  $\mu$ F. Through harmonic spectrum analysis,  $m_{a,sw}$  is determined to be 0.82. Therefore,  $\gamma_{Lg}$  should be selected in the range of 0.25 to 0.6, while  $\gamma_{Li}$  is chosen in the range of 0.01 to 0.03 to completely eliminate high grid current harmonics.

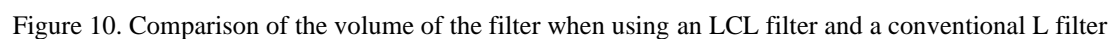
Figure 9(a) represents a simplified LCL filter design process, and Figure 9(b) provides a design example for a 40 kW system. Based on Figure 9(b),  $\gamma_{Li}$  can be chosen as 0.354 to minimize the total impedance



The L filter has a significantly larger inductance value compared to the LCL filter to achieve the same THD value. Therefore, the L filter requires a larger core volume than the LCL filter. In Table 2, the comparison of the core volume between the conventional L filter and the LCL filter can be observed. Table 2 shows that the conventional L filter uses nine cores (three cores per phase), with a total volume of 3,290.67 cm<sup>3</sup> during operation. Meanwhile, the LCL filter only needs six cores (two cores per phase) with a total volume of 316.86 cm<sup>3</sup>. Therefore, using the LCL filter not only reduces costs but also increases power density. This comparison is clearly illustrated in Figure 10.



Type of filter	L Filter	LCL filter
Core selection	CH165125	CH610060
Number of cores	9	6
Core volume	365.63cm <sup>3</sup> /core	52.81cm <sup>3</sup> /core



#### 4. SIMULATION AND EXPERIMENTAL RESULTS

In this section, simulation results will be presented to validate the operation of the converter and the effective high-order harmonic filtering capability of the designed LCL filter in both continuous and time domains. The software PSIM and MATLAB are used, and the simulation parameters are used consistently for the validation cases presented in Table 3.

Table 3. Simulation and experimental parameters

Parameters	Values
Power	40 kW
DC link voltage	820 V
Grid frequency	50 Hz
AC input voltage (line to line)	380 V
Switching frequency	25 kHz
The inductance of converter side	61.5 $\mu$ H
The inductance of grid side	61.5 $\mu$ H
The capacitor of LCL filter	10 $\mu$ F
The capacitor of DC link	90 $\mu$ F

##### 4.1. Simulation results at steady state

Figure 11 presents the simulation results of the converter with the LCL filter during initialization. The simulation results demonstrate appropriate controller parameters and provide the control signal outputs that align with the set values. Regarding the DC voltage, the voltage ripple  $\Delta V$  is 14 V, the average voltage  $V_{dc}$  is 820.0 V, and the peak voltage  $V_{max}$  is 828 V. The grid-side current has a total harmonic distortion (THD) of 0.875%, and the effective value of the fundamental current is 62.6 A. The power factor achieves 0.999.

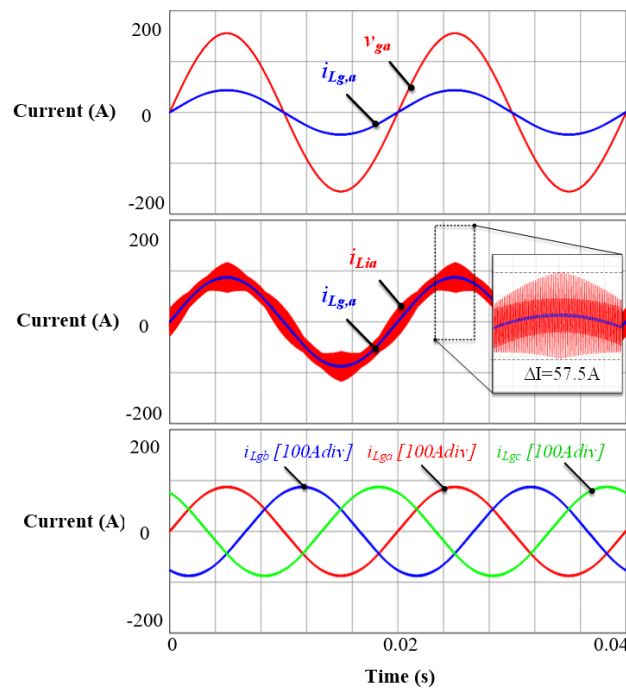


Figure 11. Simulation waveforms of converter at steady state full load

##### 4.2. Experimental results

An experimental setup was built in laboratory to verify the proposed method. Figure 12(a) depicts the three-dimensional design model, which includes the printed circuit board (PCB) circuits and LCL filter. The experimental setup for a 40 kW three-phase connected is shown in Figure 12(b) which including power board, DSP board, LCL filter, sensors, and the capacitors. The experimental parameters are matched with the simulation ones to confirm the proposed method. These parameters are presented in Table 3.

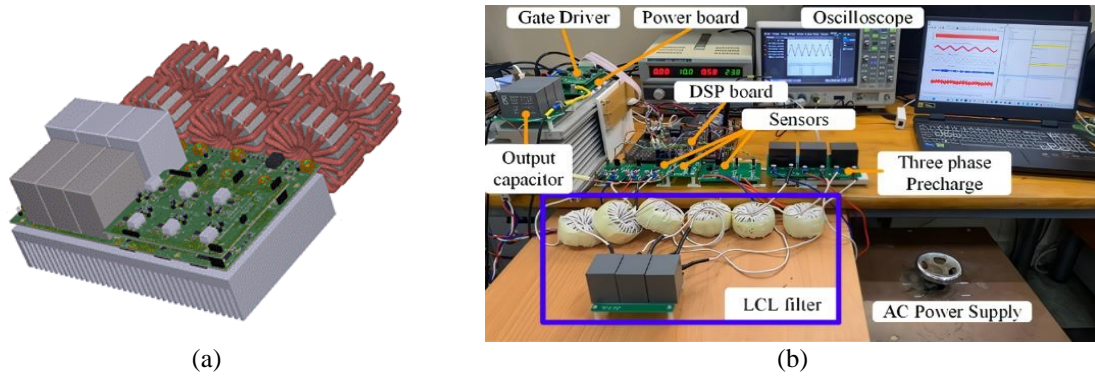


Figure 12. Experimental process of proposed method: (a) 3D design model and (b) experimental setup

#### 4.2.1. Current sampling method

During the experiment, the measurements were conducted with feedback signals for control purposes, such as alternating current from the converter-side, grid voltage, and DC output voltage, under various operating conditions. This ensured that the measurement circuits operated well through multiple tests. Figure 13 illustrates the AC current on the converter-side and the voltage on the analog-to-digital converter (ADC) pin of the DSP. After reading these values, low-pass filter functions were used in the control software to eliminate unnecessary signals. Additionally, to ensure no phase discrepancies, the paper used functions to calibrate the magnitude and coefficient of the current sensor. The result was a well-functioning current sensor with minimal phase discrepancies. Figure 13 also indicates noise due to the large rate of change of voltage  $dv/dt$  causing voltage spikes in the feedback signal. However, this had little impact on the measured values as the sampling point was at the beginning of the waveform, where noise interference is minimal. Similar to the current sensor, the voltage sensor was also calibrated through software to achieve high accuracy. This ensured that the measured values closely followed the required values.

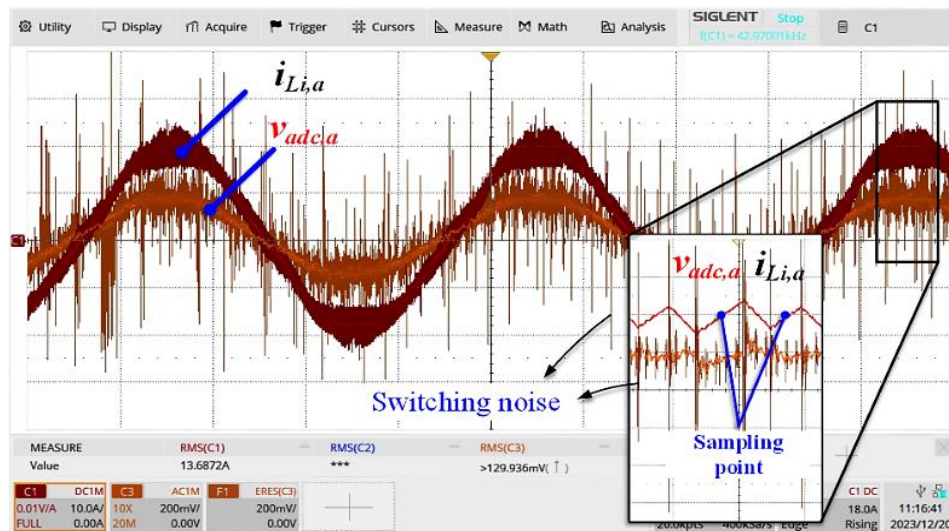


Figure 13. Converter-side current and ADC sampling voltage

#### 4.2.2. Power factor correction

Figure 14 shows the control results of the converter to achieve a power factor of 0.999 as per the design requirement. The results showed that the voltage and current at the input have a phase deviation of approximately 5 degrees. In this case, the power factor can be calculated to be close to the cosine of the phase deviation between the phase voltage and phase current – in this instance, reaching 0.996, surpassing 0.99.

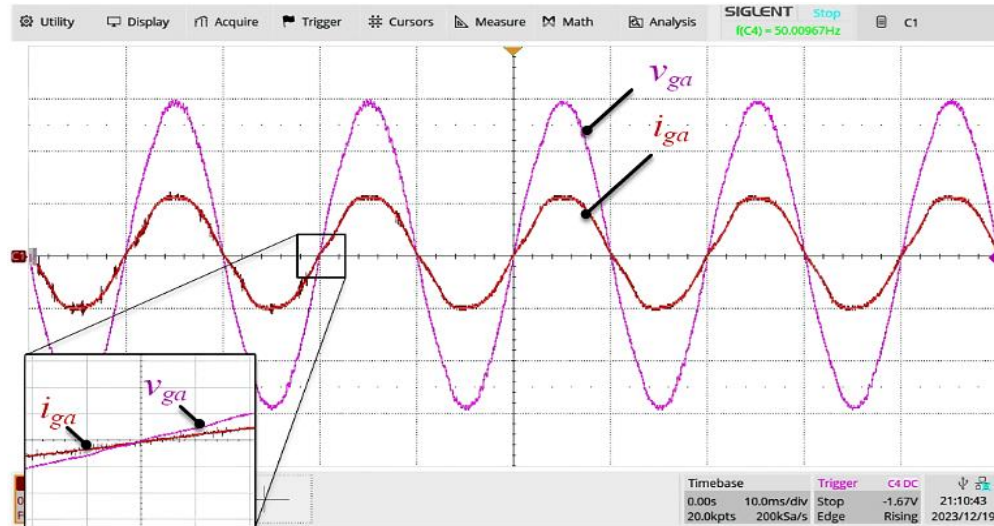


Figure 14. Measurement results and evaluation of grid-side current on one phase

#### 4.2.3. Analysis of grid-side current

Setting the control current at 25 A, the converter control is conducted, and the results are recorded. Due to device load limitations for the converter, this study only performs up to a current of approximately 25 A. Figure 15 presents the measured and THD analysis results for phase A grid-side current. The results show that at 25 A, the grid current has a THD of 2.81%.

FFT analysis for the grid-side current at the low frequency and cutoff frequency is presented in Figure 16. Some low-order harmonics in Figure 16(a) also affect the THD value of the current. The main cause is the unbalanced input AC voltage. This will be improved in further research by using harmonic compensators of orders 3, 5, 7, and so on. It can be noted that the higher-order harmonics from the cutoff frequency have significantly attenuated, with reduced amplitudes:  $I_{hsw} = 0.78$  A,  $I_{2hsw} = 0.28$  A, and  $I_{3hsw} = 0.05$  A as presented in Figure 16(b).

#### 4.2.4. Changing demand voltage

When changing the set voltage from 700 V to 920 V and then back to 810 V, the entire experimental system performed well. The DC voltage was controlled without any overshoot and undershoot. The voltage ripple at 920 V was 3.5% - meeting the design requirements. The experimental result is presented in Figure 17.

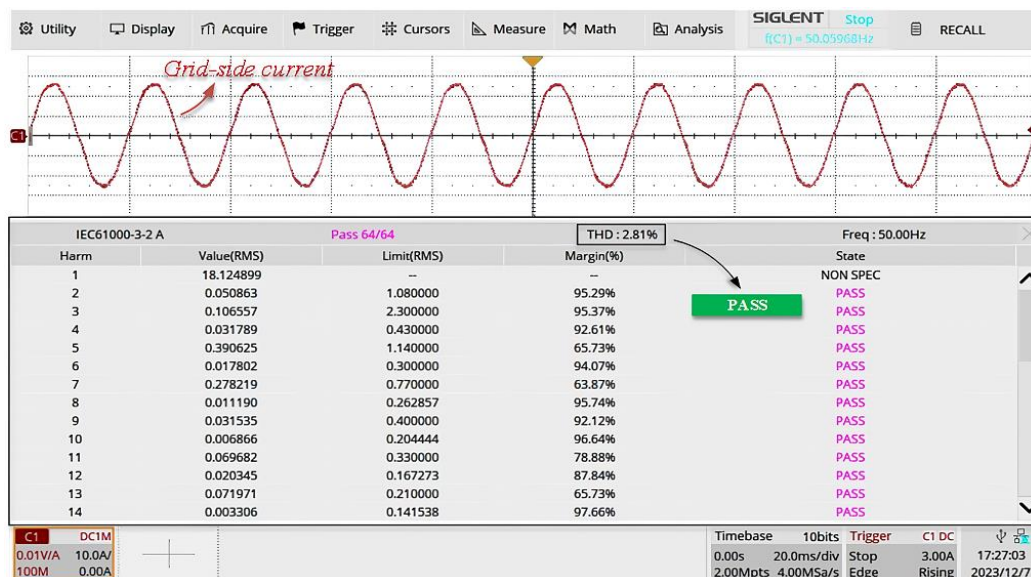


Figure 15. Measurement results and evaluation of grid-side current on one phase



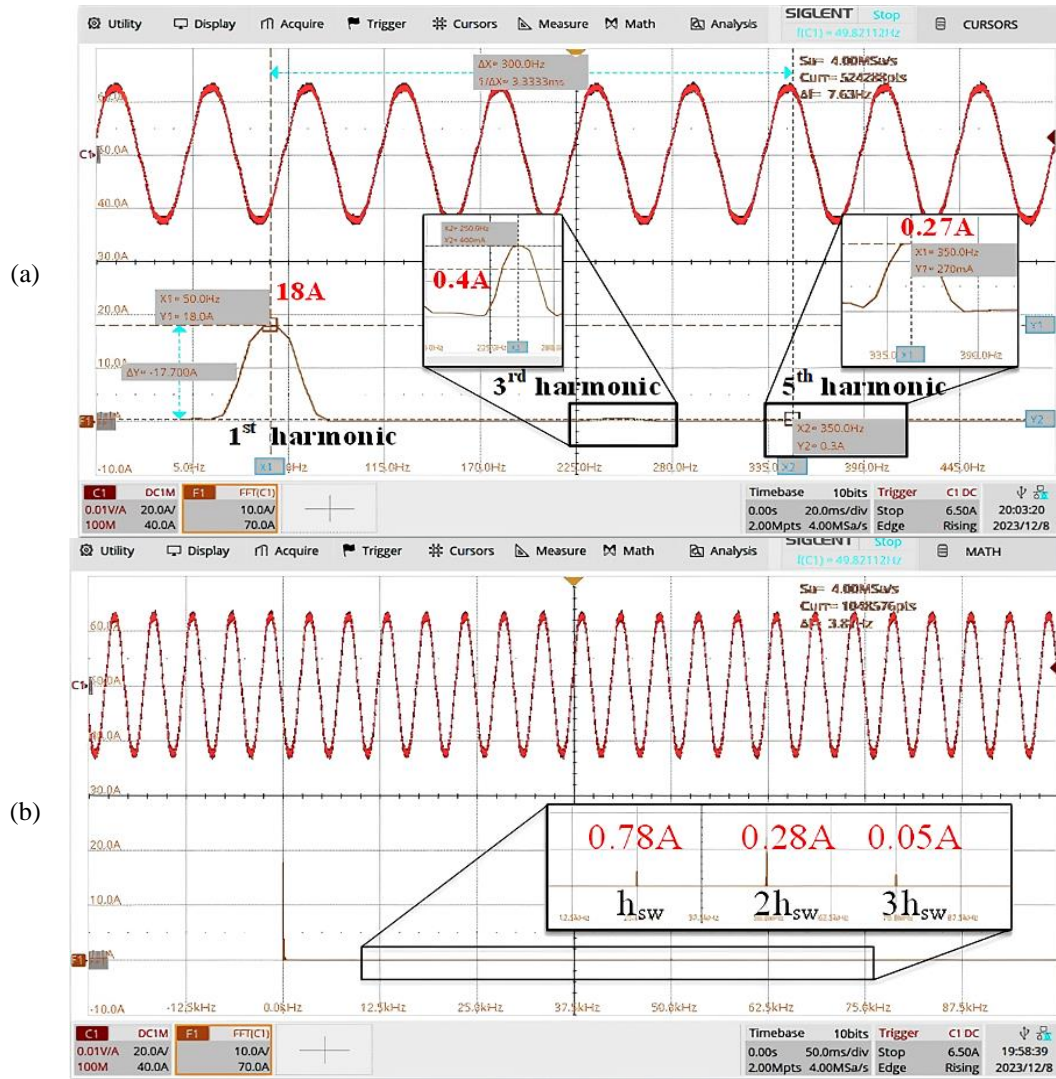


Figure 16. FFT analysis for the grid-side current at (a) low frequency and (b) cutoff frequency

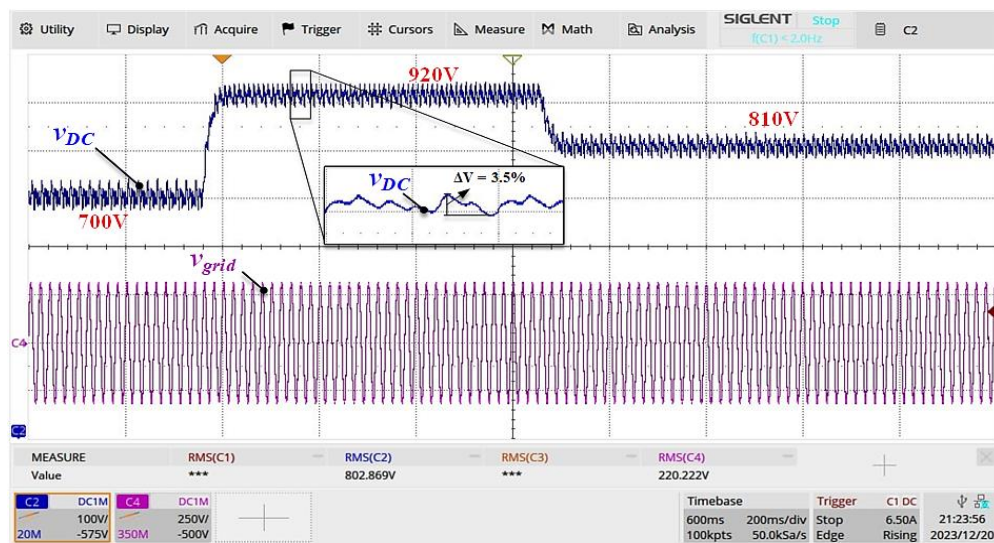


Figure 17. Experimental results of control voltage variation

## 5. CONCLUSION

This study has focused on the crucial aspect of LCL filter design within the context of bidirectional chargers. The conventional components, such as transformer filter cores in DC-DC converters or L-filter cores, contribute significantly to the increased weight and size of chargers. To overcome these limitations, our proposed LCL filter design offers a promising solution.

The application of the LCL filter design procedure for a 40 kW three-phase converter, acting as the power factor correction (PFC) stage of the onboard charger, demonstrates its effectiveness. The cascade control designed for DC output voltage and input current further validates the practicality of the proposed solution. Both PSIM simulation and experimental results showcase the successful implementation of the LCL filter design and control system. By reducing the size and weight of chargers without compromising efficiency, our LCL filter design contributes to the ongoing efforts in making high-power density AC/DC converters for electrical charger applications. As the electric vehicle industry continues to expand, innovations like the proposed LCL filter design are crucial for meeting the evolving needs of consumers and driving environmental sustainability.

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