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Single-phase five level modified neutral point clamped grid connected inverter topology with front-end chopper control of DC-link capacitor voltages

Y. Sravan Kumar[1], T. Murali Krishna[2], Yesuratnam Guduri[1]
[1]Department of Electrical Engineering, University College of Engineering, Osmania University, Hyderabad, India
[2]Department of Electrical and Electronics Engineering, Chaitanya Bharathi Institute of Technology, Hyderabad, India

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ABSTRACT

Conventionally, only the standalone operation of a single-phase fault tolerant-based 5-level neutral point clamped (SPFT-5L-NPC) inverter with two stiff DC sources has been explained with consideration of phase disposition pulse width modulation (PD-PWM) technique. In this topology, the bidirectional switch arrangement consists of four diodes and one IGBT switch. This arrangement inherently increases conduction losses of topology. Generally, any NPC inverter topology suffers from a DC-link capacitor voltage (DCL-CV) balancing issue. In the conventional contribution of work, authors have not discussed the front-end voltage balancing issue. This study describes the extension work of a single-phase grid connection with a modified 5L-NPC (M5L-NPC) inverter topology, taking into account the aforementioned concerns. In this topology, the simple front-end chopper circuit has been utilized to balance the DCL-CVs and to reduce conduction losses, another arrangement of bidirectional switch has been utilized. In this paper, both standalone and grid connections of M5L-NPC topology have been explained along with control of DCL-CVs. The grid-connected important objectives of active power control (APC), reactive power control (RPC), and injecting sinusoidal current with low harmonic distortion have been discussed thoroughly considering a simple control strategy.

Corresponding Author:

Y. Sravan Kumar
Department of Electrical Engineering, University College of Engineering, Osmania University
Hyderabad, Telangana, India
Email: y.sravan16@gmail.com

1. INTRODUCTION

In multilevel inverters (MLIs), the lower dv/dt minimizes electromagnetic interference, while the increased number of components may lower reliability. To obtain higher reliability, the fault tolerance of multilevel structures serves as a compensating factor [1]. As the number of levels rises, the traditional NPC inverter design results in uneven losses in the semiconductor components increases cost, and decreases the reliability [2]. The traditional flying capacitor (FC) based MLIs need a large number of FCs, and additional voltage sensors are needed to balance these capacitors. Then it leads to lower reliability as going to higher levels [3].

The cascaded H-Bridge (CHB) MLI topologies offer higher modularity and dependability. Nonetheless, a greater quantity of separate DC sources is required [4]. In comparison to the FC and NPC-MLI topologies, the nested neutral point clamped (NNPC) topology features fewer clamping diodes and fewer FCs, but it is less reliable due to uneven voltage distribution on switches [5]. A five-level F-type inverter topology is suggested in [6], however the meaning of dependability is not clarified. The carrier-overlapped PWM solution is proposed to address the neutral point voltage disparity issue in the traditional 5L-NPC inverter design [7], however, the reliability concept has not been addressed.

The idea of reliability is not described in [8], which discusses only a capacitor voltage balancing with the utilization of redundant states for the traditional 5L-FC-based inverter topology. A hybrid MLI topology is suggested in [9], however, to provide 5L-output voltage, more components are required. A 5L-H-Bridge type NPC inverter topology without fault tolerance concept using an improved PWM approach is described in [10], however, this design also requires a higher component count.

A SPFT-5L-NPC topology with redundant states is described in [11]. However, this just explains the standalone operation and the authors have not described the DCL-CV balance problem also. Several topologies with common DC links have been laid out in the literature [12]. A summary of various fault-tolerant MLI topologies can potentially provided in [13]. The result [14]-[16], various DCL-CV balancing control strategies have been explained but these are complex. Hence, it is necessary to develop a simple control strategy to apply all common DC-link-based inverter topologies to ensure safe operation.

Aside from this, improving the quality of the output voltage for any MLI design also depends on the PWM implementation. Although space vector modulation strategies for NPC-MLI topology have been reviewed in [17], the intricacy of control becomes burdensome as one moves to higher levels. Several kinds of multi-carrier PWM schemes have been discussed in [18]. In these, the PD-PWM gives an excellent harmonic profile but implementation needs more triangular carrier signals. An absolute function unipolar PD-PWM (UPD-PWM) has been reported in [19], [20] to simplify the PD-PWM stage. The triangular carrier count can be cut in half with this UPD-PWM strategy.

The DCL-CV accounts for the complete grid connection while taking H-bridge topology into account [21]. It is balanced through the battery using a bidirectional converter. The sliding mode control approach for a 1-phase grid-connected H-Bridge inverter topology has been documented in [22]. The phase-locked loop (PLL), which has been explained in [23], is generally considered to be crucial when thinking about any grid operation. The grid control approach based on the orthogonal signal generator (OSG) and featuring two proportional-integral (PI) controllers was documented in [24]. A dq-frame control scheme for grid operation has been disclosed in [25]. For grid operation, the linear quadratic controller has been described in [26]. A simple control technique must be needed because all of the existing grid-connected control strategies are complicated.

In this paper, the DCL-CV balancing and single-phase grid connection with various dynamic investigations have been discussed by taking into account the modified SPFT-5L-NPC topology. The DCL-CVs are balanced by employing a straightforward chopper-based control method, which works with all popular DC-link MLI topologies. A straightforward current control approach has been used to explain single-phase grid operation, which reduces computation effort. The rest of the paperwork is organized as follows. In section 2, the circuit description of the proposed M5L-NPC grid-connected inverter (GCI) topology and control strategy for balancing DCL-CVs have been discussed. In section 3, the control strategy for grid connected operation (GCO) has been explained. In section 4, the simulation results of both standalone and GCO have been explained. In section 5, the comparative study between conventional and extension work of the proposed topology has been discussed. Finally, conclusions are reported.

2. CIRCUIT DESCRIPTION OF PROPOSED M5L-NPC GCI TOPOLOGY AND CONTROL STRATEGY FOR BALANCING DCL-CVS: CHOPPER CIRCUIT

2.1. Circuit description of proposed M5L-NPC GCI topology

In the literature, only the stand-alone operation of an SPFT-5L-NPC inverter topology has been discussed [11]. The conventional SPFT-5L-NPC inverter topology is depicted in Figure 1. However, this topology needs two DC sources and the conventional bidirectional switch with four diodes increases conduction losses. The front-end voltage balancing problem has not been covered by authors in the traditional contribution of work. To explain the grid connection operation, a M5L-NPC inverter topology has been proposed and it is depicted in Figure 2 which is a modified version of SPFT-5L-NPC topology. It consists of one DC source along with a chopper control circuit and to reduce conduction losses, the conventional bidirectional switch has been replaced with two diodes and two IGBTs which are connected in anti-parallel. The new connected bidirectional switch is operating under a common emitter (CE) configuration thereby only one gate driver circuit is needed.

The front-end chopper circuit consists of two IGBT switches, one resistor, one inductor, and two DC-link capacitors. This independent chopper circuit easily provides an equal amount of balancing voltages at DC-link capacitors (C_1 and C_2) and the respective control action has been explained in this sub-section. At the end, an inductor filter and grid have been connected to the topology.

After balancing the DCL-CVs with chopper control, the switching operation of the inverter topology at each state is important and it is depicted in Table 1. To produce 0 V_{dc}, the switches S_2-S_3-S_5 should be turned ON, and the remaining are in the OFF state. By turning ON the one of redundant states of S_1-S_2-S_5 switches, the inverter generates 0.5 V_{dc} at the output. To produce 1Vdc, the switches S_1-S_2-S_7 should be turned ON, and the remaining are in the OFF state.

By turning ON S_2-S_3-S_6 switches, the inverter generates -0.5 V_{dc} at the output. Similarly, to produce -1 V_{dc}, the switches S_3-S_4-S_6 should be turned ON, and the remaining are in the OFF state. Finally, the topology provides five levels at the output with peak values of ±1V_{dc}. At each stage, only three switches are conducting and else are in OFF mode. The drawback of this topology is, it provides only unity gain.

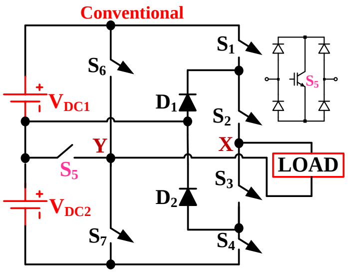

Figure 1. Conventional SPFT-5L-NPC inverter topology

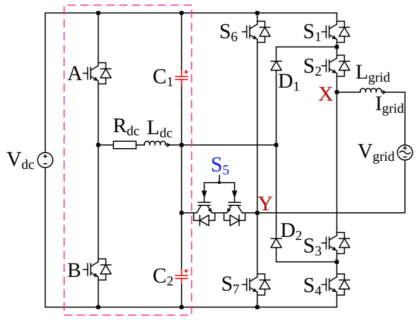

Figure 2. Proposed M5L-NPC GCI topology-extension of work

Table 1. Switching operation

S. No	V_{XY}	ON State Switches
1.	0 V_{dc}	S_2-S_3-S_5
2.	0.5 V_{dc}	S_1-S_2-S_5
3.	1 V_{dc}	S_1-S_2-S_7
4.	-0.5 V_{dc}	S_2-S_3-S_6
5.	-1 V_{dc}	S_3-S_4-S_6

2.2. Control strategy for balancing DCL-CVs: Chopper circuit

In Figure 2, the dotted line portion represents the chopper circuit, and the respective proposed control strategy is depicted in Figure 3. In this control strategy, RO indicates the relational operator and PB indicates the product block. Firstly, sense each DCL-CV (V_{c1} and V_{c2}) and compare with the reference half of DC-bus voltage. The obtained outputs have been multiplied and it gives respective switching pulses to A and B switches.

Finally, capacitors' corresponding charging and discharging operation through R_{dc} and L_{dc} leads to balancing the capacitor voltages at the desired reference voltage level. The implementation of the chopper control strategy is simple and it is effectively suitable for different types of front-end DC-link-based inverter topologies.

To attain the grid-connected objectives of APC, RPC, and injecting sinusoidal current with low harmonic distortion, a proper simple control strategy should be required to reduce the computational burden on the real-time processor units. Figure 4 represents a conventional dq-frame-based current control strategy for 1-phase grid-connected systems. In this, the implementation requires more transformation blocks, more PI controllers (tedious tuning), and more mathematical operations.

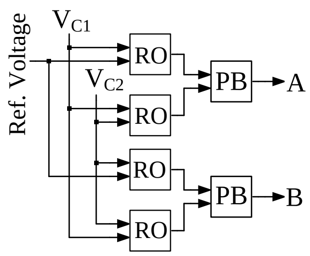

Figure 3. Proposed control strategy for chopper circuit

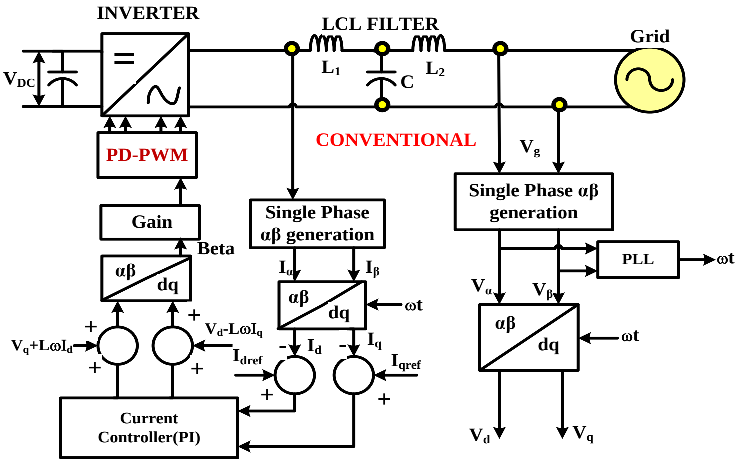

Figure 4. Conventional dq-frame control strategy: grid operation

After generating a modulating signal from the control algorithm, at the end stage of implementation, the authors have generally used the conventional PD-PWM technique. In this PWM technique, to generate a five-level output, four triangular carriers are required and the rest of the implementation process also increases. To reduce the complexity of the grid operation control strategy along with the PWM stage, a simple control strategy has been implemented to attain all required objectives and it is applied to the proposed M5L-NPC topology. The proposed grid-connected current control strategy along with the UPD-PWM technique is depicted in Figure 5. The UPD-PWM technique has been adopted from [19], [20]. Its implementation needs only two carrier signals to generate a 5-level output voltage and the rest of the implementation is also simple as compared with the PD-PWM technique.

The operation of the proposed grid-connected current control strategy has been explained in the following steps. Its implementation is simple as compared with the traditional dq-frame control strategy along with the PWM stage.

a. In GCO, firstly, sense the grid voltage (V_{grid}) and grid current (I_{grid}).
b. The V_{grid} is fed to a PLL and it provides grid synchronization.
c. The obtained output is fed to the sinusoidal term.
d. This can be multiplied with a peak value of the grid current (I_{peak}) and it gives the reference value of the injected grid current (I_{ref}).
e. The Iref is compared with Igrid and the error output is fed to the PI controller.
f. The PI output gives a reference signal for the PWM stage.
g. To generate the necessary switching pulses, the UPD-PWM has been employed.
h. Finally, the complete control strategy provides all the objectives of a grid-connected system.

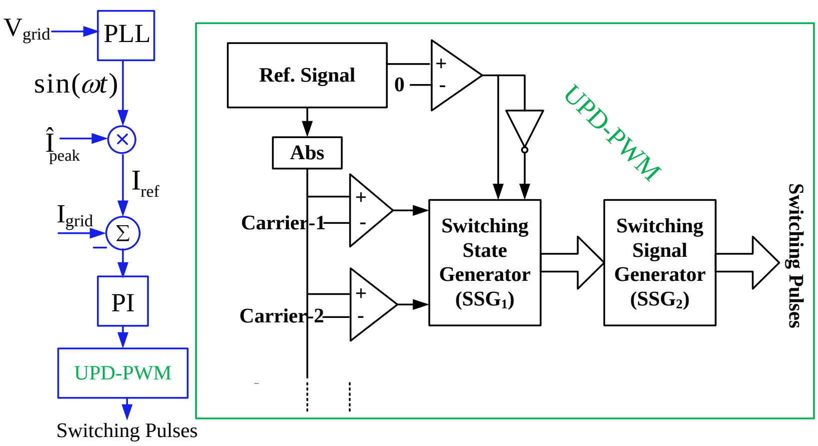

Figure 5. Control strategy for proposed M5L-NPC topology: GCO

3. SIMULATION RESULTS: STANDALONE AND GCO-PLECS TOOL

3.1. Standalone operation: R and RL-loads

Before going to GCO, the proposed work has been tested in standalone mode with only consideration of the UPD-PWM technique. Here the standalone operation is nothing but resistive and inductive loads only. In standalone operation the value of the switching frequency considered is 5 kHz. By considering UPD-PWM technique the number of triangular carriers can be reduced to half as compared with level shifted PWM technique. Table 2 represents simulation parameters for the standalone mode.

By considering the step change of load (R to RL) and step change of modulation index (MI) =1 to 0.5 at t=0.06 sec, the following simulation results are obtained which are depicted in Figure 6. In this, the first result represents UPD-PWM technique with MI=1 to 0.5. The second and third results show DCL-CVs which are balanced at 200 V with less voltage ripple. The fourth result shows inverter output voltage (IOV: V_{XY}) and it gives 5 levels with a peak value of ±400 V at MI=1.0 and similarly, it generated 3 levels with a peak value of ±200 V at MI=0.5.

The final result represents the corresponding step change of load current waveforms. In the resistive load operation with MI=1.0, the peak value of load current approximately at 4 A has been obtained. Similarly, in the RL-load operation with MI=0.5, the peak value of load current is approximately 1.85 A has been obtained. Even step change of load and step change of MI, the chopper control strategy effectively balances the DCL-CVs at the desired voltage level.

Table 2. Simulation parameters-standalone operation

S. No	Parameter	Value
1.	Resistor-load	100 Ω
2.	Inductor-load	80 mH
3.	Switching frequency	5 kHz
4.	DC-link: V_{dc}	400 V
5.	Chopper-C_1	1000 μF
6.	Chopper-C_2	1000 μF
7.	Chopper-R_{dc}	0.1 Ω
8.	Chopper-L_{dc}	0.01 mH

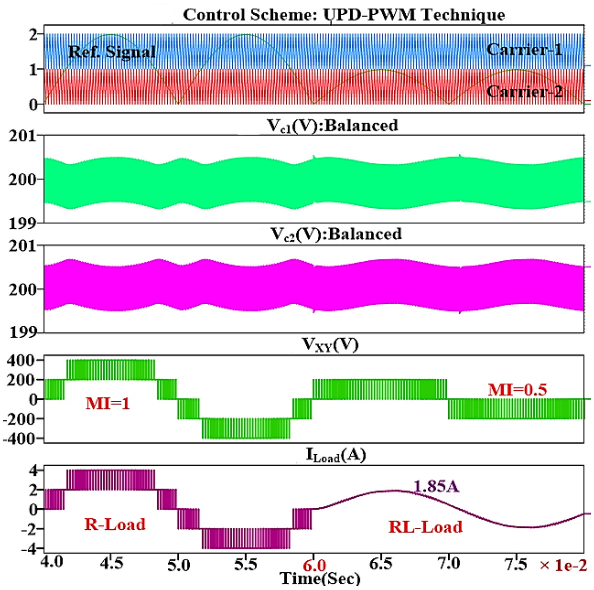

Figure 6. Results for M5L-NPC topology: standalone operation

3.2. Grid-connected operation (GCO): results

By using the Figure 5 control strategy, the GCO has been explained in this section. The respective grid-connected simulation parameters are represented in Table 3. Generally, the minimum DC-link voltage in a single-phase grid-connected system can be selected 1.2 times of peak value of V_{grid}. To explain the GCO of the proposed M5L-NPC topology, there are different transient case studies have been explained in this section.

Figure 7 represents simulation results for GCO with a step change of unity power factor (UPF) to 0.9 leading PF at t=0.08 sec. Figure 8 represents simulation results for GCO with a step change of UPF to 0.9 leading PF at t=0.08 sec. In these two cases, the injected I_{peak}=10 A is considered and for visibility of the I_{grid}

in simulation results, the outer side of the gain value=10 is multiplied by the I_{grid} component. Figure 9 represents simulation results for GCO under UPF operation with a step change of I_{peak}=5 A to 15 A.

In all cases with the utilization of the chopper control strategy, both DCL-CVs are balanced at half DC-bus voltage = 200 V. Here, the proposed chopper control strategy is universally suitable to all split DC-link-based inverter topologies. The inverter generated 5-levels with a peak value of ±400 V and of course, based on reference I_{peak}, the levels may vary. In these studies, the UPF and leading/lagging PF indicate injecting active and reactive power into the grid. All transient results with the utilization of a simple proposed current control strategy give better performance according to the reference value of I_{grid}.

Table 3. Simulation parameters-GCO

S. No	Parameter	Value	S. No	Parameter	Value
1.	Resistor-filter	0.01 Ω	6.	Grid frequency	50 Hz
2.	Inductor-filter	3.5 mH	7.	Chopper-C_1	1000 µF
3.	Switching frequency	10 kHz	8.	Chopper-C_2	1000 µF
4.	DC-link: V_{dc}	400 V	9.	Chopper-R_{dc}	0.1 Ω
5.	V_{grid} (Peak)	325 V	10.	Chopper-L_{dc}	0.01 mH

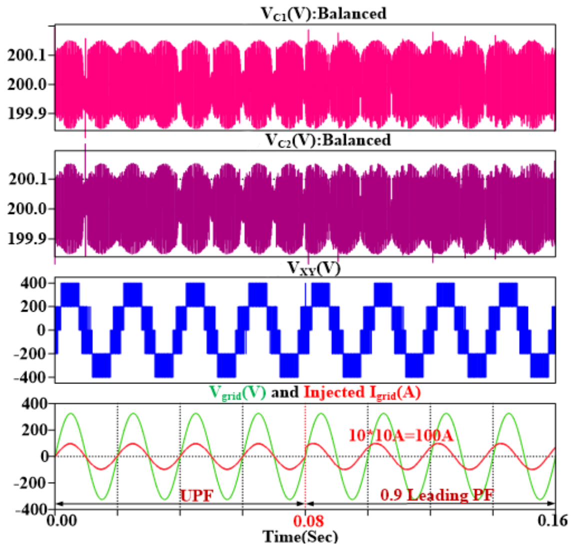

Figure 7. Results for M5L-NPC topology: GCO (UPF to 0.9 leading PF with I_{peak}=10 A)

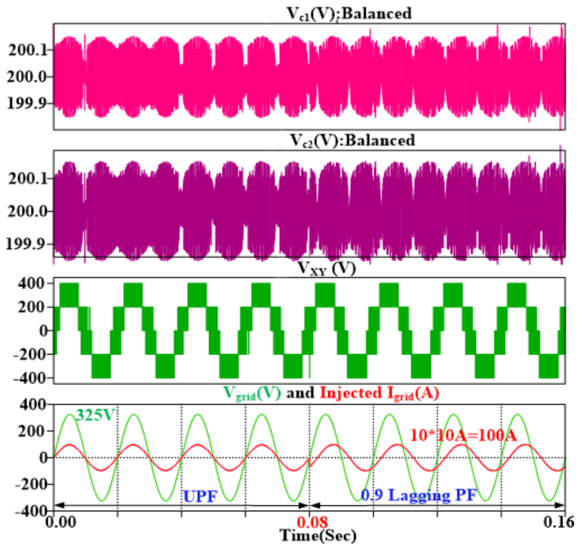

Figure 8. Results for M5L-NPC topology: GCO (UPF to 0.9 lagging PF with I_{peak}=10 A)

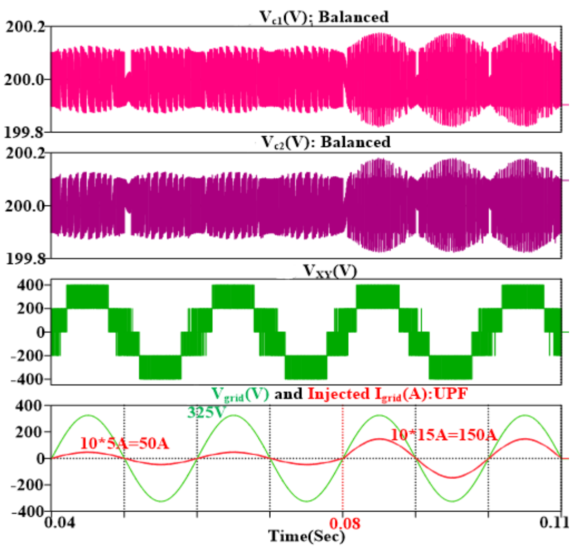

Figure 9. Results for M5L-NPC topology: GCO (UPF with step change of I_{peak}=5 A to 15 A)

Figure 10 represents the zoomed view of reference and carrier signals in GCO at UPF mode. In this, the black color represents the unipolar reference signal in closed-loop operation. Figure 11 shows the harmonic spectrum of I_{grid} at UPF operation. In this, the first band of switching frequency harmonics is placed at 10 kHz. It gives the peak value of current=9.989 A at the fundamental frequency and provides total harmonic distortion (THD) = 2.43%. It follows IEEE-1547 standards and provides good power quality on the utility side. Finally, APC, RPC, and low harmonic I_{grid} distortion objectives have been achieved successfully along with balanced DCL-CVs.

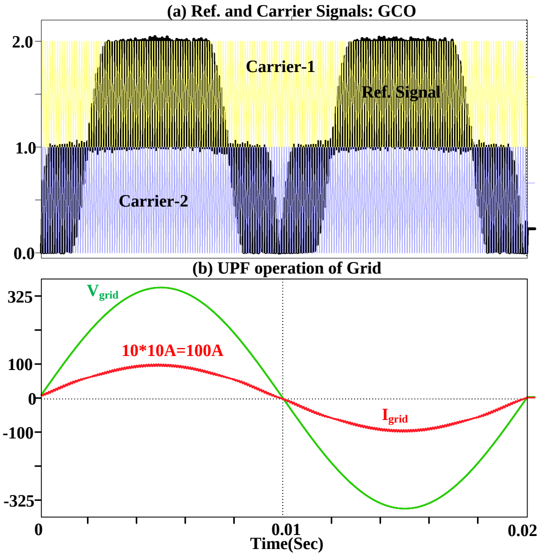

Figure 10. Zoomed view results: GCO (UPF operation with I_{peak}=10 A)

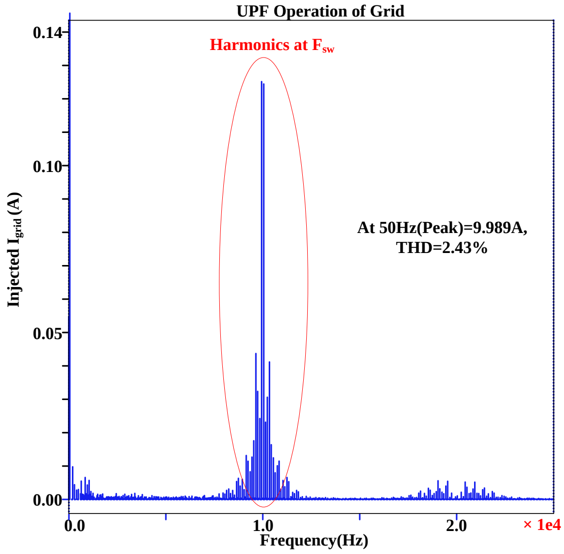

Figure 11. Harmonic spectrum of I_{grid}: GCO (UPF operation with I_{peak}=10 A)

4. COMPARATIVE STUDY

The comparative study between conventional topology and proposed modified topology is represented in Table 4. The conventional SPFT-5L-NPC Topology has 2 DC sources, while the proposed M5L-NPC topology utilizes 1 DC source. The conventional SPFT-5L-NPC operates only as a standalone system, whereas the proposed M5L-NPC supports both standalone and GCOs. The conventional SPFT-5L-NPC employs PD-PWM ($N_{carriers}$ = 4), while the proposed M5L-NPC utilizes UPD-PWM ($N_{carriers}$ = 2) for generating switching pulses.

The conventional SPFT-5L-NPC features a bidirectional switch with 4-diodes and 1-IGBT, whereas the proposed M5L-NPC uses 2-diodes and 2-IGBTs for bidirectional switching. The chopper control strategy is not explained in the conventional SPFT-5L-NPC, while the proposed M5L-NPC elaborates on its chopper control strategy, suitable for both standalone and GCOs.

Table 4. Comparative study

S. No	Conventional SPFT-5L-NPC Topology	Proposed M5L-NPC Topology
1.	Number of DC sources = 2	Number of DC sources = 1
2.	Operation: Only standalone	Operation: Both standalone and GCO
3.	PWM: PD-PWM ($N_{carriers}$ = 4)	PWM: UPD-PWM ($N_{carriers}$ = 2)
4.	Bidirectional switch: 4-Diodes and 1-IGBT	Bidirectional switch: 2-Diodes and 2-IGBT
5.	Chopper control strategy: Not explained	Chopper control strategy: Explained. It is effectively suitable for both standalone and GCO

5. CONCLUSION

In this paper, the comparative study between conventional and proposed topology has been discussed. This study explains the control of DCL-CVs as well as standalone and grid connections of the proposed M5L-NPC architecture. In both standalone and GCO, the DC-link capacitors are effectively balanced at half of the total DC-bus voltage. Of course, the suggested chopper control approach works with every split DC-link-based inverter topology. The APC, RPC, and injecting sinusoidal current with low harmonic distortion-three grid-connected key objectives have been comprehensively examined while taking a straightforward simple current control approach into account. The drawback of the proposed M5L-NPC topology is that it provides only unity gain along with the chopper circuit. To improve the gain value along with the balancing of DCL-CVs, a new study is necessary and it can be considered as a future scope of work.

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BIOGRAPHIES OF AUTHORS

Y. Sravan Kumar is a research scholar at the Department of Electrical Engineering, Osmania University. He obtained his master's and bachelor's from Jawaharlal Nehru Technological University, Hyderabad, India in 2011 and 2008 respectively. He worked as an associate professor and assistant professor for over a decade. His research interests include control systems, power electronics, and electromagnetic fields. He can be contacted at email: y.sravan16@gmail.com.

T. Murali Krishna received UG degree from the Institution of Engineers (India), Kolkata in 2001, M.Tech. in Electrical Power Systems, and Ph.D. from JNTUA, Anantapuramu, Andhra Pradesh in 2005 and 2016, respectively. He is presently working at Chaitanya Bharathi Institute of Technology as an associate professor in the Department of EEE. His research interests include power electronics, FACTS, wavelets, and renewable energy integration. He can be contacted at email: tmuralikrishna_eee@cbit.ac.in.

Yesuratnam Guduri received B.Tech. degree in Electrical and Electronics Engineering from Jawaharlal Nehru Technological University, Hyderabad, India in 1995. He received an M.Tech. degree in 1998 from Regional Engineering College, Warangal in the field of power systems. He received a Ph.D. degree from the Department of Electrical Engineering, Indian Institute of Science, Bangalore in 2007. Currently, he is working as a senior professor in the Department of Electrical Engineering, University College of Engineering, Osmania University, Hyderabad. His research interests include computer-aided power system analysis, reactive power optimization, voltage stability, and artificial intelligence applications in power systems. He can be contacted at email: ratnamgy2003@gmail.com.