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Five-level transformerless inverter with reduced voltage stress on components

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ABSTRACT

Leakage current flow is an important issue of transformerless (TL) inverters due to the absence of galvanic isolation between the source and grid sides in grid-connected solar photovoltaic (PV) systems. This article proposes a five-level (5L) TL direct ground point (DGP) type inverter employing two switched capacitors (SCs). The DGP configuration shares a common ground point for the PV negative terminal with grid neutral, thereby completely suppressing the leakage current. The employed semiconductors endure maximum voltage stress equivalent to the input voltage, while the switched capacitors (SCs) are rated at only half of the input voltage. This significantly reduces both the size and cost of the inverter. In addition, it uses reduced power components and has a lower total standing voltage per unit among the recent same art of topologies. A detailed comparison to show the merits of the proposed inverter is presented. Simulations and experiments were conducted at a 1 kW output power level in stand-alone as well as grid-connected mode to validate the feasibility of the proposed inverter.

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1. INTRODUCTION

Renewable energy generation in distributed generation offers a promising path towards a cleaner, more resilient, and sustainable energy future [1]. Multilevel inverters play a vital role in renewable energy generation by converting direct current from sources like solar into high-quality alternating current. Their ability to handle high voltages and mitigate fluctuations enhances overall power quality, making them essential for efficient and reliable integration of clean energy into the grid [2]-[4]. The integration of solar photovoltaic or PV systems with the grid using multilevel inverters (MLIs) and transformers commonly faces drawbacks, including increased size, cost, losses, and reduced efficiency. This is primarily due to the inclusion of transformers in the system [5], [6]. On the contrary, transformerless inverters are now widely favored in grid-tied photovoltaic (PV) systems, owing to their distinct advantages such as higher efficiency, generally 1-3% higher than inverters with transformers, enhanced power density, compact size, and cost-effectiveness [7]. However, in transformer-free integration, due to the absence of galvanic isolation provided by transformers, transformerless inverters generate a high-frequency common mode voltage (CMV) between the PV panels and the ground. This CMV results in a current, known as leakage current (LC), to flow through the parasitic capacitance and back to the grid [8]. This LC can contribute to harmonic distortion in the grid, requiring additional filtering measures, the risk of individuals touching the PV panels, and increased power losses [9],

[10]. Therefore, this LC current should be maintained within the limit as defined by German code standard VDE-0126-01-01 or eliminated [11]. There have been various TLIs proposed in the literature including decoupling methods (DC and AC) [12], [13], and neutral point clamped (NPC) topologies [14]-[17], to curtail the LC in grid-connected solar PV systems. However, all these topologies do not completely suppress the LC [18].

The approach known as the direct ground point or DGP type is employed in grid-connected PV systems to effectively eliminate leakage current to ~0 [19]. In this configuration, a direct and solid connection point is shared by the negative terminal of PV panels and the grid neutral [20]. Different DGP topologies have been proposed in the literature [21]-[31], and each of them has its pros and cons. Some of the drawbacks are the requirement of more power components with peak inverse voltage (PIV) higher than their output voltage, increased total standing voltage per unit ($TSV_{p.u.}$), more active switches in each voltage level, and high-voltage rating switched capacitors (SCs).

The use of common ground type (CGT) inverters in PV systems provides a notable advantage by eliminating leakage current, contributing to enhanced safety, reduced power losses, and improved efficiency. However, this advantage comes with a trade-off DGP inverters rely on at least one high-voltage capacitor and increased power components in their circuit configuration. In a study by Sandeep *et al*. [22], a DGP structure for 5L voltage generation is proposed with higher power components and 3 SCs with two different ratings. Due to their two different ratings their capacitor voltage diversity factor (C_{VD}) is very high which increases the volume and cost of the inverter. Though the topology proposed in the study by Grigoletto [23] uses only six switches, it requires two different ratings for their capacitors like Sandeep *et al*. [22]. Even though the topology [24], uses 2 SCs with a voltage rating equal to half of the input voltage, they use more power components with high $TSV_{p.u}$. The overall cost and volume of the topology proposed in research by Kumari *et al*. [25] are high due to increased power components with high $TSV_{p.u.}$ and more SCs to achieve 5L output voltage. Even though the $TSV_{p.u.}$ of the topology presented in Habib Khan *et al*. [26] is low, it comes at the cost of high C_{VD} and more power components. Like the study of Habib Khan *et al*. [26], the topology presented in Dhara *et al*. [27] also suffers from high values for C_{VD} and $TSV_{p.u.}$ which results in increased volume and cost. Even though the topologies [28] and [29], use reduced power components their PIV and C_{VD} are high. Despite having low C_{VD} and $TSV_{p.u.}$, the topologies presented in previous researches [30] and [31] use one additional switch than the topologies [28] and [29]. Considering the above discussion, this article is proposed with reduced power components with low voltage stress on switches and capacitors. The key features of the proposed 5L-DG inverter are: i) Requires only six switches and one diode; ii) Uses two self-balanced SCs with even voltage stress i.e., half of the input voltage; iii) Low $TSV_{p.u.}$ and C_{VD}; iv) Reduced charging current ripple due to soft-charging inductor; v) Minimum average number of active switches; vi) PIV is equal to the input voltage; and vii) LC is suppressed completely.

2. PROPOSED 5L INVERTER TOPOLOGY

The power circuit of the overall system integrating the solar PV system with the grid is shown in Figure 1. The input PV source is connected with the DC-DC boost converter which provides a constant DC voltage (V_{CB}) to the proposed 5L-DG inverter topology. The proposed 5L-DG inverter topology is configured using six switches (S_1-S_6), two SCs (C_1 and C_2), and one diode (D). In addition, a soft charging inductor (L_{SC}) is used in the capacitor charging path to minimize the inrush current spikes. Since capacitors are connected in parallel with the input voltage (V_{CB}) during the output voltage levels 0, 0.5 $V_{CB,}$ and V_{CB}, the series connected SCs C_1 and C_2 are charged to a voltage equal to half of the input voltage i.e., 0.5 V_{CB}. The proposed 5L-DG topology mitigates the leakage current to ~0 due to their direct ground point for the PV negative and grid neutral. Figures 2(a)-2(e) depict all five output voltage level generations along with the capacitor charging and discharging.

2.1. State 1

In this state, the positive terminal of DC-link capacitance (V_{CB}) is connected to the terminal 'y' to generate v_o=+V_{CB} as shown in Figure 2(a). To achieve this, the switches S_1 and S_2 are turned ON, while the SCs C_1 and C_2 are charged to half of the input voltage i.e., 0.5 V_{CB}. The load current path and SCs charging path are (+V_{CB})-S_1-S_2-L_f-*Grid*-(-V_{CB}) and (+V_{CB})-C_1-C_2-D-L_{SC}-(-V_{CB}).

2.2. State 2

Figure 2(b) shows the output voltage level of v_o=+0.5 V_{CB} which is obtained by switching ON the switches S_1, S_4, and S_5. Here, the load current path is (+V_{CB})-S_1-S_4-S_5-L_f-*Grid*-(-V_{CB}). Further, both the SCs are charged to half of the input voltage 0.5 V_{CB} and the respective charging path is (+V_{CB})-C_1-C_2-D-L_{SC}-(-V_{CB}).

2.3. State 3

The zero-voltage level is generated by triggering the switch S_6 and the load terminals are shorted via S_6-D-L_{SC}. At the same time the switch S_1 is turned ON to charge the SCs C_1 and C_2. In this state of operation, the charging path of SCs is (+V_{CB})-C_1-C_2-D-L_{SC}-(-V_{CB}).

2.4. State 4

The first negative voltage level generation is obtained due to the discharging of SC C_1. The voltage across the SC C_1 i.e., V_{C1} =0.5 V_{CB} is delivered to the load. The active switches during this state are S_3, S_4, and S_5 through which the terminals 'y' and 'b' are connected to generate v_o=-0.5 V_{CB} as shown in Figure 2(d).

2.5. State 5

During this state, both SCs C_1 and C_2 are discharging to achieve the output voltage level of v_o=-V_{CB}. That is, the voltage of the SCs C_1 and C_2 are added together to deliver to the load. Here the load path is via C_1-C_2-L_f-grid. As illustrated in Figure 2(e) the switches S_3 and S_6 are turned ON to connect the terminals 'y' and 'b'.

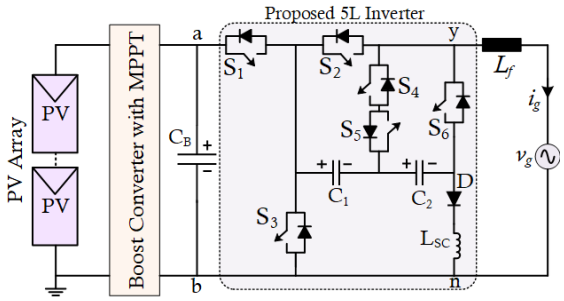

Figure 1. Circuit configuration of proposed 5L-DG inverter topology

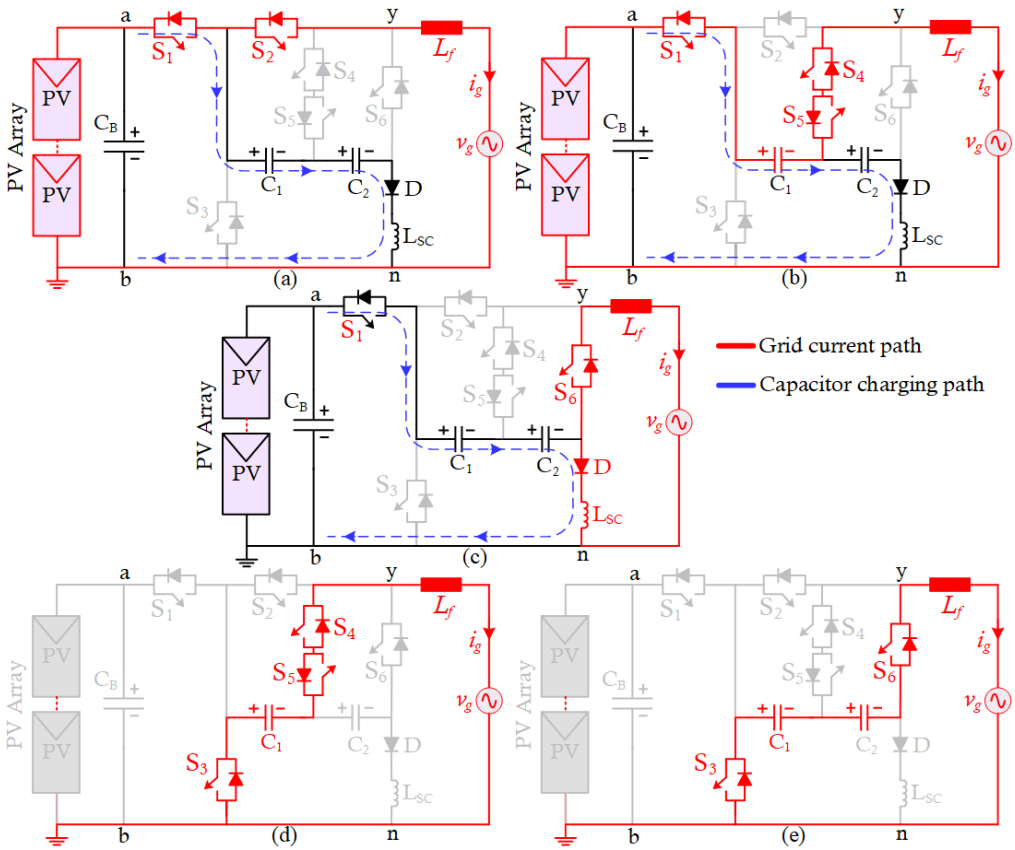

Figure 2. Output voltage level generations of proposed 5L-DG inverter: (a) v_o=+V_{dc}, (b) v_o=+0.5 V_{dc}, (c) v_o=0, (d) v_o=-0.5 V_{dc}, and (e) v_o=-V_{dc}

3. DESIGN OF CAPCITORS (C_1 AND C_2) AND FILTER INDUCTOR (L_f)

Figure 3 depicts the level-shifted pulse width modulation (LSPWM) employed and the 5L output voltage waveform (v_o) along with the capacitor ripple voltage waveform. From the switching sequence of switches given in Table 1, and the maximum discharge time (MDT) of SCs C_1 and C_2, their capacitance are calculated as (1)-(4).

$$Q_{C1} = \frac{I_{peak}}{\omega}(1 - \cos(\omega\pi)) \quad (1)$$

$$C_1 = \frac{I_{peak}}{\omega * \Delta V_{C1}}(1 - \cos(\omega\pi)) \quad (2)$$

$$Q_{C2} = \frac{I_{peak}}{\omega}(\cos(\omega t_a) - \cos\omega(\pi - t_a)) \quad (3)$$

$$C_2 = \frac{I_{peak}}{\omega * \Delta V_{C2}}(\cos(\omega t_a) - \cos\omega(\pi - t_a)) \quad (4)$$

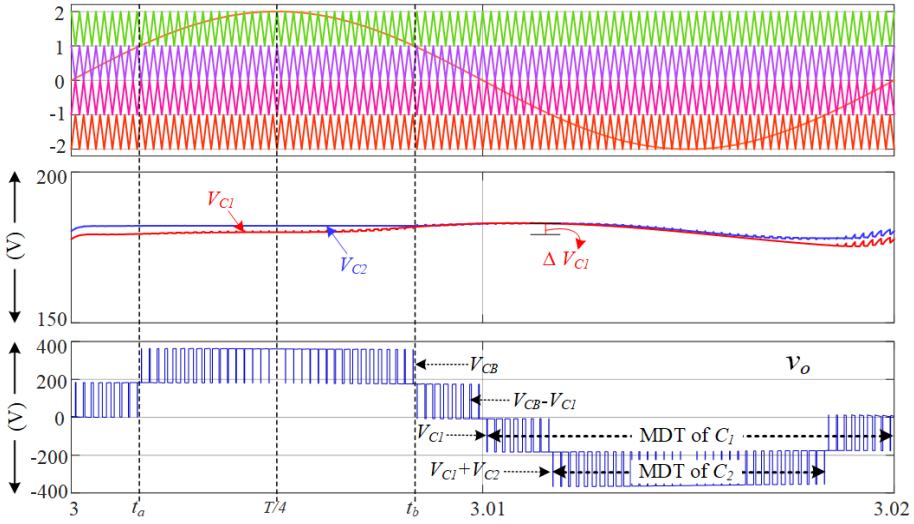

Figure 3. PWM Scheme along with 5L output voltage waveform

Table 1. Switching pattern and PIV of switch of 5L-DG inverter

State	v_o (V)	S_1	S_2	S_3	S_4	S_5	S_6	C_1	C_2
1	V_{CB}	1 / 0	1 / 0.5 V_{CB}	0 / V_{CB}	0 / 0.5 V_{CB}	0 / 0	0 / V_{CB}	Charge	Charge
2	0.5 V_{CB}	1 / 0	0 / V_{CB}	0 / V_{CB}	1 / 0	1 / 0.5 V_{CB}	0 / 0.5 V_{CB}	Charge	Charge
3	0	1 / 0	0 / V_{CB}	0 / V_{CB}	0 / 0	0 / 0.5 V_{CB}	1 / 0.5 V_{CB}	Charge	Charge
4	-0.5 V_{CB}	0 / V_{CB}	0 / V_{CB}	1 / V_{CB}	1 / 0	1 / 0.5 V_{CB}	0 / 0.5 V_{CB}	Discharge	No effect
5	-V_{CB}	0 / V_{CB}	0 / V_{CB}	1 / 0	0 / 0	0 / 0.5 V_{CB}	1 / 0.5 V_{CB}	Discharge	Discharge
PIV		V_{CB}	V_{CB}	V_{CB}	0.5 V_{CB}	0.5 V_{CB}	V_{CB}	-	

To calculate the filter inductor (L_f), the current flowing through it over a full cycle is considered as (5).

$$i_{Lf}(t) = i_{Lf}(0) + \frac{1}{L_f}\int_0^t V_{Lf}\, dt \quad (5)$$

The filter inductance value of (L_f) can be derived using (5) as (6).

$$L_f = \frac{1}{f_s * \Delta i_{Lf}}(3V_m \sin(\omega t) - V_{CB} - \frac{2V_m^2 sin^2(\omega t)}{V_{CB}}) \quad (6)$$

Considering the maximum inductor current ripple, the maximum inductance value of the inductor (L_f) is calculated as (7).

$$L_{f,max} = \frac{1}{f_s * \Delta i_{Lf}}(3V_m - V_{CB} - \frac{2V_m^2}{V_{CB}}) \quad (7)$$

4. COMPARATIVE ANALYSIS

To comprehensively demonstrate the advantages of the proposed topology, a detailed comparison with the same prior-art existing topologies is performed considering the key aspects such as number of components (power switches (S), gate drivers (G), capacitors (C), diodes (D), and soft charging inductors (L)), PIV of switches, $TSV_{p.u.}$, level to component ratio (LCR), capacitor voltage stress (V_{CS}), voltage diversity factor of capacitor (C_{VD}) cost function (CF), self-balancing (C_{SB}) ability, efficiency (η%) at 400 W as given in Table 2. Further, LCR and CF are calculated using the expression as (8) and (9).

$$LCR = \frac{5}{Number\ of\ (S+G+C+D+L)} = \frac{5}{(6+5+2+1+1)}=0.33 \quad (8)$$

$$CF = Number\ of\ (S + G + C + D + L) + (\alpha * \text{TSVp. u.})$$
$$=17.5 \text{ (for } \alpha=0.5) \text{ and } 20 \text{ (for } \alpha=1) \quad (9)$$

Table 2. Comparison with recent 5L state of art topologies

Ref	Power components						LCR	$TSV_{p.u}$	PIV	V_{CS}	C_{VD}	CF		C_{SB}	η%@ 400 W
	S	G	C	D	L	Tc						α=0.5	α=1		
[21]	6	6	2	0	0	14	0.36	8	1.5	0.5 V_{dc} (2)	1	18	22	No	97.2
[22]	8	7	3	0	0	18	0.29	6.5	1.5	0.5 V_{dc} (2), V_{dc} (1)	2	20.3	23.5	Yes	97.1
[23]	6	6	2	1	0	15	0.33	6	1	0.5 V_{dc} (1), V_{dc} (1)	1.5	18	21	No	96.2
[24]	8	8	2	1	0	19	0.26	6	1	0.5 V_{dc} (2)	1	22	25	Yes	NA
[25]	9	7	3	0	0	19	0.26	7.5	1	0.5 V_{dc} (2), V_{dc} (1)	2	22.8	26.5	Yes	NA
[26]	8	7	3	1	0	19	0.26	5	1	0.5 V_{dc} (2), V_{dc} (1)	2	21.5	24	Yes	NA
[27]	8	7	4	2	0	21	0.24	8	1.5	0.5 V_{dc} (4)	2	25	29	Yes	97.2
[28]	6	6	2	1	1	16	0.31	6	1.5	0.5 V_{dc} (1), V_{dc} (1)	1.5	19	22	Yes	96.5
[29]	6	5	3	1	0	15	0.33	5.5	1	0.5 V_{dc} (2), V_{dc} (1)	2	17.8	20.5	Yes	98.1
[30]	7	7	2	1	0	17	0.29	5	1	0.5 V_{dc} (2)	1	19.5	22	No	NA
[31]	7	7	2	0	0	16	0.31	5	1	0.5 V_{dc} (2)	1	18.5	21	Yes	97.7
[P]	6	5	2	1	1	15	0.33	5	1	0.5 V_{dc} (2)	1	17.5	20	Yes	98.9

3.1. In terms of component count T_c, LCR, and V_{CS}

The total component count T_c and LCR of the proposed topology and those in previous studies [23] and [29] are the same i.e., 15 and 0.33, which is slightly higher and lower than the topology proposed by Kadam and Shukla [21]. While comparing the Tc of the remaining topologies of Table 2 topologies, they use more components to generate a 5L output voltage waveform. A higher LCR directly corresponds to a reduced component count, and conversely, a lower LCF indicates a greater number of components. Even though the topology in study by Kadam and Shukla [21] has slightly fewer power components and higher LCR than the proposed topology, they suffer from high inrush current due to the absence of soft charging. Further, they need additional control strategies to balance their capacitor voltage. This will be reflected in the overall cost as well.

3.2. In terms of $TSV_{p.u.}$, PIV and V_{CS}

In the evaluation of TSVp.u. and PIV among various topologies, the results demonstrate the superior performance of the proposed topology. Notably, the proposed configuration surpasses alternative topologies by achieving lower TSVp.u. and PIV, even when employing a minimal number of semiconductor switches. In contrast to topologies presented by previous researchers [21], [23], [28], and [29] that share an equivalent number of switches with the proposed design, these existing topologies exhibit significantly higher TSVp.u. values. Furthermore, the PIV values for the topologies in studies [21] and [28] exceed that of the proposed topology by 50%. This confirms that the proposed topology is effective in attaining superior performance metrics while utilizing a reduced number of semiconductor switches.

3.3. In terms of CF and η%

The proposed topology exhibits the lowest CF as per (9) among all compared topologies. Additionally, the simulation efficiency of the proposed topology surpasses that of all other topologies listed in Table 2. In the context of the comparative analysis, the 5L-DG topology distinguishes itself with an efficient design characterized by minimal components, decreased TSV and PIV, a low-CF, inherent soft charging, and the absence of a pre-charge requirement. These features collectively position it as highly suitable for integration into solar PV systems with the grid.

4. RESULT AND DISCUSSION

This section presents the simulation and experimental validation of the proposed topology's performance at a 1 kW output power in both stand-alone and grid-connected modes. The validation utilizes the parameter values specified in Table 3. Figure 4 shows the simulation results during stand-alone operation for

steady state and transient operating conditions. Figures 4(a) and 4(b) illustrate the output voltage (v_o) and current (i_o) waveforms along with capacitor voltage (V_{C1} and V_{C2}) and current waveforms (i_{C1} and i_{C2}) for R=72 Ω and RL=75 Ω+j100 mH. It is observed that when the DC-link capacitor voltage is V_{CB}=360 V, the output voltage (v_o) is 360 V and load current (i_o) is 5 A for the R-load whereas the output voltage (v_o) is 360 V and load current (i_o) is 4.5 A for the RL-load. The transient response of the proposed 5L-DG inverter is shown in Figure 4(c) when the load value is changed between R=72 Ω and RL=75 Ω +j100 mH. Further, Figure 4(d) and 4(e) depict the output voltage (v_o) and current (i_o) waveforms while varying the DC-link voltage V_{CB} from 360 to 400 V, and during the modulation index (MI) change from 1.0 to 0.7.

Table 3. Comparison with recent 5L state of art topologies

Parameters	Simulation and experiment
DC-link voltage (V_{CB})	360 V to 400 V
Output voltage (v_o)	360 V to 400 V
Grid voltage (v_g)	230 V RMS
Rated power (P_o)	1 kW
SCs (C_1 & C_2)	1100 µF
Load details	50 Ω, 72 Ω, 90 Ω, 75 Ω +j100 mH, 100 Ω +j100 mH
Grid frequency (f_o)	50 Hz
Switching frequency (f_{sw})	5 kHz
Filter inductor (L_f)	7.8 mH
Soft charging inductor (L_{SC})	40 µH

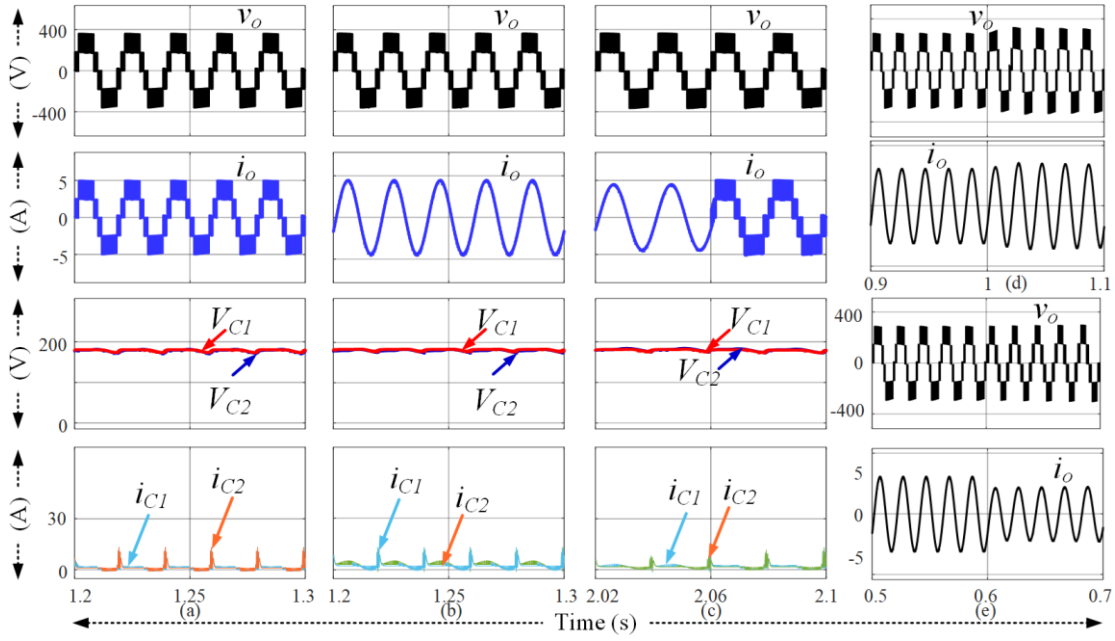

Figure 4. Simulation waveforms during stand-alone steady state and transient operating conditions: (a) load=72 Ω, (b) load=75 Ω+j100 mH, (c) load change from 75 Ω+j100 to 72 Ω, (d) variation of DC-link voltage from 360 V to 400 V, and (e) modulation index variation from 1.0 to 0.7.

The proposed 5L-DG inverter topology is controlled using a proportional-integral (PI) current controller and proportional-resonant (PR) voltage controller [22] as depicted in Figure 5. The output voltage (v_o) waveform along with grid waveforms i.e., voltage (v_g) and current (i_g) when the proposed topology is connected with the grid is shown in Figure 6. The grid current waveforms shown in Figure 6 are multiplied by a factor of 15. Figures 6(a)-6(c) depicts the output voltage (v_o) waveform along with grid waveforms v_g, i_g during the cos ϕ=1, cos ϕ=0.65 lagging, and cos ϕ=0.65 leading power factor operating conditions with the grid. Figure 6(d) illustrates the response of the proposed topology when the reference grid current ($i_{g,r}$) is altered between 2.5 A and 5 A and Figure 6(e) is the response when the reference grid current ($i_{g,r}$) is varied from 5 A to 2.5 A. These results confirm that the proposed control method works correctly to track the grid (i_g) and inject the power into the grid.

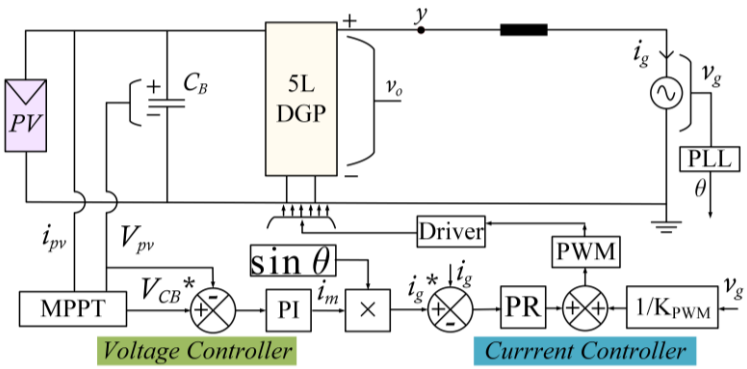

Figure 5. Control method of proposed 5L-DG inverter topology

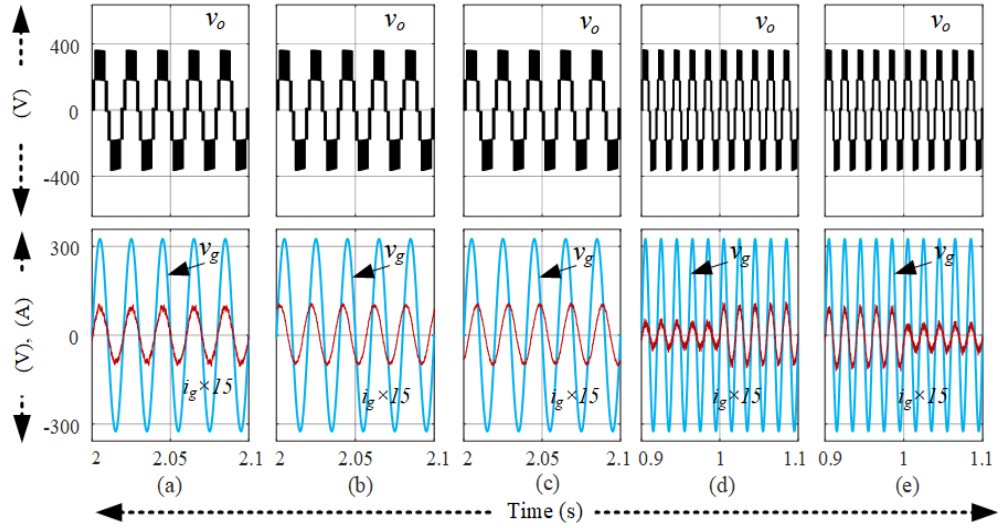

Figure 6. Simulation waveforms grid-connected mode: (a) at cos (ϕ)=1, (b) At cos (ϕ)=0.64 lead, (c) at cos (ϕ)=0.65 lag, (d) at cos (ϕ)=1 and reference current ($i_{g,r}$) is varied from 2.5 A to 5 A, and (e) vice-versa

A laboratory setup of 1 kW has been built using switches FGHL50T65LQDT, diode RUR5060, and Texam Lancu pad TMS320F2837D. The output voltage (v_o), load current (i_o), and capacitor voltages (V_{C1} and V_{C2}) during steady-state operating conditions are shown in Figure 7. Figures 7(a) and 7(b) depict the results of SCs voltages (V_{C1} and V_{C2}) which are balanced at 200 V each, when the R and RL loads are used at MI=1. Further, when the load value of RL of 50 and 100 mH is used, the waveforms of voltage and current stress of the SCs C_1 and C_2 are depicted in Figure 7(c). During the different transient operating periods i.e. MI change from 1.0 to 0.7, input change from 360 V to 400 V, and R load to RL load change, it is observed that the SCs voltages are well maintained at their rated value ~200 V as shown in Figures 7(d)-7(f). This verifies the self-balancing ability and low voltage stress of the SCs C_1 and C_2, as depicted in Figures 7(d)-7(f).

Furthermore, when the proposed 5L-DG inverter topology is operated in grid-connected mode with active power and reactive power injection to the grid, the corresponding results of inverter output voltage (v_o), grid voltage (v_g), and grid current (i_g) are shown in Figures 8(a)-8(c). The grid voltage (v_g) and grid current (i_g), when the reference grid current ($i_{g,r}$) is varied, is shown in Figure 8(c). Further, using the thermal models implemented in PLECS software with switch parameters of IKW75N60T_IGBT and IKW75N60T_Diode, the power loss distribution of semiconductor devices has been estimated as shown in Figure 9. The efficiency of the proposed topology as a function of different output powers is obtained as depicted in Figure 10. The PLECS simulation efficiency is ~98.9%, whereas it is 97.7% for the measured value at the output power of 400 W.

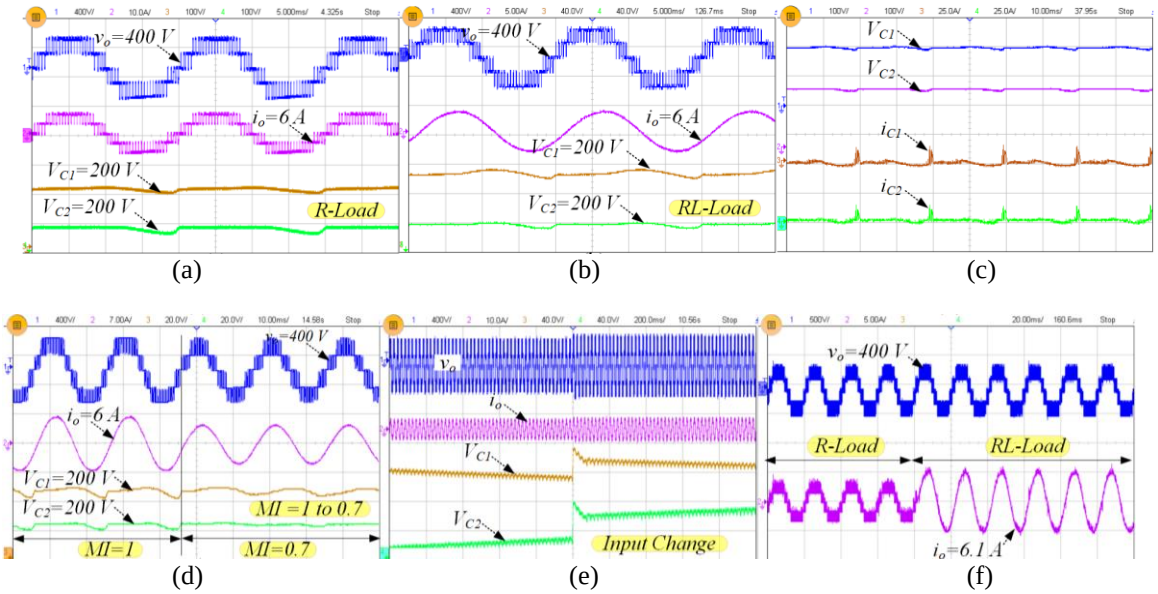

Figure 7. Steady-state response and transient response at MI=1: (a) at R load, (b) At RL Load, (c) voltage and current stress of SCs C_1 and C_2, (d) MI change from 1 to 0.7, (e) when V_{CB} is changed from 360 V to 400 V, and (f) during change of load from R=90 Ω to RL=50 Ω and 100 mH

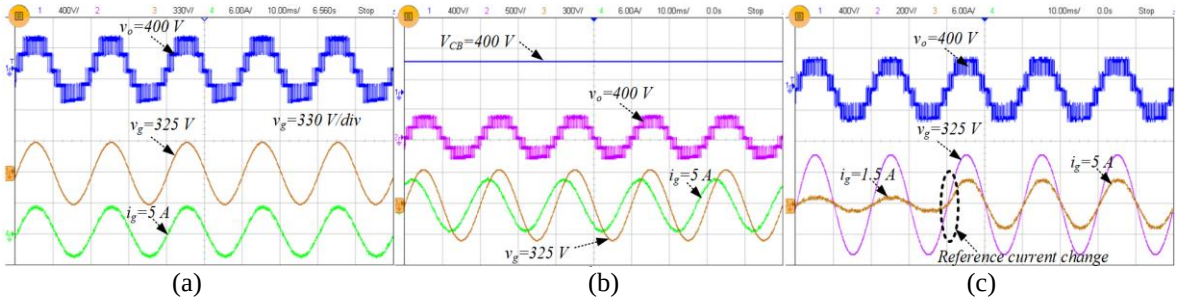

Figure 8. Results during grid-tied operation: (a) at cos (ϕ)=1, (b) At cos (ϕ)=0.64 lead, and (c) at cos (ϕ)=1 and reference current ($i_{g,r}$) is varied from 1.5 A to 5 A

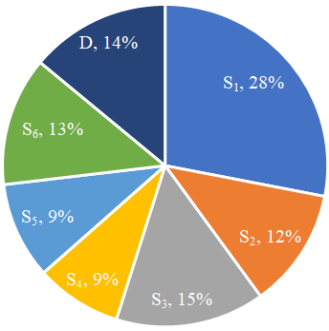

Figure 9. PLECS semiconductor loss distribution of proposed 5L-DG inverter topology

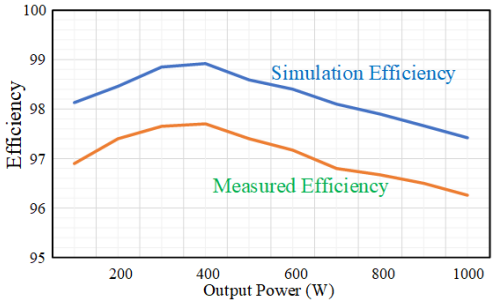

Figure 10. Simulation and measured efficiency as a function of different power output power

5. CONCLUSION

This article proposes a 5L-DG TLI topology with reduced power components and SCs with low voltage stress and leakage current elimination. The suggested inverter topology has a soft-charging inductor

that limits the peak charging current for SCs thereby minimizing transient stress and enhancing system stability. The operational principles were explained, and a detailed design of passive components was presented. The low TSVp.u., CVD, high LCR, low PIV, and reduced and even voltage stress on SCs is highlighted through a comprehensive comparison of the proposed topology with the same art of topologies. The feasibility of the proposed topology is validated using the simulations and experimental prototype for 1 kW output power in stand-alone and grid-connected modes of operation. The inverter achieves a maximum conversion efficiency of 98.95% at 400 W in the PLECS simulation tool. With the above key features, the proposed 5L-DG topology is a highly suitable candidate for a grid-connected solar PV system.

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