

A novel eight-switch nine-level modified ANPC inverter topology and its optimal modulation strategy

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ABSTRACT

An eight-switch nine-level modified ANPC inverter (8S-9L-MANPC) is designed and simulated in this paper. With this topology, only one DC voltage source and eight active semiconductor switches are required, significantly reducing system size, weight, and cost. The structure consists of a five-level ANPC inverter cascaded with a two-level leg converter. This arrangement extends the 5L-ANPC structure to a 9L configuration without requiring the use of additional capacitors. To maintain the balancing of the flying capacitor (FC), a modulation strategy using a switching state redundancy-based control method is employed. Recent 9L inverters incorporating flying capacitors and based on a hybrid structure have been compared with the proposed structure. By conducting this comparison, we can highlight the potential improvements offered by the proposed structure over the recent 9L inverters in terms of reduced component count, simplified design, and cost savings. The proposed 8S-9L-MANPC inverter is tested under various operating situations in MATLAB/Simulink simulation.

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1. INTRODUCTION

The concept of using multilevel voltage inverters was patented by researchers approximately 30 years ago [1]. Multilevel inverters (MLIs) with natural or hybrid topologies are currently well-tested choices in the medium- and high-power domains [2], in addition to the traditional applications of MLIs such as electric traction and industrial drives [3], other applications have emerged, including flexible AC transmission systems [4], high voltage direct current transmission [5], medical applications, emergency power supplies, uninterruptible power supplies [6], active filters [7], renewable energy systems [8], among others. MLIs are recognized for their superior current quality owing to lower harmonics compared to conventional inverters, they also feature good electromagnetic compatibility (EMC) behavior and reduced switch voltage stress [9]. However, this method requires the use of more power semiconductors, increased complexity of control, and voltage balancing across the capacitors [10].

Neutral point-clamped (NPC) [11], flying capacitor (FC) [12], and cascaded H-bridge (CHB) [13] are now the most common topologies of voltage source MLIs. When voltage levels rise, the NPC inverters use more clamping diodes and active semiconductor switches, resulting in higher conduction losses and reverse recovery currents that impact the switching losses of other devices [14], in CHB multilevel inverters, each module requires its individual DC voltage source, which limits the inverter's application to higher output voltage levels. Conversely, the flying capacitor (FC) inverter proves to be a suitable solution for high-level applications. However, a high number of flying capacitors (FCs) could lead to a less reliable system and a higher initial cost.

Due to these considerations, numerous researchers have turned their attention to other multilevel topologies. They propose various structures of hybrid and modular MLIs. Indeed, in recent years, hybrid inverters featuring active neutral point clamped (ANPC) topologies have seen a surge in popularity, it combines NPC and FC inverters, this topology avoids the disadvantages of conventional NPCs and has gained popularity due to its low cost, small size, and low design complexity. Recent years have seen increased interest in the 5L-ANPC inverter, which is already being used commercially for industrial applications requiring medium power levels [15], [16]. Wang *et al.* [17] proposed a new six-switch 5L-ANPC topology. Compared to conventional 5L-ANPC inverters, this structure reduces two switches and shows lower conduction loss. However, one limitation of this structure is its inability to maintain FC voltage balancing under modulation index variation. To address this challenge, researchers [18] and [19] propose a solution based on output voltage control. The inverter can control the output voltage and ensure the balance of the FC voltage even with modulation index variations. This control strategy allows for more stable and accurate voltage control, resulting in improved performance and reliability of the 5L-ANPC inverter in maintaining FC voltage balancing.

With a minimum number of power semiconductor devices, and without any diode-clamped or flying capacitors, authors in [14] propose a novel nine-level inverter. However, this structure generates nine voltage levels with only nine switches by cascading the derived T-Bridge module and the NPC structure. To reduce switching losses in power semiconductors, a novel modulation method based on multi-carrier-based sinusoidal pulse-width modulation techniques and fundamental frequency modulation is proposed. Another way to produce a nine-level is discussed in [16], involving the series connection of two five-level ANPC inverters. While this configuration offers a modular structure, it requires additional components, increasing the converter's size and cost. In the article [20], an innovative configuration is introduced featuring a nine-level modified ANPC inverter utilizing only ten switches. This design comprises two primary components: a five-level ANPC unit and a two-level converter leg with an additional AC terminal positioned at its midpoint. To maintain a tight balance in the voltage across the flying capacitor, a modulation technique based on ad-hoc switching state redundancy is utilized. This approach employs a lookup table to streamline control complexity. Another hybrid 9L inverter is proposed in [21], the paper introduces a nine-level ANPC/H-Bridge inverter tailored for high-power medium voltage motor drive applications. Two five-level ANPC half-bridges compose each phase of this inverter. Single DC-link powers all the phases. Furthermore, all five levels of the ANPC bridges operate at the fundamental frequency for the series linked or high-voltage switches, and PS-PWM is used for controlling the remaining switches.

By cascading of five-level ANPC structure and a two-level leg converter, this paper proposes a novel eight-switch nine-level modified ANPC inverter (8S-9L-MANPC). Compared to conventional ANPC topologies and recent ANPC topologies, the proposed structure uses eight active semiconductor switches instead of the conventional ANPC-based topology, thereby reducing system size, weight, and cost. The FC voltage is controlled at its reference value using a straightforward switching state redundancy-based control. Section 2 of this paper presents a brief description of the 6S-5L-ANPC inverter, which can be used as a basis for designing the proposed 9L inverter. Section 3 presents a circuit analysis of the 8S-9L-MANPC inverter, a topology description, and a modulation approach for ensuring the FC capacitor's self-balancing. In section 4, the performance of the proposed topology is tested and simulated to evaluate its effectiveness. The results obtained from these tests are presented and analyzed in detail. To demonstrate how well it can overcome some of the drawbacks of recently proposed nine-level topologies, a brief comparison analysis is discussed in the final section of the paper, and accompanying comments and conclusions are provided.

2. SIX-SWITCH FIVE-LEVEL ANPC INVERTER

The 5L-ANPC inverter proves to be a favorable option for renewable energy harvesting owing to its improved efficiency and desirable output waveform characteristics [17]. Figure 1(a) depicts the six-switch five-level ANPC (6S-5LANPC) topology. To generate a five-level output, this structure requires six active power semiconductor switches (S1-S6) and two discrete diodes (D7, D8). The outer switches (S1-S4) function at the switching frequency, whereas the inner switches (S5, S6) switch at the line frequency. Additionally, the current pathways involving S5 and S6 incorporate fast recovery diodes, permitting only unidirectional current flow. In PV grid-connection applications, ensuring that the inverter output current is in phase with the grid voltage is essential. This requirement enables the elimination of specific reactive current routes. Consequently, the 6S-5L-ANPC inverter proves to be a suitable choice for PV applications. However, this topology cannot be used under low power factor conditions. Therefore, to make the inverter more flexible, especially for loads with a low power factor, we propose the replacement of the S5 and S6 switches in the 6S-5L-ANPC topology with bidirectional switches as depicted in Figure 1(b).

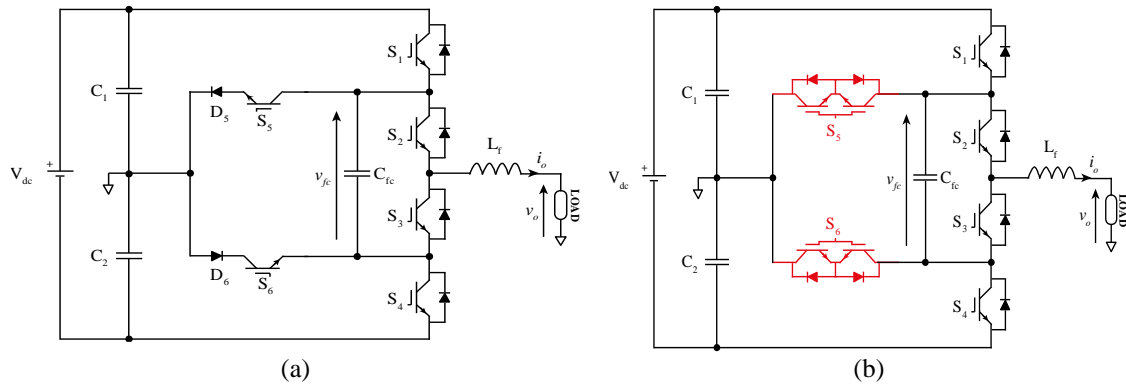


Figure 1. 5L-ANPC inverter: (a) 6S-5L-ANPC inverter and (b) the proposed 5L-ANPC

3. PROPOSED EIGHT-SWITCH NINE-LEVEL MODIFIED ANPC INVERTER (8S-9L-MANPC)

3.1. Topologies description

The structure of the proposed 8S-9L-MANPC inverter is depicted in Figure 2. It consists of the proposed 5L-ANPC inverter Figure 1(b) cascaded with a 2L leg converter. In this configuration, instead of being located at the midpoint of the DC link, the additional AC terminal is located at the midpoint of the 2L converter leg. The switches within the 2L converter leg are engineered to function at the line frequency. Indeed, employing a gate turn-off (GTO) thyristor can be a viable option for designing the switches in the 2L converter leg of the inverter. GTO thyristors are specifically designed to handle high voltages and high-power applications, making them well-suited for this purpose. They can efficiently handle low-frequency operations and provide robust switching capabilities. The proposed 5L-ANPC inverter generates five different voltage levels (0, 0.25 Vdc, 0.5 Vdc, -0.25 Vdc, -0.5 Vdc) at its output, which are based on the capacitor voltages within the inverter. To further expand the available voltage levels, an additional midpoint of the 2L Leg is introduced. This addition enables the generation of four more voltage levels (0.75 Vdc, Vdc, -0.75 Vdc, -Vdc) in addition to the existing five levels. By incorporating this midpoint of the 2L Leg, the inverter can now provide a total of nine voltage levels at its output. These additional voltage levels enhance the flexibility and control of the inverter, allowing for more precise power conversion and improved performance.

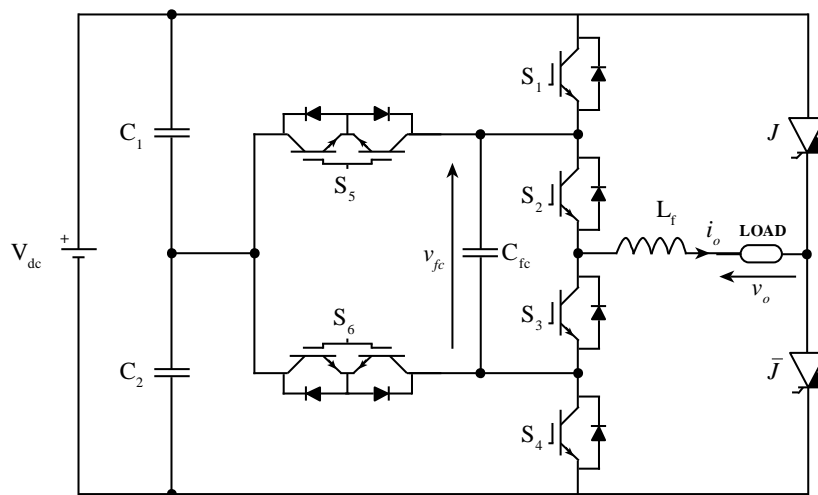


Figure 2. Scheme of the proposed inverter

3.2. Operating principles

An overview of the switching states for the proposed 8S-9L-MANPC inverter is shown in Table 1. As can be seen, there are four pairs of switching states that are redundant resulting in identical output voltage:

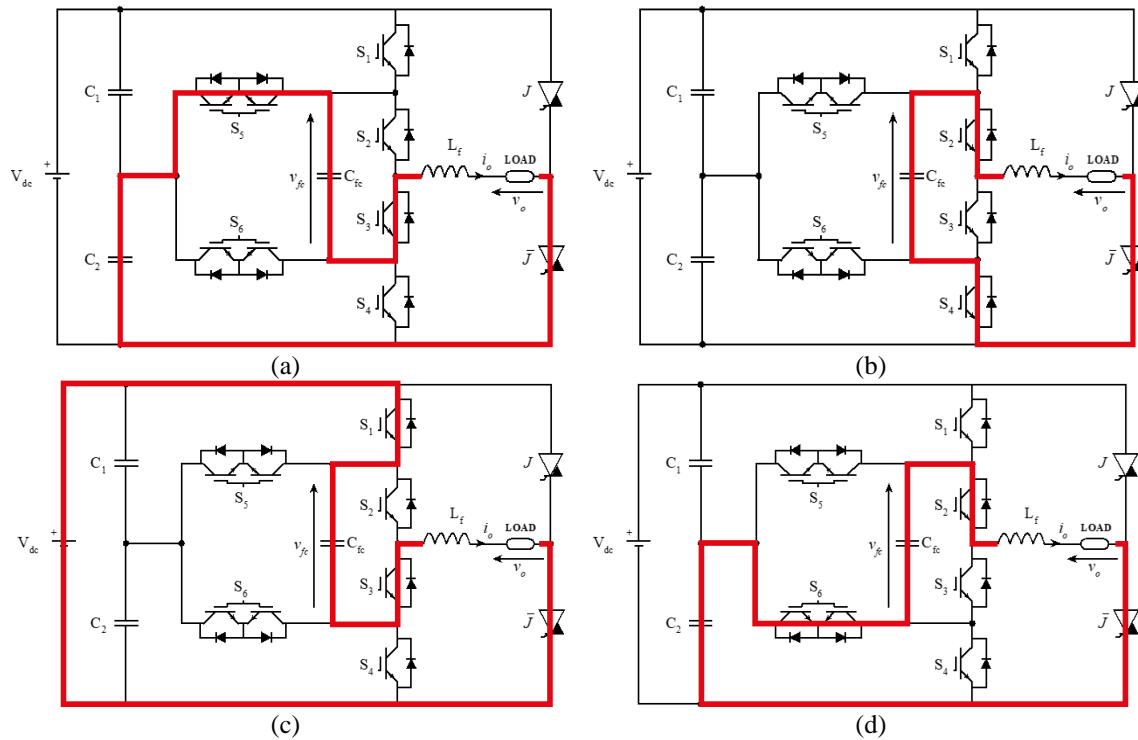
- States V_{31+} and V_{32+} that generate $3V_{dc}/4$;

- States V_{11+} and V_{12+} that generate $V_{dc}/4$;
- States V_{31-} and V_{32-} that generate $-3V_{dc}/4$;
- States V_{11-} and V_{12-} that generate $-V_{dc}/4$.

By utilizing these redundant states, it's become possible to control the flying capacitor voltage to a constant value of $V_{dc}/4$. The switching states within each pair generate opposing currents through the FC, resulting in a balanced voltage across the capacitor. Figures 3(a)-3(d) show the inverter scheme and current path for states: V_{31+} , V_{32+} , V_{11+} , and V_{12+} .

Table 1. Switching states for the proposed inverter

State	Switches states						Output voltage V_o	FC capacitor
	S1	S2	S3	S4	S5	S6		
V_{4+}	1	1	0	0	0	0	V_{dc}	--
V_{31+}	0	1	0	0	0	1	$3V_{dc}/4$	Discharging
V_{32+}	1	0	1	0	0	0	$3V_{dc}/4$	Chargin
V_{2+}	0	1	0	0	1	0	$V_{dc}/2$	--
V_{11+}	0	0	1	0	1	0	$V_{dc}/4$	Chargin
V_{12+}	0	1	0	1	0	0	$V_{dc}/4$	Discharging
V_{0+}	0	0	1	1	0	0	0	--
V_{0-}	1	1	0	0	0	0	0	--
V_{11-}	1	0	1	0	0	0	$-V_{dc}/4$	Discharging
V_{12-}	0	1	0	0	0	1	$-V_{dc}/4$	Chargin
V_{2-}	0	0	1	0	0	1	$-V_{dc}/2$	--
V_{31-}	0	0	1	0	1	0	$-3V_{dc}/4$	Discharging
V_{32-}	0	1	0	1	0	0	$-3V_{dc}/4$	Chargin
V_{4-}	0	0	1	1	0	0	$-V_{dc}$	--

Figure 3. Switching states and current path for: (a) V_{11+} , (b) V_{12+} , (c) V_{32+} , and (d) V_{31+}

3.3. Proposed 8S-9L-ANPC control scheme

Figure 4 illustrates the proposed control scheme for the 8S-9L-MANPC inverter. As depicted in the figure, the inverter control diagram comprises several vital components and elements:

- Pulse width modulator: generates the 9-level waveform by comparing a reference sinusoidal signal with eight triangle carriers with identical peak-to-peak amplitudes and frequencies. The eight signal comparison outputs are then summed together to generate the 9L staircase reference signal V_{r-anpc} .
- Level identifier: from the reference signal V_{r-anpc} , this block is able to identify the voltage level that needs to be produced, enabling the selection of the appropriate switch states for the inverter.

- Zero-band comparator: which can determine the direction of the inverter output current, the output of this comparator is designated as i_{od} . When $i_{od} = 1$, it is assumed that the load current flows out of the AC terminal ($i_o > 0$). Conversely, if $i_{od} = 0$, the load current flows into the AC supply terminal ($i_o < 0$). Detecting the direction of the output current allows the appropriate switching state to be selected for the four redundant states. This ensures the self-balancing of the FC capacitor.
- Hysteresis comparator: in this scheme, the FC voltage is controlled using a hysteresis band. This block measures the voltage across the flying capacitor to select a proper switch combination each time the FC voltage crosses any of the defined bands. When the FC voltage reaches the upper limit, H becomes “1”, and vice versa.
- Control law: The switching states depicted in Table 1 are implemented using a script. This block takes into account three factors: the desired voltage levels to be generated (V_{r-anpc}); the direction of the load current (i_{od}); and the state of the flying capacitor voltage (H). By considering these parameters, the script determines the appropriate switching states for the inverter output.

As the switching states for voltage levels V_{dc} and $V_{dc}/2$ are not redundant, the process of selecting the switching state is straightforward. However, to produce the other voltage levels, the involvement of the flying capacitor is necessary. For this, the state of the FC voltage is considered through the output current direction i_{od} and H state. For example, when the output voltage is $V_{dc}/4$, $i_{od} = 1$, and $H = 0$, this indicates that the FC capacitor is discharged and needs to be charged; in this case, the control algorithm selects the switching state V_{11+} . Similarly, when the output voltage is $V_{dc}/4$, $i_{od} = 1$, and $H = 1$, the switching state V_{12+} is selected, and the FC voltage starts to decrease, ensuring the balancing of the FC capacitor. Another pair of redundant states, V_{0+} and V_{0-} , which generate 0 V in the output voltage, is used to balance the power losses in the inverter.

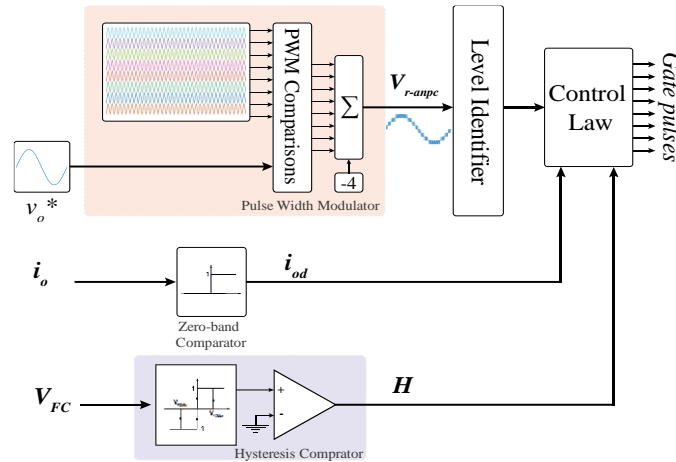


Figure 4. The proposed control scheme of 8S-9L-MANPC inverter

4. SIMULATION RESULTS AND DISCUSSIONS

Simulations of the proposed 8S-9L-MANPC inverter are conducted using MATLAB/Simulink. An overview of the parameters of the proposed inverter required for the simulations is given in Table 2. Initially, we assess the performance of the proposed multilevel system and validate the efficacy of the control strategy in maintaining voltage balance across the flying capacitor. The results are presented in Figure 5. From top to bottom, the figure shows the output voltage, the two DC link capacitor voltages, the output current, and the FC capacitor voltage. According to the results, Figure 5(a) demonstrates the capability of the new 8S-9L-MANPC inverter to generate 9L voltage waveforms, facilitated by the proposed control scheme, the voltage across the two DC link capacitors varies around $V_{dc}/2$, the choice of 2000 μF capacitors limits its voltage ripples within 2.5% Figure 5(b) and the output current of the inverter is purely sinusoidal Figure 5(c); additionally, we can observe the effect of the control strategy on achieving FC voltage balance around $V_{dc}/4$ Figure 5(d); voltage ripple can be controlled by adjusting the hysteresis band of the comparator used in the control circuit. Figure 5(e) displays the output current THD measurement, which is 2.63% Furthermore, we test the performance of the proposed inverter under index modulation variation; the aim of this test is to evaluate its robustness and ability to handle different operating conditions. Figures 6(a)-6(d) demonstrates that as the modulation index varies from 0.5 to 0.9, both the FC capacitor and the DC link capacitors maintain a balanced state, this observation confirms the efficacy of the proposed control strategy in ensuring the adaptability of the 8S-9L-MANPC inverter to modulation index variations.

Table 2. Parameters of the proposed inverter

Parameter	Value
Load resistance (Ω)	50
Load inductance (mH)	10
FC capacitance (μF)	310
Filter inductance (mH)	10
DC link voltage Vdc (V)	400
DC capacitance (μF)	2000
Switching frequency (kHz)	5
Power factor	0.5 – 0.9

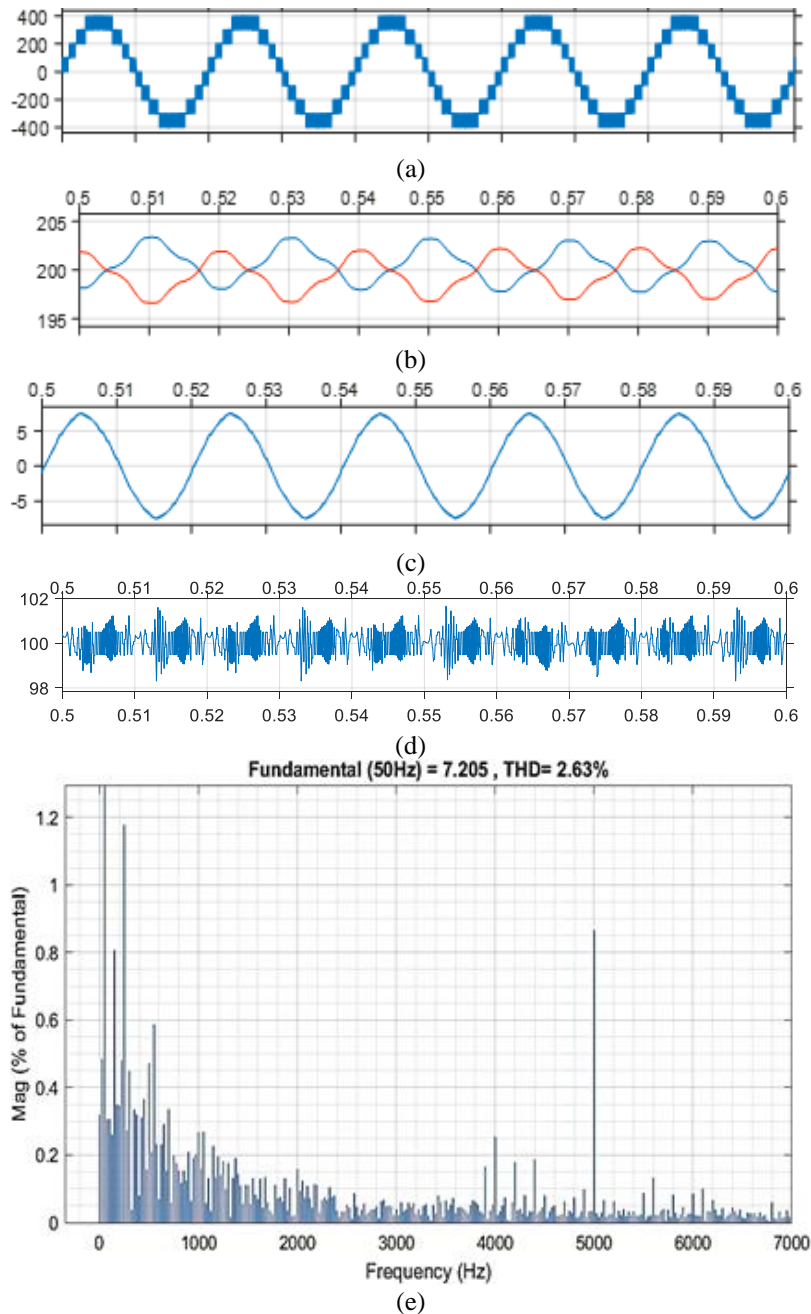


Figure 5. Simulation results of 8S-9L-MANPC inverter: (a) output voltage, (b) DC-link capacitor voltage, (c) output current, (d) FC voltage, and (e) THD of output current

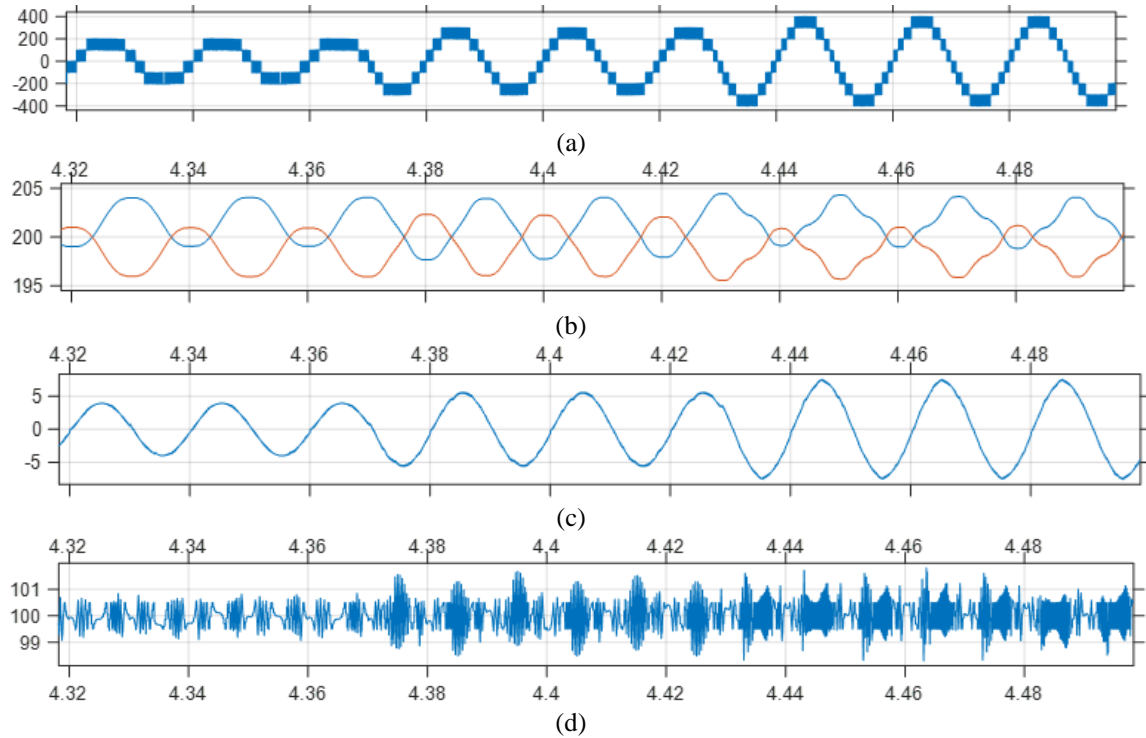


Figure 6. Simulation results under index modulation variation: (a) output voltage, (b) DC-link capacitor voltage, (c) output current, and (d) FC voltage

5. COMPARISON ANALYSIS OF THE PROPOSED CONVERTER

The proposed topology is evaluated based on a comparative study. We compare our structure to similar structures that incorporate floating/flying capacitors akin to those employed in ANPCs and/or that involve hybridizing between two topologies, similar to the approach presented in this paper. In Table 3, we summarize the key features of the proposed topology and its counterparts. The variables that are compared are number of high-frequency switches (HFS), the number of low-frequency switches (LFS), the number of flying/floating capacitors (FC), and the number of DC-link capacitors. These variables can significantly impact the overall cost of the inverter. However, increasing the number of switches and capacitors leads to higher costs due to the additional components required, such as capacitors and associated control circuitry. By selecting the 9-level structures as the basis of comparison, it can be seen from Table 3 that the proposed structure has the fewest switches and capacitors. The purpose of this comparison is to demonstrate and highlight the superiority of the proposed design in terms of reducing complexity and optimizing component requirements.

Table 3. Comparison of the 8S-9L-ANPC inverter with other recent topologies (single-phase inverter)

MLI	No. of HFSs	No. of LFSs	No. of FCs	No. of DC link cap.	Total of cap.
[16]	-	16	2	4	6
[20]	8	2	1	2	3
[22]	8	4	2	2	4
[23]	12	-	2	2	4
[24]	6	4	1	2	3
[25]	10	2	1	2	3
[26]	6	2	1	2	3
[27]	8	2	0	2	2
[28]	6	2	-	-	3
[29]	6	2	-	-	2
P	6	2	1	2	3

6. CONCLUSION

In this paper, a novel eight-switch, nine-level modified ANPC inverter (8S-9L-MANPC) is presented. The 5L-ANPC inverter and a 2L converter leg are combined to develop this topology. There is only one DC voltage source and eight active semiconductor switches required by the 8S-9L-MANPC; this decrease in the total number of parts results in a smaller overall system size, weight, and price. Additionally, using fewer components simplifies the design and manufacture of systems. The proposed structure employs a straightforward switching state redundancy-based control method to regulate the Flying Capacitor voltage. This control strategy guarantees that the FC voltage is maintained at its reference value, allowing for efficient operation and stable performance of the inverter. Simulated studies were used to evaluate the proposed control strategy, which validated its effectiveness by showcasing the system's ability to adapt and respond to changes in index modulation. The inverter demonstrated stable operation, accurate voltage regulation, and efficient power conversion across a range of index modulation variations.

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