Unlocking the potential of multilevel inverters: a comprehensive review

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ABSTRACT

The energy usage of the electricity system increased dramatically during the last few years as a result of the rise in consumers and businesses. It resulted in large-scale traditional energy generation, causing an increase in global emissions. As a result, the perforation of sources that are renewable inside electrical networks has greatly grown. Solar power systems (PS) have grown into the most prominent sources because of their tremendous potential; hence, global installed solar power capability has expanded beyond more than 635 gigawatts (GW), representing about 2% of the world's energy consumption. Multilevel inverters (MLI) are now on top of two-level inverters due to their ability to deliver diminished electromagnetic interference (EMI) and elevated capability. This study examines MLIs in terms of categorization, development, and problems, as well as practical advice for use in renewable energy systems (RES). This review also emphasizes the significance and development of an improved multilevel inverter. In summary, this study focuses on the usage of multilayer inverters in PV systems to stimulate and assist society in developing efficient, cost-effective inverters with integrated capacities of those converters described in the survey.

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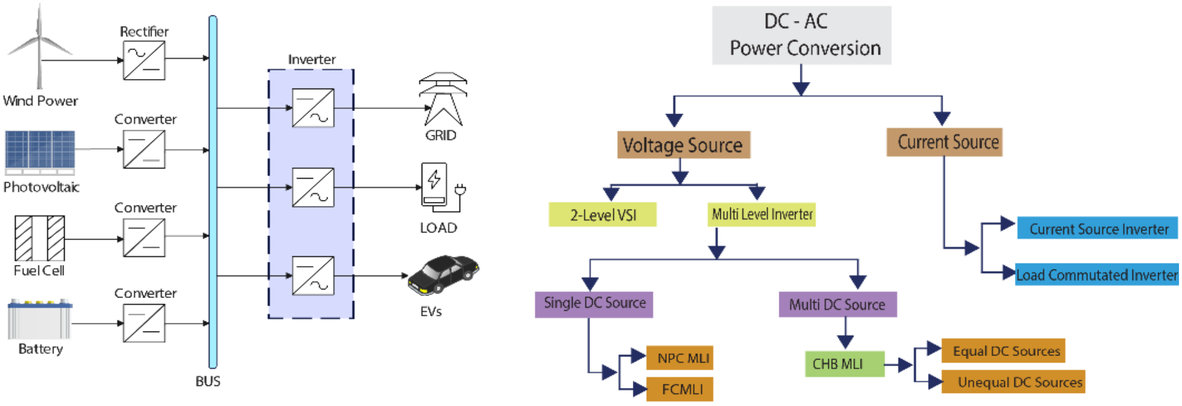
1. INTRODUCTION

Enormous high demand for power worldwide has resulted in excessive use of fossil fuels, severely impacting large emissions of polluted gas. Resulting from this, there has been a substantial focus on the advancement of sustainable energy sources, as they offer an efficient means of generating electricity while causing minimal harm to the environment [1]. Renewable energy sources (RES) include solar power, wind energy [2] geothermal energy and others. Despite availability, solar power worldwide production remains minimal [3]. Despite the substantial advances in PV systems, numerous challenges persist, notably high costs of capital, intermittency, and dependability, as well as solar technologies' moderate conversion efficiency [4]-[6].

Several research studies have been conducted on problems to enhance reliability, efficiency, and profitability [7]-[9]. Photovoltaic is used in the conversion from the sun into electrical power. The important components required for a PV system are shown in Figure 1. Nonetheless, further research is being conducted to better integrate RES into the electricity system. Due to their elevated voltage demands, inefficient operations, and elevated temperature, two-level converters were commonly utilized by low-level enterprises. Consequently, a rated capacity grid-tied solar system often incorporates multiple converters [10].



(a) (b)

Figure 1. PV components and ML topologies: (a) block diagram of PV system components and (b) machine learning types categorized by topology

Multilevel inverter (MLI) started from three levels to different levels and progressing more. Currently, MLI trends are mostly concentrating on decreasing the number of switches, drivers, quality, and making the system reliable. Hence, a pivotal focus within the realm of multilevel inverters revolves around minimizing device count while maintaining the output voltage at a consistent level. Numerous innovative technologies surfaced in recent times, intending to decrease components within multilevel inverters [11]-[14]. The reduction in devices within MLI achieves harmonics mitigation in the output voltage pattern through the adjustment of the level, thereby necessitating fewer required related components [15]-[20]. These innovative topologies facilitate efficient device utilization and streamline whole system configuration when compared to traditional approaches. Recent research has introduced several such topologies aimed at diminishing device counts within multilevel inverters, and the forthcoming sections delve into contemporary studies illuminating current trends in the multilevel inverter era.

Siddique *et al.* [21] introduced an innovative single-phase configuration characterized by a decreased number of devices and DC sources for accomplishing a greater voltage level. Furthermore, they put forward three distinct algorithms tailored for a cascaded connection. They successfully generated an impressive 71 voltage levels at the output. Bana *et al.*, as per their work [22], conducted an extensive study on reduced device count multilevel inverters (RDC MLI) and the latest configurations pertinent to RE systems and applications related to drives. In an independent investigation, Kanaujia and Kumar [23] introduced a specialized topology for open-end winding induction motor (OEWIM) drive applications. This inventive design integrated a hybrid flying capacitor (FC) setup that supported one terminal of the OEWIM, while the other terminal incorporated a three-level-cascaded H-bridge inverter. This configuration employed a three-level FC cascaded arrangement to establish a capacitor-fed H-bridge. Furthermore, a pragmatic solution for a nine-level active neutral point clamped switched capacitor MLI with enhanced capacitor charging current management was outlined by Pal *et al.* [24]. Elias *et al.* [25] suggested a hybrid MLI that relies on a series connection of half-bridge and full-bridge configuration components to produce multiple voltage levels coupled with a T-type inverter. This configuration successfully produced 11 levels, although it involved a higher component count, which raised concerns about economic feasibility.

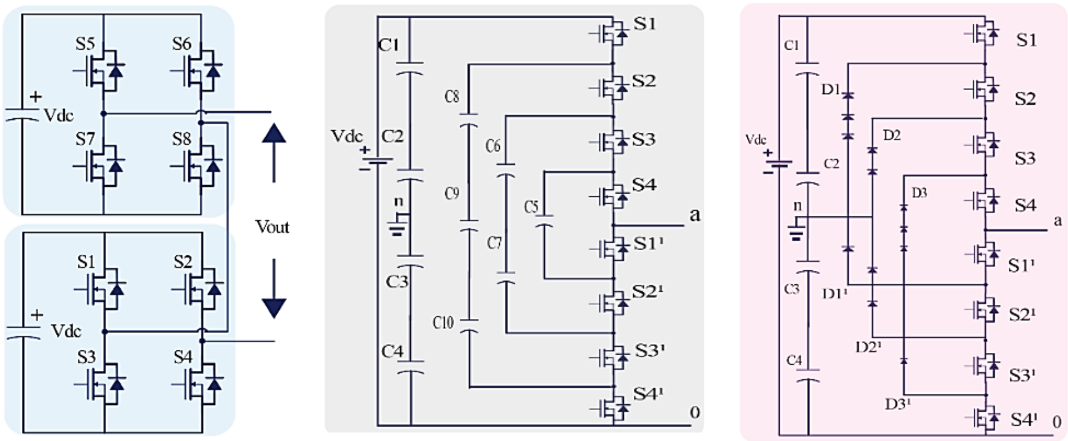
Numerous review articles have also explored the realm of multilevel inverters. Gupta *et al.* [26] provided a thorough analysis of RDC MLIs, emphasizing their quantitative and qualitative attributes. Single DC sourced MLI (SDCS MLI), known for efficiency and compactness, was discussed in detail. Singh *et al.* [27] conducted a review specifically focused on transformer-oriented SDCS MLI. Furthermore, several studies have delved into the applications of multilevel inverters in diverse fields [28]-[31]. Notably, Latran and Teke [32] scrutinized papers relating to grid-tied inverters, while Kala and Arora [33] performed a comprehensive review concerning hybrid MLI tailored for grid-tied usages. The comprehensive analysis consolidates a wealth of information on multilevel inverters, offering valuable insights into their various applications and configurations. Different MPPT controllers were discussed in the literature. They rely on a variety of factors, including tracking methodologies, modernism, and sensor implementation. MPPT approaches are broadly classed as standard, advanced, and hybrid. These standard approaches are typically easy, but they cannot distinguish between local and global peaks during PS, which is one of the root causes of poor efficacy. Because of their improved efficiency, they necessitate enhanced tracking systems. Due to the multiple constraints connected with the employment of conventional and modern techniques alone, studies have recommended hybrid approaches with a mix of both to address the issues. By, selecting the optimum MPPT approach remains a challenge. As a result, additional Exploratory investigations are underway in the field of MPPT approaches to develop a model, improved with less cost, installation, efficiency, and adaptation to diverse PV systems.

This article is structured as follows: i) Section 2 says about the classification in MLIs, along with an explanation of their design and operational principles, as well as a comparison of their advantages and drawbacks; ii) Section 3 analyzes an enhanced version of MLI, offering a rationale for its preference over alternatives; iii) Section 4 provides a summary of MLIs implemented in renewable energy setups; iv) Moving to Section 5, attention shifts to solar energy setups and their characteristics, followed by an in-depth depiction of employed MPPT techniques; v) Section 6 also delves into the application of multilayer inverters in photovoltaic systems; and vi) Section 7 addresses the challenges encountered in the study and potential areas for future exploration, culminating in a summary of the findings.

2. MULTILEVEL INVERTER (MLIS)

The term “Multilevel” refers to the development of multiple levels in output voltages, which serves to reduce the need for filtering components, minimize electrical strain on the switching devices caused by voltage, and thus improve the overall harmonic profile. Three categories of multilevel inverters exist, and different types were shown in Figure 2: i) cascaded H-bridge MLI, ii) flying capacitor MLI, and iii) diode-clamped MLI.

Among types, a cascaded multilevel inverter is often preferred due to its simplicity in design and operational adaptability. Achieving multiple levels can be accomplished in two ways. One approach involves increasing the count of DC inputs, switches; the latter approach involves a reduced switching device topology by using appropriate pulse width modulation (PWM) techniques. Many multilayer converter topologies were created as a result. A multilayer converter delivers large power ratings while simultaneously allowing the use of RES. The emergence of the three-level converter resulted in the word “multilevel”. Over the past few years, several MLI topologies have been presented. Moreover, the literature has documented three significant MLI architectures. Additionally, several modulation schemes have evolved to enhance their performance.



(a) (b) (c)

Figure 2. 5-levels topology for (a) CHB MLI, (b) FCMLI topology, and (c) DC MLI

2.1. Cascaded H-bridge MLI (CHB MLI)

A notable benefit of this multilevel topology arrangement is its reduced component count in comparison to DC and FC inverters. This results in decreased expenses and a lighter inverter weight. The circuit topology of a 5-level circuit is shown in Figure 2(a). If ‘m’ denotes the number of devices in 1ϕ symmetrical CHB, and n denotes the output level, and Vo denotes the voltage at the output, can be calculated by (1) and (2) respectively. Similarly, levels in an asymmetrical CHB are determined through binary, trinary factors. The (3) outlines levels, and (4) states peak voltage for binary operation. Similarly, (5) and (6) express the output voltage for trinary operation. For the binary factor of 2 in the GP, determining the number of voltage levels at the CHB multilevel output is achieved via (3), where ‘n’ signifies the levels and ‘m’ signifies the sources. For a symmetrical CHB, there are (1) and (2).

$$n = (2 \times m) + 1 \quad (1)$$

$$V_0 = m \times V_{dc} \quad (2)$$

For asymmetrical CHB, the equations are (3) and (4).

$$n = 2^{m+1} - 1 \quad (3)$$

$$V_0 = (2^m - 1) \times V_{dc} \quad (4)$$

For ternary CHB, the equations are (5) and (6).

$$n = 3^m \quad (5)$$

$$V_0 = \frac{(3^m - 1)V_{dc}}{2} \quad (6)$$

$$S = 2 \times (k - 1) \quad (7)$$

As the number of sources increases, the number of levels rises exponentially, with the symmetric configuration showing the slowest growth. The asymmetric (binary) configuration exhibits a more rapid increase in the number of levels compared to the symmetric configuration. The asymmetric (trinary) configuration shows the steepest growth, achieving the highest number of levels for each number of sources. This indicates that asymmetric configurations, especially the trinary one, significantly enhance the number of levels compared to the symmetric configuration, highlighting their potential for applications requiring a higher resolution of levels.

2.2. Flying capacitor MLI (FC MLI)

The primary advantage of this architecture lies in its utilization of multiple capacitors, despite potentially elevating manufacturing complexity and costs. Nevertheless, a notable drawback involves the intricate control of reactive and active power. In a single-phase FC MLI with 'n' levels, the count of needed switching components, equilibrating capacitors (C_b), and DC link capacitors is determined utilizing (8)-(10). The circuit diagram is shown in Figure 2(b) for the FC MLI of 5 levels.

This inverter lessens fluctuations within the output voltage pattern, thus eliminating the need for a filter. Moreover, these converters could take both powers of active and reactive powers. Moreover, the cost of FC MLI rises with greater levels due to heightened capacitor prerequisites.

$$S = 2 \times (N - 1) \quad (8)$$

$$C_b = \frac{(n-1)(n-2)}{2} \quad (9)$$

$$C_{dc} = (n - 1) \quad (10)$$

2.3. Diode clamped MLI (DC MLI)

In 1981, Nabae *et al.* [34] diode-clamped type MLI boasts minimal leakage current, heightened efficiency, and straightforward construction. It incorporates switching components, diodes, and capacitors. Figure 2(c) illustrates a 5-level DC-MLI. For an n-level, the switch components S, link capacitors (C_{dc}), and clamping diodes (C_d) were represented in (11), (12), and (13), respectively. The capacitor voltage is uniform and follows (14). This type of MLI necessitates high clamping diodes with the rise in levels. The voltage on the line encompasses $2(n-1)$ tiers.

$$S = 2 \times (n - 1) \quad (11)$$

$$C_d = (n - 1) \times (n - 2) \quad (12)$$

$$C_{dc} = (n - 1) \quad (13)$$

$$V_c = \frac{V_{dc}}{n-1} \quad (14)$$

To achieve a positive V_{out} in the diode capacitor multilevel inverter (DCMLI), switches S_1, S_2 are activated, whereas polarity V_{out} is achieved by activating switches S_3 and S_4. To generate a zero level S_1 and S_3 or S_2 and S_4 were switched on. DCMLI offers greater versatility in voltage synthesis compared to the flying clamped multilevel inverter (FCMLI). In cases where a challenge with voltage balance is tackled through selecting the appropriate switching combination [35]. One of the advantages of the FCMLI topology is the utilization of multiple capacitors, although it can augment the intricacy and expenses associated with manufacturing. The comparative analysis of traditional topologies is presented in Tables 1 and 2, with 'n' representing the inverter level count. A comparison of component requirements for five-level topologies is depicted in Figure 3.

Table 1. Pros and cons of classical MLI

Type	Pros	Cons
DC-MLI	• Capacitors have the potential to be pre-charged collectively. • The control approach is straightforward. • Requires fewer DC sources. • Applicable in fault-tolerant scenarios.	• The balancing circuit's complexity. • The uneven distribution between inner and outer switches. • With each increment in levels, the count of clamping diodes expands.
FC-MLI	• Reduces the number of DC sources necessary. • There is no requirement for harmonic reduction filters.	• The voltage balancing circuit's complexity. • For high levels, multiple capacitors are required. • For genuine power transfer, high losses and switching frequency are required. • Expensive installation.
CHB-MLI	• Structure is modular and straightforward. • Asymmetric source configurations are possible. • It is possible to accomplish this as a single DC source configuration.	• There are fewer output voltage levels. • More gate driver circuits are required. • To boost the output voltage, numerous DC sources are required.

Table 2. Comparative table of conventional MLIs

Sr. No.	Implementation factors	CHB	NPC	FC
1	Switches	$2(n-1)$	$2(n-1)$	$2(n-1)$
2	Input source	2	1	1
3	Voltage level	(Symmetrical) $n-1$ (Binary) $n=(2\times m)+1$ (Trinary) $n=2^{(m+1)}-1$	$2(n-1)$	$2(n-1)$
4	Diode	0	$(n-1)(n-2)$	0
5	Capacitors	$\frac{n-1}{2}$	$(n-1)$	$(n-1)$
6	FD	$(n-1)^2$	$(n-1)^2$	$(n-1)^2$
7	Balancing capacitor	0	0	$\frac{(n-1)(n-2)}{2}$
8	Carrier waves	$(n-1)$	$(n-1)$	$(n-1)$

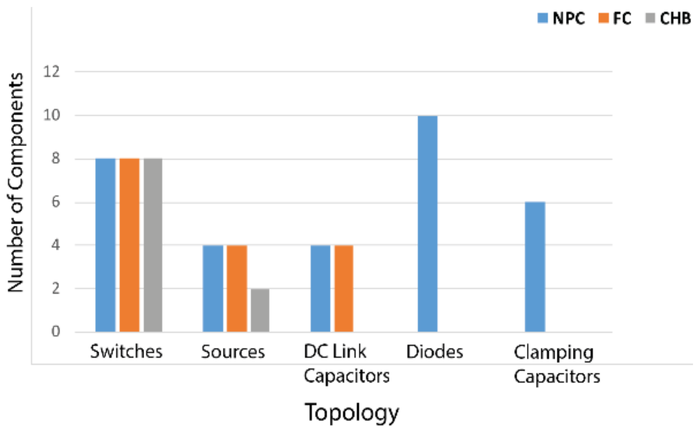


Figure 3. Component chart for conventional MLIs

3. MODIFIED MULTILEVEL INVERTERS

A modified multilevel inverter was devised through the modification of MLI configurations with fewer power devices. The advantages of these systems include cost effectiveness, a decreased count of components, and reduced space requirements as a result of the lower number of switched MLIs. Multilevel inverters with fewer devices effectively eliminated harmonics by adjusting the level count using fewer device components [36]-[38] other and related elements. These configurations demand DC sources in single or multiple forms in order to generate multilevel voltage. This encompasses both symmetric and asymmetric setups. For symmetric topology, sources possess identical magnitudes, while the latter one exhibits varying magnitudes. In practice, discrepancies in DC source magnitudes within symmetric topologies can arise due to shading impacts on PV panels or divergent battery charge states. Battery balancing systems effectively address these challenges. Numerous recently devised configurations employing fewer components were classified and shown in Figure 4, which provides an encompassing overview of the most recent developments in these topologies.

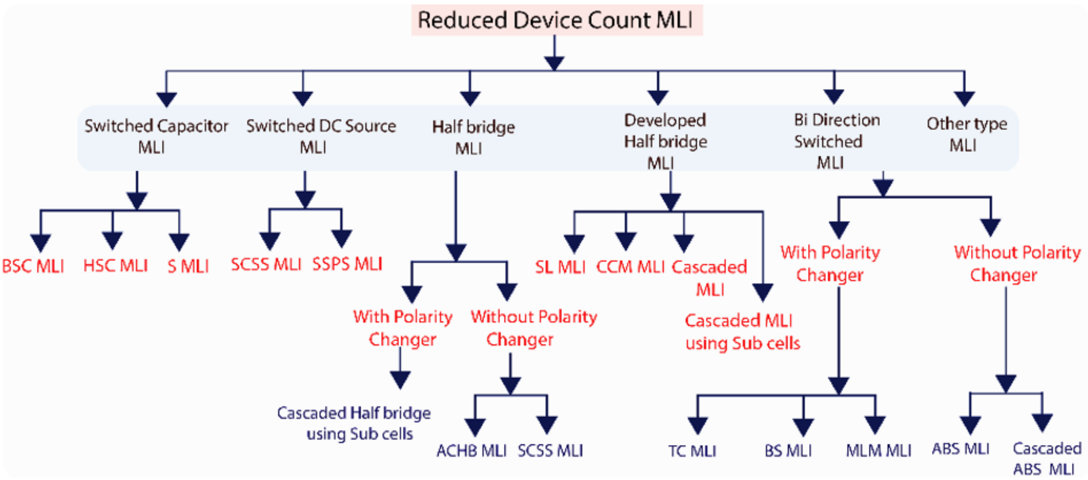


Figure 4. Modified MLI types

3.1. Cascaded type bridge MLI (CHB-MLI)

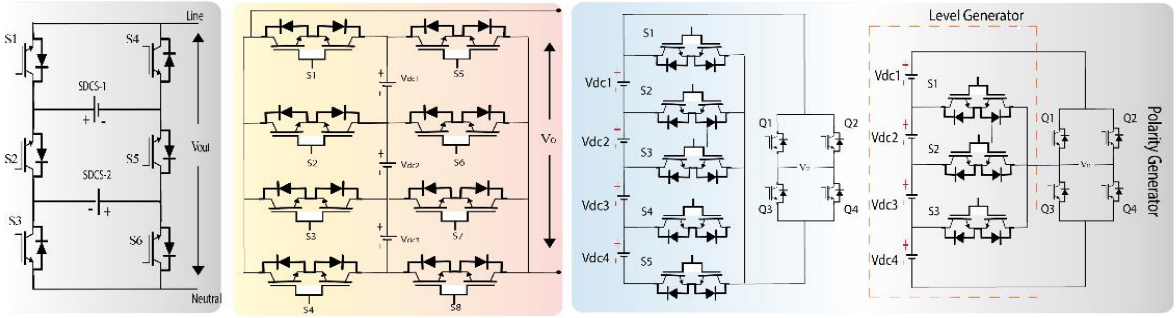
Considering these factors, this topology was chosen due to fewer device requirements compared with other MLI designs. To achieve 5-level output for 1-ø utilization, a modification was made to the design of cascade MLI, resulting in fewer switching components compared to the traditional design, which typically requires eight switches. This is illustrated in Figure 5.

Additionally, the system is complemented by the inclusion of filters at the end, which further reduces total harmonic distortion (THD). In this particular scenario, [39] 5-level topology is selected due to its reduced circuit structure and lower total harmonic distortion. The overall topologies of MLI are illustrated in Figure 5(a) represents the modified version implemented in this study. MLIs are known for their modularity and ease of design. The multilevel architecture offers the advantage of distributing the stress evenly across individual components, enabling increased voltages without necessitating high-rated devices. Therefore, MLIs' potential has to be utilized in 10 kV-rated DC-link voltage inverters. Additionally, in that context has been a noteworthy reduction in incurring switching losses. Furthermore, a five-level inverter can reduce overall rated load losses by 60%. Moreover, employing to increase the quantity of inverter level results in reducing output (THD), thereby enhancing signal quality [39].

3.2. Bidirectional switch multilevel inverter

This configuration was established either with or without [40] polarity changer. A polarity changer equipped configuration employs both bidirectional and unidirectional switching components. Conversely, the polarity changer topology exclusively utilizes bidirectional Switches. This type of MLI was discussed in [41]. It consists of 4 bidirectional switches and a DC source producing 3 3-step quasi waveforms. An increment in the DC source level of output can be elevated. The 13-level asymmetrical bidirectional switch MLI is shown in Figure 5(b) [42]. Ebrahimi *et al.* [43] introduced a configuration type multilevel module (MLM), Figure 5(c) using bidirectional switches and DC sources to produce positive polarity. An H-bridge polarity generator produces alternating polarity.

In topology studied in are transistor clamped MLI which combines both bidirectional and unidirectional. Where bidirectional (S_1, S_2, S_3) produce levels while unidirectional devices (Q_1, Q_2, Q_3, Q_4) handle polarity. Fewer devices are needed in this type. Figure 5(d) depicts a TC multilevel; the connection of insulated gate bipolar transistors defines it as such. Unidirectional transistors (Q_1, Q_2, Q_3, Q_4) act as a polarity changer.



(a) (b) (c) (d)

Figure 5. The illustration of (a) 5-level topology CHB conversion circuit, (b) asymmetric bidirectional switch MLI, (c) multilevel module multilevel inverter, and (d) 5-level TC MLI

3.3. Switched sources type MLI

The switched capacitor configurations yield a greater number of output voltage stages utilizing numerous capacitors and switching components, albeit necessitating fewer symmetrical and asymmetrical DC sources. This Topology was introduced by Gupta and Jain [44] in a series-connected form of switch sources in also known as the series connected switched source (SCSS). It negates the necessity of a two-level full-bridge VSI to reverse polarity. The foundational module comprises a solitary DC input and 2 unidirectional switches in Figure 6(a) illustrates this setup. Figure 6(b) introduced an innovative switched-series-parallel-sources (SSPS) topology that includes an H bridge; the incorporation of an LC filter in this topology further minimizes harmonic distortion. The SCSS configuration of 5 levels necessitates 6 switches, while a classical type CHB needs 8 devices. Consequently, SCSS topology achieves output voltage synthesis with fewer components compared to CHB.

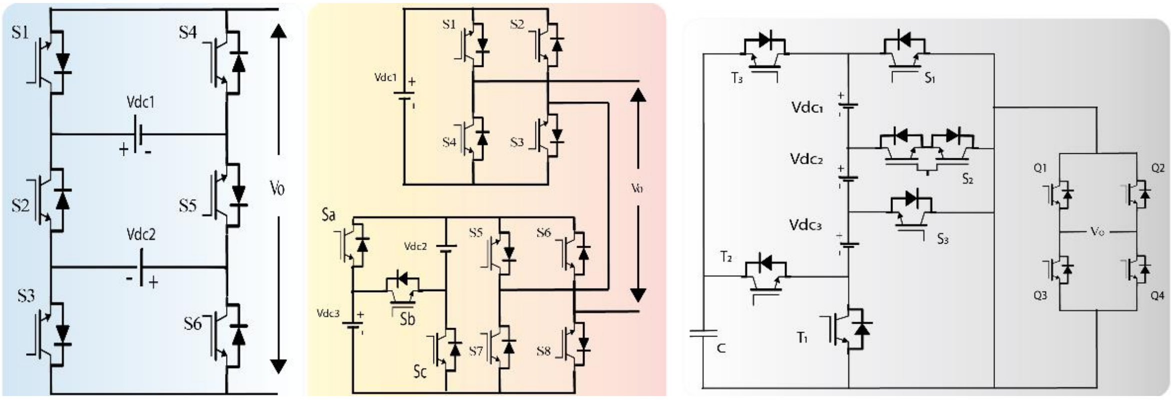
The hybrid-switched capacitor multilevel inverter (HSCMLI) features switched capacitors, as illustrated in Figure 6(c). HSCMLI integrates a switched capacitor module, a bidirectional switched MLI, and an H-bridge. This configuration facilitates bidirectional power transmission, making it highly suitable for applications like motor drives, especially in regenerative braking scenarios. To streamline the SCMLI structure further, certain active switches are substituted with diodes, particularly in applications like grid tie inverters for RE facilities.

Foti *et al.* [45] presented a novel double T-type 13-level inverter topology, which sets itself apart by requiring fewer components compared to conventional multilevel inverter types and 13-level inverters with reduced switch counts. Notably, this topology eliminates the need for additional circuits. Utilizing the nearest level modulation technique, this innovative configuration demonstrates excellent performance and confirms its effectiveness, validating its practical utility in various applications.

Kubendran and Shuhaib [46] introduce a double capacitor double diode double switch (DCDDDS) Figure 7(a) MLI designed to generate both positive and negative voltage utilizing a polarity changing circuit. They explore various algorithms for the determination of magnitude sources, allowing for increased levels with fewer switching devices. This circuit eliminates the requirement for additional power switches and has been validated through real-time testing and simulation.

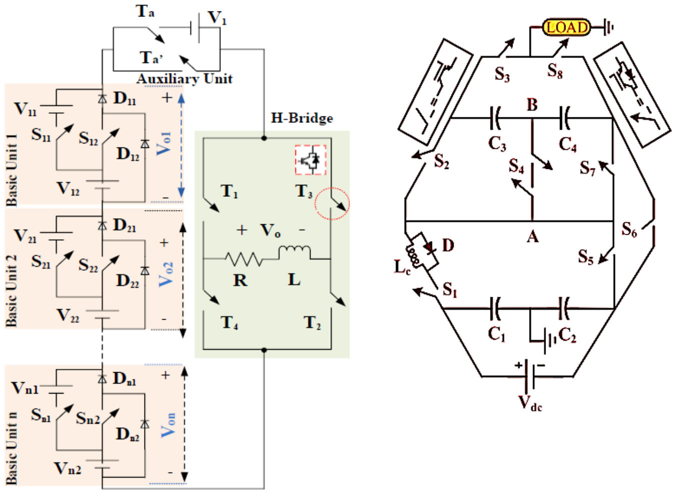
Marangalu *et al.* [47] proposed a system integrating a modified switched-capacitor (SC) based MLI with a DC-DC flyback converter; this configuration enables the fine-tuning of DC-link capacitor voltages, ensuring their alignment at the same levels. This design effectively resolves a prominent concern linked with switched capacitors, which is the occurrence of inrush currents during capacitor charging. It achieves this by including a circuit module consisting of an inductor and a parallel power diode in the path of capacitive charging current.

Islam *et al.* [48] propose a 7-level switched-capacitor-based multilevel inverter (SC-MLI), Figure 7(b) to overcome the limitations of existing topologies. The proposed converter reduces the voltage stresses on switches and the overall switch count, making it suitable for high-power applications. It also includes a soft switching circuit to reduce spikes. This topology eliminates the need for an auxiliary diode and further reduces losses. Deepak Singh [49] presents a multisource multilevel inverter (MSMLI) tailored for HFAC applications. This achieves a remarkable reduction in the devices, resulting in reduced filtering requirements. The topology comprises a switched-capacitor (SC) frontend DC-DC converter and a polarity generator, ensuring self-balancing voltage across SC. Two modulation methods are utilized for waveform generation, and the proposed topology exhibits independence from load power factor (PF) and modulation method, validated through PLECS simulation and thermal analysis. Refer to Tables 3 and 4 for comparative analysis of SC based MLIs as shown in Figure 8 [50]-[58].



(a) (b) (c)

Figure 6. Reduced MLI topologies: (a) five-level SCSS MLI, (b) SSPS DC source MLI, and (c) hybrid switched capacitor MLI



(a) (b)

Figure 7. Multilevel inverter topologies: (a) DCDDDS multilevel inverter and (b) 7-level SC-MLI

Table 3. Comparative analysis of SC-based inverter topologies

Reference	Source	Level	Switch	Diode	Capacitor	THD
[50]	1	9	11	1	2	1.44
[51]	4	15	15	6	3	4.1
[52]	1	13	13	13	5	2.5
[53]	4	17	16	0	4	4
[54]	1	13	15	0	3	9.7
[55]	1	13	13	3	4	9.2
[56]	1	17	16	2	4	6.96
[57]	2	13	12	3	3	5.39
[58]	2	17	12	3	4	3

Table 4. Comparison of the symmetric SDMLI topologies

Parameter	[58]	[59]	[60]	[61]	[62]	[63]
Voltage level	$4n+3$	$4n+1$	$6n+1$	$4n+1$	$6n+1$	$4n+1$
Switches	$2n+4$	$6n$	$5n+4$	$4n$	$5n+6$	$4n+4$
IGBTs	$3n+4$	$6n$	$6n+4$	$6n$	$5n+6$	$2n+6$
Gate circuit	$2n+4$	$6n$	$5n+4$	$4n$	$5n+6$	$4n+4$
ON state switches	$n+2$	$3n$	$2n+2$	$2n$	$3n+6$	$n+3$
Total blocking voltage	$(11n+6)V_{dc}$	$(8n)V_{dc}$	$(19n)V_{dc}$	$(4n)V_{dc}$	$(21n+6)V_{dc}$	$\frac{1}{2}(16n+3n^2+1)V_{dc}$

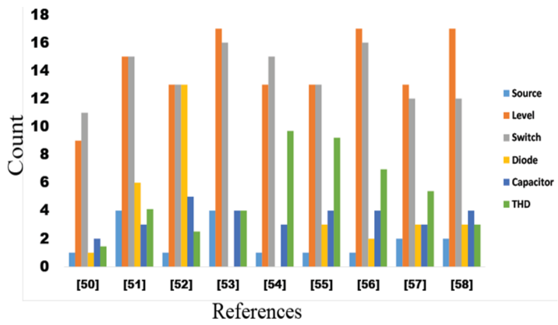


Figure 8. Comparison of different reference vs parameters of RDC MLI's

4. ANALOGOUS ANALYSIS OF MODIFIED MLIS

A primary aim of modified MLIs is in enhancement of output voltage waveform levels with minimal device usage. In this context, this section conducts comparisons. An asymmetric CHB MLI requires fewer switches to achieve specific levels in comparison with inverters. Lee *et al.* [64] introduced a sequential arrangement that incorporates a condensed module. This arrangement exhibits a reduced quantity of switching components and offers protection against voltage surges arising in periods of inactivity. Within devices with coils, the arrangement effectively enables the uninterrupted movement of coil-induced electrical currents by establishing a path for unrestricted flow. An illustration of a 7-level sequential condensed module multilevel inverter (CCMMLI) is depicted in Figure 9(a). Table 5 provides component details and output voltages for various inverter topologies. The relationship between switching devices and level count highlights that reduced device count (RDC) multilevel inverters employ fewer switches than conventional types.

A densely populated unit cell (PUC) topology in MLIs can increase the number of output voltage levels while reducing the number of components compared to traditional multilevel inverters. As a result, it leads to lower power losses, requires fewer triggering circuits, and simplifies the overall topology. The fundamental building block of this configuration consists of a direct current (DC) source or a capacitor along with two unidirectional switches. In Figure 9(b), a 7-level single-phase PUC topology is presented by Ounejjar *et al.* [65]. Furthermore, the same researcher enhances the control over the PUC topology dynamics through the implementation of a hysteresis controller.

Samadaei *et al.* [66] proposed the utilization of an asymmetrical square T (ST) module in a multilevel inverter configuration. The fundamental component of this arrangement, depicted in Figure 9(c), is capable of producing 17 distinct levels in the output voltage, all achieved without the need for an H-bridge. Through a cascaded arrangement, the basic unit can be further extended to generate additional levels in the output voltage. In contrast configuration in Figure 9(b) demands a high number of switches with an increase in level.

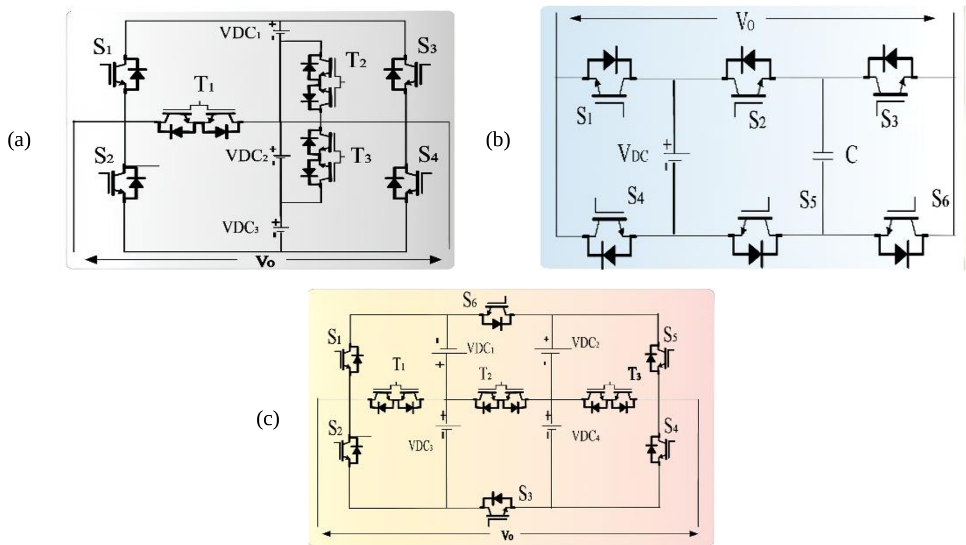


Figure 9. Multilevel inverter topologies: (a) CCM MLI, (b) P U cell MLI–7 level, and (c) asymmetric switched t-type multilevel

Table 5. Summarizes research contributions by various authors related to RDCMLI

No. of switching devices (S)	Levels (k)	Type	Reference
$2nc + 2$	$2^{(nc+1)} - 1$	PUC MLI	[65]
$12\ kst$	$16\ nst + 1$	ST MLI	[66]
$2(k + 1) + 1$	$k(k + 1) + 1$	BS-MLI	[67]
$6k + 4$	$1 + 2^{(k+2)} + 2^{(2k+1)}$	SMLI	[68]
$6k + 2$	$8\ k + 1$	BSC MLI	[69]
$4k + 2$	$2^{(k+1)} - 1$	HB MLI	[70]
$10\ kcm$	$6\ kcm + 1$	CCM MLI	[71]
10	9	IQB9L	[72]
12	11	11 Level Hybrid MLI	[73]
30	$7 + 2(n - 1)$	T-S cells	[74]
$9 + 2(n - 1)$		S-T cells	[74]

5. APPLICATIONS OF MULTI-LEVEL INVERTERS IN RES

MLIs are strongly recommended for high-power applications. These versatile MLIs find extensive use across various applications, including power supplies (PSs), in grid-connected systems, and numerous MLI configurations successfully integrated with RESs to facilitate the seamless contribution of RES-generated electricity to the grid. Solar photovoltaic (PV) has gained considerable importance due to its multitude of benefits. These include easy installation, extended life span, noise-free operation, environmental friendliness, quick deployment, flexibility in component mobility and portability, and the ability to generate electricity. PV arrays offer the capability to generate power that can meet high load requirements, making them suitable for various industrial applications. These include battery charging systems, solar cars, other equipment, and more. However, PV generating systems have certain limitations, for instance, lower conversion efficiency, and susceptibility to weather conditions. This output of PV cells is correspondingly influenced by solar intensity or radiation and, to a lesser extent, by temperature variations.

To match certain solar panel properties with load characteristics, DC-DC [75], [76] converters were used. The correct kind is selected based on the anticipated voltage requirements. Batteries are utilized to enable PV systems to function as reliable power sources, ensuring stable voltage levels that adapt to changing loads. Additionally, batteries are employed for power storage and to provide temporary correction for power fluctuations, thus aiding in power conservation. The limited conversion efficiency of PV modules has emerged as a hindrance to the advancement of PV systems. To address this challenge, research efforts are focused on integrating power converters with maximum power point tracking (MPPT) capability into PV. This integration aims to optimize the extraction of energy from existing atmospheric conditions. MPPT controllers play a crucial function in tracking MPP and have thus gained significant attention as a vital component of PV systems that require enhancement.

Based on the available literature [77]. There is a broad spectrum of MPPT algorithms to choose from. Each with its own set of constraints, requirements, and applications. MPPT techniques are classified into several types, including sensor implementation, tracking approach, and current. These broad classes are further subdivided depending on various variables, operating principles, or implementation. They are broadly categorized and shown in Figure 10 and tabulated in Table 6.

High switching frequency (HSF) and fundamental switching frequency are the two primary modulation techniques used in multilevel inverters. Unlike HSF, which involves multiple commutations per cycle, fundamental switching frequency requires only one or two commutations per cycle [78]. The two major forms of high switching frequency modulation are pulse width modulation (PWM) and space vector modulation (SVM).

In references to single-phase multilevel inverters (MLIs), as outlined in [79] a modified single-phase multilevel inverter for photovoltaic (PV) applications was proposed by Rajalakshmi and Rangarajan [74] This particular design necessitates nine switching devices, three diodes, and three DC sources to achieve thirteen output voltage levels. Bana *et al.* [80] introduced an alternative multilevel inverter with a reduced device count, featuring an H-bridge-based MLI and a level-doubling circuit. The implementation of a polarity changer was utilized to produce negative voltage levels, with the output voltage being regulated through the application of the selective harmonic elimination pulse width modulation (SHE-PWM) technique.

A dual-source multilevel inverter for PV systems was developed by Ponnusamy *et al.* [81], comprising a level generator and a polarity changer. This particular inverter underwent testing in both symmetric and asymmetric modes utilizing nearest-level modulation (NLM). Pourfaraj *et al.* [82] put forth a proposal for a single-phase dual-mode interleaved multilevel inverter, which integrated a step-up chopper to enable operation in both step-up and step-down modes, in conjunction with a polarity changer. Mukundan *et al.* [83] fused a support vector machine (SVM) converter with a newly developed multilevel inverter. The generation of positive voltage levels was facilitated through a level generator, while the management of negative levels was handled using a polarity changer.

Modulation techniques of multilevel inverters (MLI) are of significant importance as they directly influence the overall efficiency of the system. Various modulation methods have been proposed within the domain of multilevel inverters (MLIs). These methods are employed to regulate both the output voltage and current, as well as to compute crucial MLI parameters like total harmonic distortion (% THD) and switching losses. The primary goal of utilizing a modulation signal is to produce a discrete waveform that accurately represents a specific reference signal. This waveform encompasses variations in frequency and amplitude, along with a fundamental component that typically demonstrates sinusoidal characteristics in a stable state. A visual representation illustrating common modulation strategies can be observed in Figure 11. Several key factors are taken into consideration when selecting an appropriate modulation technique for a specific MLI configuration, including distortion levels, total harmonic content, switching frequency, power losses, and response time.

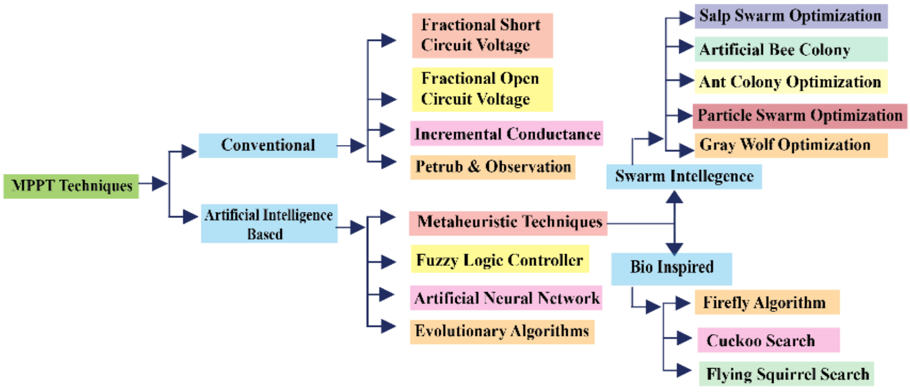


Figure 10. MPPT methods

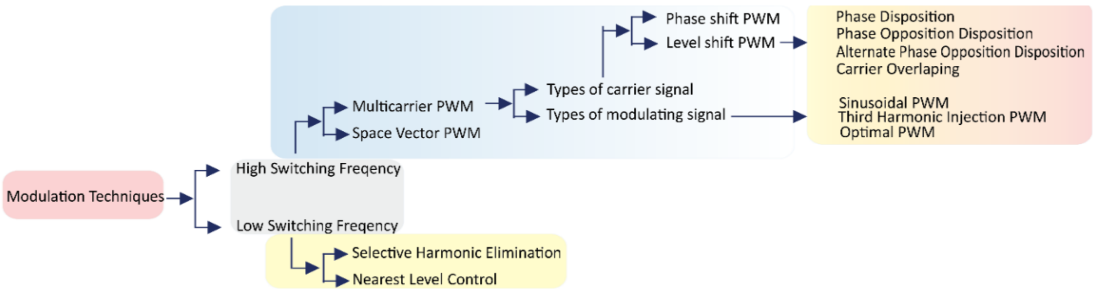


Figure 11. Modulation techniques for RDC ML

Table 6. MPPT inverter types and specifications

Ref.	Inverter type	Switches	Level	MPPT
[74]	Modified CHB	9	8	-
[84]	S-packed U-cells	5	5	IC with Hysteris controller
[85]	Switched capacitor MLI	7	8	Fuzzy controller
[86]	Switched capacitor MLI	29	9	Grey wolf optimization technique and fuzzy logic control
[87]	Cascaded H-bridge sub-MLI	15	7	Fuzzy logic
[88]	Neutral-point-clamped multilevel inverter (NPC)	6	5	Artificial neural network (ANN)
	Voltage level boost (VLB) MLI	10	15	Distributed maximum power point tracking (DMPPT) Control
[89]	Nine-level active neutral point clamp inverter	10	9	Predictive control technique

6. EMERGING CHALLENGES AND AVENUES FOR FURTHER EXPLORATION

Progress in power electronics components and associated techniques has spurred wider integration of RESs into grids. However, this adoption has given rise to various concerns regarding power quality, safety, energy storage, intermittent energy delivery, stability, and robustness. Consequently, numerous Regulations and protocols have been established for grid-connected renewable energy systems (RESs) to uphold power integrity. Based on the existing literature evaluation, there are specific areas that require further research in this domain, which are noted below:

i) Addressing the intermittent power supply from renewable energy sources (RESs) represents a significant hurdle in grid-connected RES systems. Given the anticipated increase in RES contribution to the global energy market, it becomes crucial to tackle power instability.
ii) The gradual integration of RE systems into power grids, facilitated by apt multilevel inverter (MLI) technologies, has propelled power networks aiming for the advancement of the modern grid. While transition poses notable challenges, it also presents opportunities for constructing and controlling MLI topologies. Consequently, noteworthy advancements have been made in this field.
iii) There is a need for further research on modern Multi-Level Inverters to effectively confront challenges experienced in grid-connected RES deployments.
iv) Many factors influence the effectiveness of the MPPT algorithm, like nonlinear, functioning state, and fluctuations. Which resulted in system failure under certain operating settings? As a result, designing is a time-consuming operation that requires greater criteria to ensure a steady state
v) Grid Resilience: As renewable energy systems (RESs) become more prevalent in grid infrastructure, ensuring grid resilience and stability in the face of intermittent power supply remains a significant challenge. Future work should focus on developing advanced energy storage technologies, robust grid control mechanisms, and improved forecasting methods to mitigate the impact of power fluctuations.
vi) Integration with diverse sources, into existing grids, presents technical, operational, and regulatory challenges. Future research should explore innovative strategies for seamless integration, including optimal DER placement, advanced power management algorithms, and effective grid communication protocols.

While a considerable number of RSC-MLI topologies have been documented in open-loop arrangements with RL loads, a select few specific configurations have been examined for specialized applications such as photovoltaic (PV), adjustable speed drives, power quality enhancement, flexible AC transmission systems (FACTS), solid-state transformer, energy storage solutions, electric vehicle system, wireless power transfer mechanisms, and power factor correction methodologies. Notwithstanding their prevalence in scholarly discussions over the preceding decade, RSC-MLI topologies have not yet achieved extensive implementation in commercial contexts.

The sluggish advancement into the commercial domain can be ascribed to the diminished switch count in numerous configurations, which has, in turn, led to a reduction in switching redundancies and modularity. This decline has adversely affected the efficacy of the DC link, alongside fault tolerance and reliability metrics. Nevertheless, particular configurations, notably MLDCL, T-type, half-leg T-type, and LDN, are progressively gaining traction and are anticipated to assume a pivotal role in forthcoming industrial applications.

7. CONCLUSION

This study has provided a brief overview of MLI to emphasize better and more innovative topologies. They had been developed in a variety of ways, including classifications, benefits, drawbacks, and the ability to improve power transmission in current systems. According to the assessment, a redesigned technique employing a higher level with less count of devices, affordability, decreased THD, and efficiency. Re-defined MLIs were potential alternatives to the present-day energy scenario. The strategies for the current leakage elimination of modern MLI were discussed. Finally, the obstacles and future progress for better green were presented.

Global progressions within diverse sectors and scholarly investigations have resulted in an escalating necessity for converters that exhibit high energy efficiency. Multilevel inverters (MLIs) are especially sought after for their pivotal function in the conversion of DC to AC, particularly in applications characterized by high power and elevated voltage, attributable to their intrinsic advantages. These advantages encompass direct engagement with intermediary voltage levels, a decrease in the requisite number of semiconductor devices and DC sources, streamlined gate driver circuits, improved efficiency, reduced costs, and a compact form factor. Such characteristics have propelled RSC-MLIs from a theoretical framework to practical implementations.

This literature review scrutinizes prevalent topologies and modulation methodologies, juxtaposing their performance indicators. It concludes that asymmetrical multilevel inverters confer greater advantages in comparison to their symmetrical counterparts. The principal emphasis of this review is directed towards multilevel inverter topologies that necessitate a diminished number of switches. The article delivers an exhaustive examination of modulation techniques applicable to both low and high switching frequencies. Its objective is to compile critical information for practitioners engaged in this domain, furnishing insights for the selection of optimal topologies for specific applications, alongside recommendations regarding switching methodologies and control techniques.

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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
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Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

Data availability is not applicable to this paper as no new data were created or analyzed in this study.

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