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Teaching learning optimization technique FOPID controlled Cuk and SEPIC converter-based PF rectification

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ABSTRACT

The foremost cause of harmonic contamination is the ample utilization of loads of non-linear type such as static power converters. Because of this load, the input power factor (PF) decreases heavily as they draw a current of non-sinusoidal in nature. This article gives a general presentation investigation of two PF rectification (PFR) converter (PFRC) geographies: Cuk type and single-ended primary-inductance converter or SEPIC type converter. The average current control (ACC) technique is utilized here. Notwithstanding, for control of output voltage, techniques like conventional proportional integral derivative controller (PIDC) or fractional order proportional integral derivative controller (FOPIDC) are used, and the gains of the controller are calculated using a novel teaching learning optimization technique (TLOT), considering integral time absolute error (ITAE). The analysis of both PFRC acted in Simulink/MATLAB and the estimated converters are studied under consistent and dynamic state conditions. The FOPIDC Cuk PFRC is providing 2.97% of THD compared to other converters.

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1. INTRODUCTION

The impact of power quality is worsening daily due to the commercial and industrial loads with their non-linear characteristics [1]. Therefore, it is necessary to improve the power quality and power factor using different compensating devices and power factor correction devices. Power factor (PF) rectification (PFR) has arisen as a fundamental piece of the cutting-edge power system for its usage and power transfer. A diode bridge and capacitor in shunt [2] are utilized to get DC voltage output. PFR outline is portrayed in Figure 1(a), while in Figure 1(b), a comparison of supply voltage-current is portrayed. As Figure 1(b) tends to see, the input current is nonlinear amid extensive harmonics [3], and the input PF is exceedingly reduced. The current harmonics [4]-[6] are wisely adverse due to electromagnetic interference or EMI problems through communication or line voltage tainting paths. Be that as it may, if such sorts of most extreme burdens are related to the supply, there will be a difficult issue. A portion of the global norms, similar to the IEC & IEEE license the limitations of harmonic incidence in supply current akin to IEEE 519 [7]-[9].

The primary goal here is to look after an AC-DC PFR to cancel out the above PF issues [10], [11] and to achieve unity power factor (UPF) at supply and regulated voltage at output [12]. Again, in comparison to

previous work such as [11], [13], in this work the PF rectification (PFR) converter PFRC has been tested under transient conditions and the % output voltage ripple is calculated to ensure reduced filter capacitor burden. A one-switch DC converter is used for single-phase AC-DC and minute power utilizations. These types of converters may be directed at the wanted voltage output, in addition to UPF at the input side. In aperfect world, there are three essential kinds of converter geographies in non-segregated classification, for example, buck-boost, buck, and boost configuration [14]-[16]. Every time a small voltage output is required, at that point buck PFRC is required; however, buck converter provides an input current of commuted type with elevated frequency. Be that as it may, given its driven nature, it gives an intruded-on current related to a quick recovery circuit. The significant fault with the Buck PFRC is: it requires a filter inductorat the input side.

The filter inductor creates a variable consistent current in the supply region. However, boost PFRC configurations create enormous result voltage and cause excess-voltage trouble on the switch [17]. The third converter, i.e. buck-boost, was found to be essential for PFRC. This converter includes ZETA, Cuk, and single-ended primary-inductance converter or SEPIC [18]. In this writing, two distinct configurations, for example, SEPIC and Cuk are utilized for PFR, amid minimum total harmonic distortions (THD) of input current alongside directed DC voltage and diminished voltage ripple [19]-[21]. The total plan and PFRC models are finished utilizing the MATLAB/Simulink tool.

The major contribution of the proposed study is as: i) To create a fractional order proportional integral derivative (FOPID)-controlled Cuk and SEPIC converter Simulink model to improve the system's power factor; ii) Optimised fractional order proportional integral derivative controller (FOPIDC) is used to extract the peak of current reference; iii) Teaching learning optimization technique (TLOT) is employed for optimization of controller parameters of FOPIDC; iv) Controller (FOPIDC) actions are tested in steady-state and transient conditions; and v) Relative study to declare the superior rejoinder of TLOT based FOPID-controlled Cuk converter. The supplementary sections of the manuscript are organized in the following way. Cuk and SEPIC converter design and analysis along with different PFRC methods and the proposed optimization technique, is discussed in detail in section 2. Section 3 discusses results and analysis. Sections 4 present the future scope and conclusions.

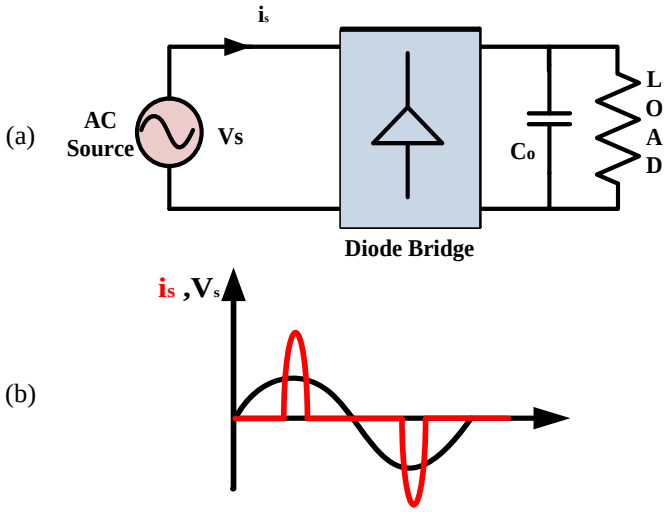

Figure 1. AC-DC converter along with voltage and current waveforms: (a) diode bridge and capacitor in shunt with load and (b) supply voltage-current

2. CONVERTER DESIGN AND ANALYSIS

A converter (Cuk or SEPIC) of DC-DC type is interfaced close to the rectifier,to get a superior PF and desired voltage in system supply and load, respectively. The introduced AC-DC SEPIC and Cuk PFRC circuit configurations are shown separately in Figures 2 and 3. Input current wave can decrease by utilizing this arrangement with controlled output voltage. This issue is highly excellent in regular buck/boost converter. Both inductors (input and output) are kept in similar attractive centers in a converter like Cuk or SEPIC to accomplish the most extreme coupling coefficient. Whenever, L_1 and L_2 the inductors, store energy switched ON, increasing current in the inductor-capacitorprovides power to output. Diode becomes RB for this situation. In switch OFF duration, the diode becomes forward bias (FB), storesenergy, and is put away to load. Table 1

portrays the demonstrated conditions of the expected PFRCs. Where V_o and P_o is, load voltage and power, Δv_o and Δv_c represents, voltage ripple of output and capacitor, Again the current ripple of an inductor, supply voltage, frequency of switching and duty cycle represents as: f_s and d.

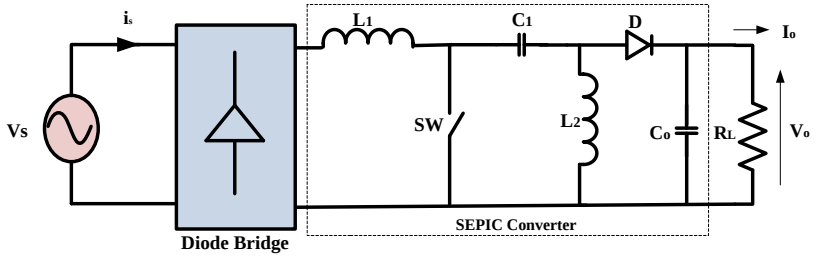

Figure 2. Structure of SEPIC PFRC

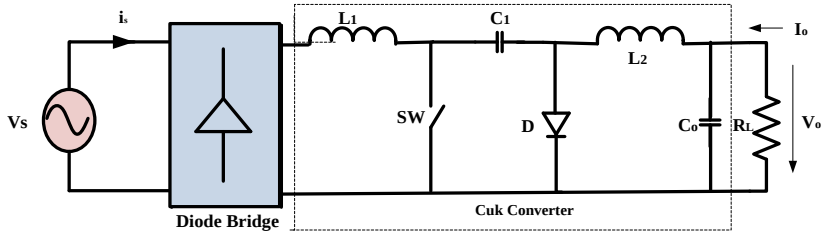

Figure 3. Structure of Cuk PFRC

Table 1. Design formula of Cuk and SEPIC PFRC

Parameters	SEPIC	Cuk	Parameters	SEPIC	Cuk
L_1	$\frac{v_s * d}{\Delta i L_1 * f_s}$	$\frac{v_s * d}{\Delta i L_1 * f_s}$	C_1	$\frac{i L_2 * d}{\Delta v_{c_1} * f_s}$	$\frac{I_0 * (1-d)}{\Delta v_{c_1} * f_s}$
L_2	$\frac{v_s * d}{2 * \Delta i L_2 * f_s}$	$\frac{v_s * d}{\Delta i L_2 * f_s}$	C_o	$\frac{P_o}{4\pi * f_s * V_o * \Delta v_o}$	$\frac{v_s * d}{8 * f_s^2 * L_2 * \Delta v_o}$

2.1. Different PFRC methods

The fundamental objective of PFRC is to get the desired voltage at load, and secondly, the source current must be a sine wave. In this manner, a response from the load is utilized to get the desired voltage. Besides, to achieve the other goal, two techniques are generally utilized: the multiplier technique (MT) [22] and the voltage follower technique (VFT) [13], [23]-[25]. The VFT method of PFRC is generally used for very low power application and produce high devices current hassle. In the Multiplier Technique, a current response is utilized from the source to manage the PFRC alongside the voltage response, as represented in Figure 4. The MT method is further classified into four types such as: i) Peak current control (PCC); ii) Hysteresis current control (HCC); iii) Borderline current control (BCC); and iv) Average current control (ACC)

There are some demerits of the other three (PCC, HCC, BCC) MT method such as: PCC method needs an external compensation ramp, HCC method produces variable switching frequency pulse width modulation (PWM) pulses, BCC method is more sensitive to commutation noises and needs a zero current detector circuit. To overcome the above issues, in our proposed work ACC method is used which gives a constant switching frequency PWM pulses, does not need a compensation ramp and less sensitive to commutation noise. Hence, Figure 5 depicts the ACC method which gives a reduced %THD input current used here. Generally, a current error amplifier filters the input inductor current, which in turn drives the PWM modulator. Because of the current loop at the input, the error gets reduced between the reference and input current. Whereas, the PIDC or FOPIDC gives the current reference, an amplifier of voltage error type. Again, in ACC, a constant switching frequency PWM pulse is obtained, which in turn eliminates the commutation noises. No compensation ramp is required in ACC, but the actual inductor current needs to be sensed in ACC.

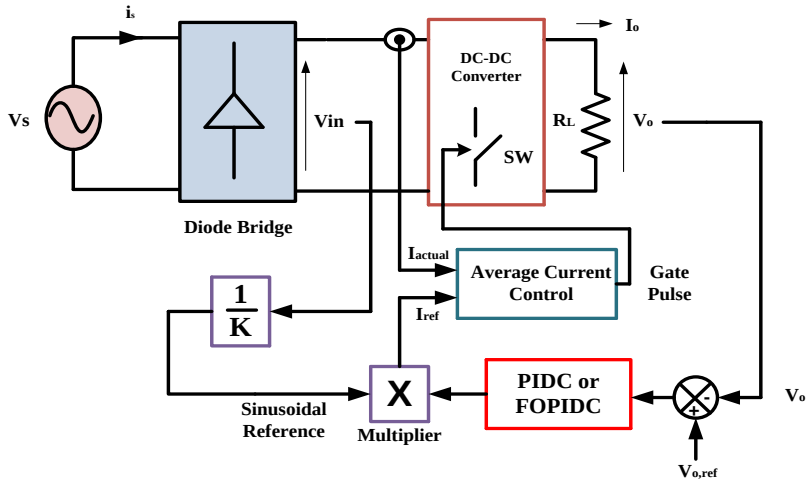

Figure 4. Multiplier technique

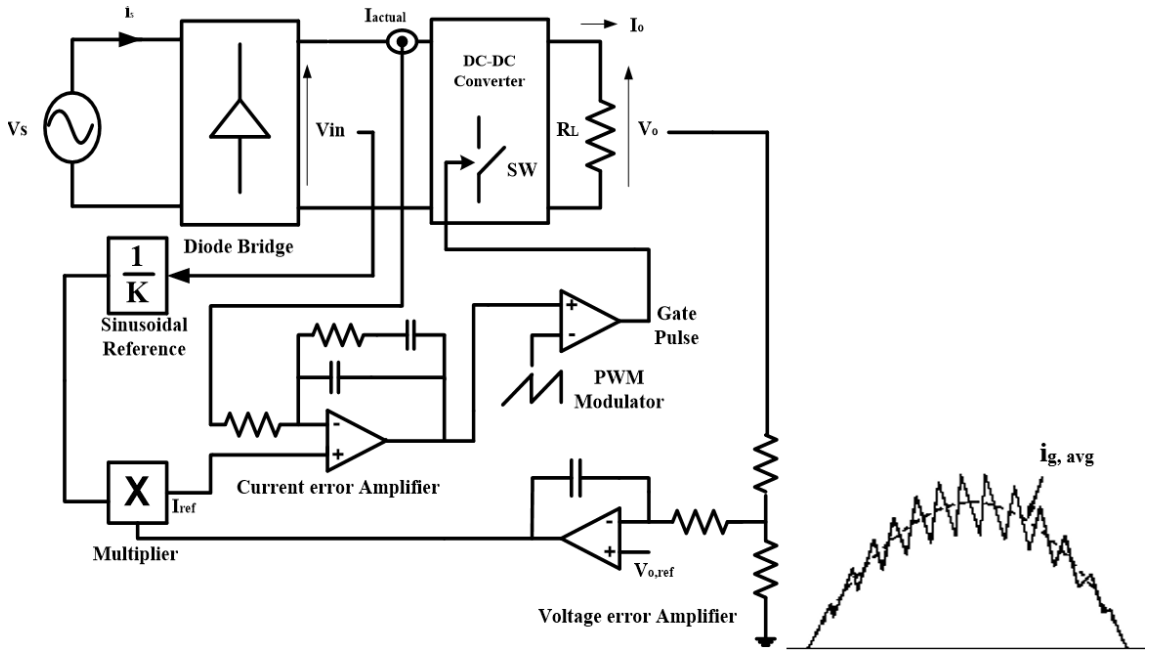

Figure 5. MT with ACC technique

2.2. PIDC and FOPIDC

PIDC is outlined in Figure 6. PIDC is known numerically (1).

$$u(t) = K_p e(t) + K_i \int_0^t e(t) + K_d \frac{de(t)}{dt} \quad (1)$$

A fractional order $PI^{\alpha}D^{\beta}$ controller-based PFC converter is presented in Figure 4 . In FOPID control, $e(t)$ the error signal, produce $u(t)$ the control signal. FOPIDC transfer function can be formulated as (2) [9].

$$TF = K_p + \frac{K_i}{s^{\alpha}} + K_d s^{\beta} \quad (2)$$

In (2) K_p, K_i, and K_d are the PID gains respectively and α, β are fraction of integrator and differentiator. Necessary steps for FOPIDC design are:

- Put in K_p to decline, rise time and error at steady-state.

- $K_d$is added to lessen % OS and time to settle.
- Further include K_i eliminating error at steady-state.
- Polish up again K_p, K_i, K_d, α, and β, to get the wanted output.
- FOPIDC Simulink structure is depicted in Figure 7.
- In MATLAB/Simulink using the FOMCON toolbox and TLOT, FOPIDC parameters are designed as shown in Table 2.

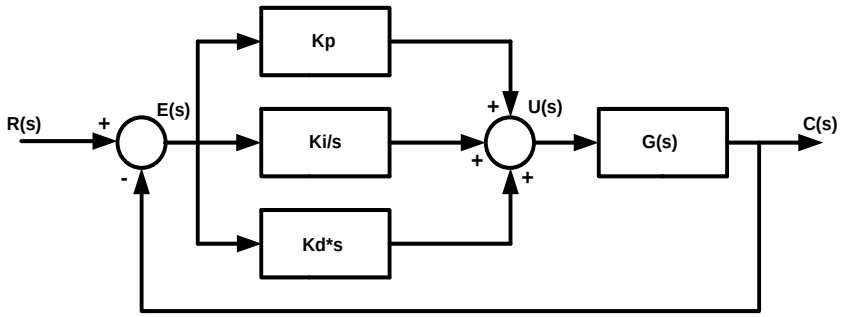

Figure 6. PIDC

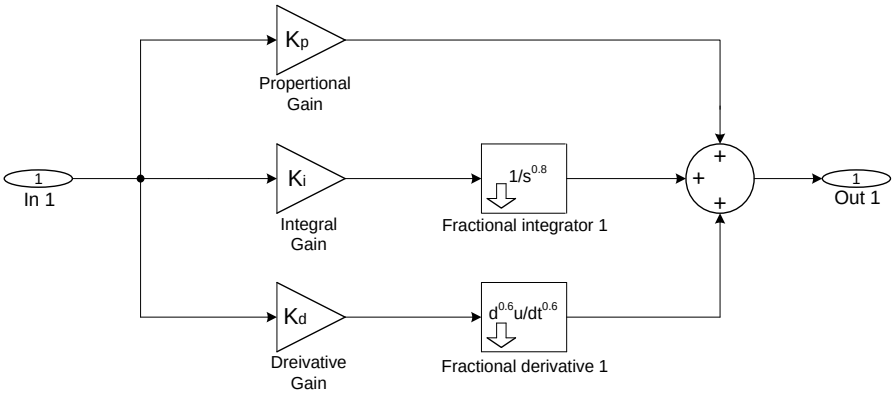

Figure 7. FOPIDC Simulink diagram

Table 2. Values of FOPIDC

K_p	K_d	K_i	α	β
15.11	3.89	2.34	0.8	0.6

2.3. TLOT

TLOT is known to be a novel information-based approach, in which the best student of the past will become the teacher in the next iteration. Subsequently, the further students have to be trained as of thatnew teacher & distribute their information to transform the measured pupil's information. In this way, previous or unpredicted convergence can be avoided, and the multiplicity can be conserved. In the last few decades, a lot of researchers have found attention in the optimization area. Mutation and crossover are found to be the foremost steps in any evolutionary techniques, but not in TLOT. TLOT has lots of similarities with various other evolutionary techniques and is aggravated by teaching-learning activities. Based on self-learning and other's experience, each member possesses an adjustable explore method in TLOT. Once the global optimum is found, to attract the whole member to that position, this experience is communicated to them. From the literature, it is obvious that TLOT may be implemented effortlessly and works greatly superior compared to other techniques. TLOT may be trapped in any neighboring maxima or minima for an intricate and multi-modal problem, which can be avoided by extensive-range learning methods.

2.4. Objective function

Here the objective function (OF) is of ITAE type, and the DC link capacitor voltage error is the OF [9]-[12]. The foremost objective is to minimize the error e(t), which is the variation between actual and reference DC link capacitor voltage. An abrupt raise or reduction in load is considered here for this J, the OF, as given in (3).

$$J = \int_0^{tsim} t|e(t)|\,dt \tag{3}$$

3. RESULTS AND DISCUSSION

The Simulink structure is made in Simulink programming to analyze exhibitions of the anticipated Cuk and SEPIC PFRC. Table 3 depicts the framework model boundary of the two PFRC. First, the framework is broken down without associating any PFRC. %THD examination and different wave shapes are shown in Figure 8. Like Figure 1, the supply current is a pulse type comprising bunches of harmonics having 191.36% of %THD. Now Cuk, SEPIC PFRC is used to enhance system performances. First, the PFC converter is tested in an open loop (OL) and with PID controlled Cuk and SEPIC PFRC, results are given in Table 4.

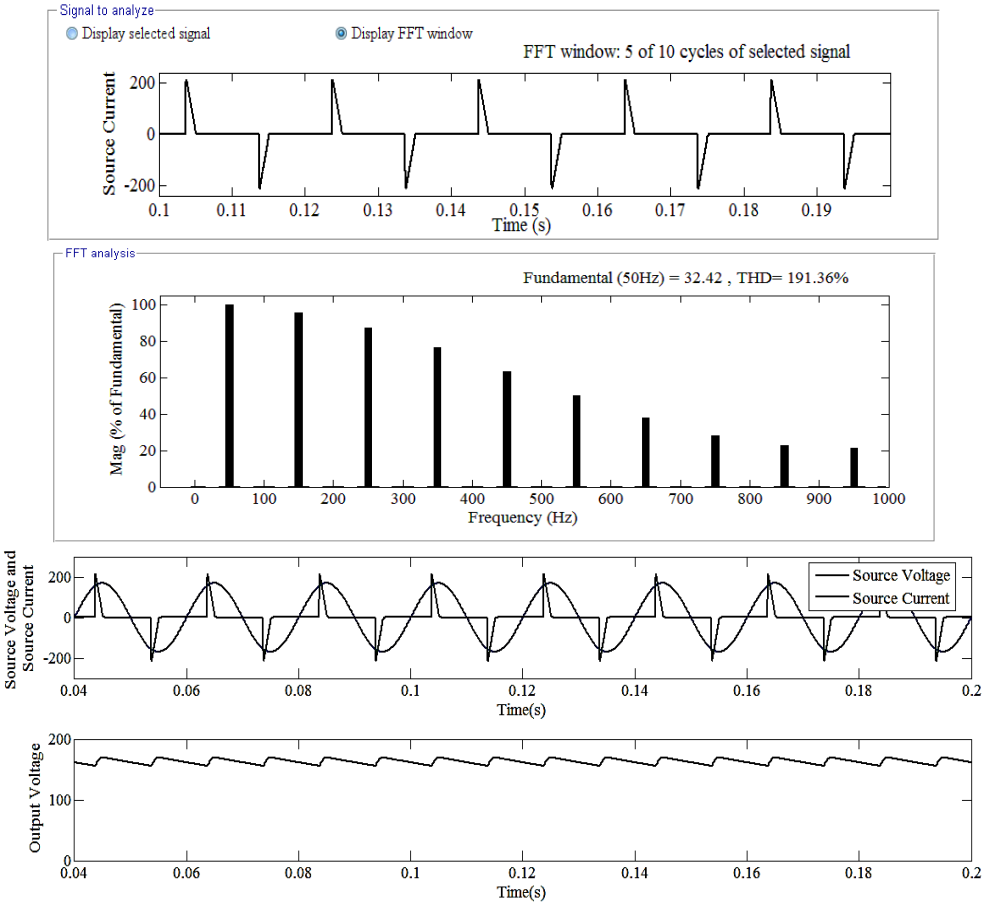

Figure 8. Without converter results

Table 3. System considerations

Parameters	Values	Parameters	Values
RMS supply voltage	120 V	Power output	1000 W
Supply frequency	50 Hz	Output voltage reference	100 V
L_1, L_2	6 mH, 10 mH	Switching frequency	40 KHz
C_1, C_o	10 mF, 10 mF	$\%\Delta v_o$ and $\%\Delta v_c$	5%
d	0.45		

Table 4. Converter's performance comparison

Performance Parameter Various situation	THD %	Supply PF	O/P Voltage Ripple %	Performance parameter Various situation	THD %	Supply PF	O/P Voltage Ripple %
No PFRC	191.36	0.4479	9.2	PIC Cuk PFRC [17]	3.13	0.9990	2.1
SEPIC OL PFRC	4.37	0.9986	2.0	FLC Cuk PFRC [17]	2.87	0.9991	1.8
Cuk OL PFRC	4.70	0.9986	2.2	PIC Boost PFRC [13]	6.81	0.9997	-
PIDC SEPIC PFRC	4.17	0.9983	2.1	FOPIDC SEPIC PFRC	4.16	0.9997	1.5
PIDC Cuk PFRC	3.73	0.9980	2.4	FOPIDC Cuk PFRC	2.97	0.9999	1.4

Different waveforms like supply current fast Fourier transform FFT examination, supply voltage, load voltage and supply current of FOPIDC based Cuk PFRC are portrayed separately in Figure 9. The primary contrast between Cuk and SEPIC PFRC is, Cuk produces a reverse voltage output the FOPIDC based SEPIC PFRC portrayed in Figure 10. To test regulator strength a variation of the load is used at 1sec. It tends to be seen that voltage is constant at -100 V. Supply PF, %THD source current is viewed as 0.9980, 3.73% and 0.9999, 2.97% separately for PIDC and FOPIDC Cuk PFRC. From THD values the FOPIDC Cuk PFRC produce improved outcome than PIDC Cuk PFRC.

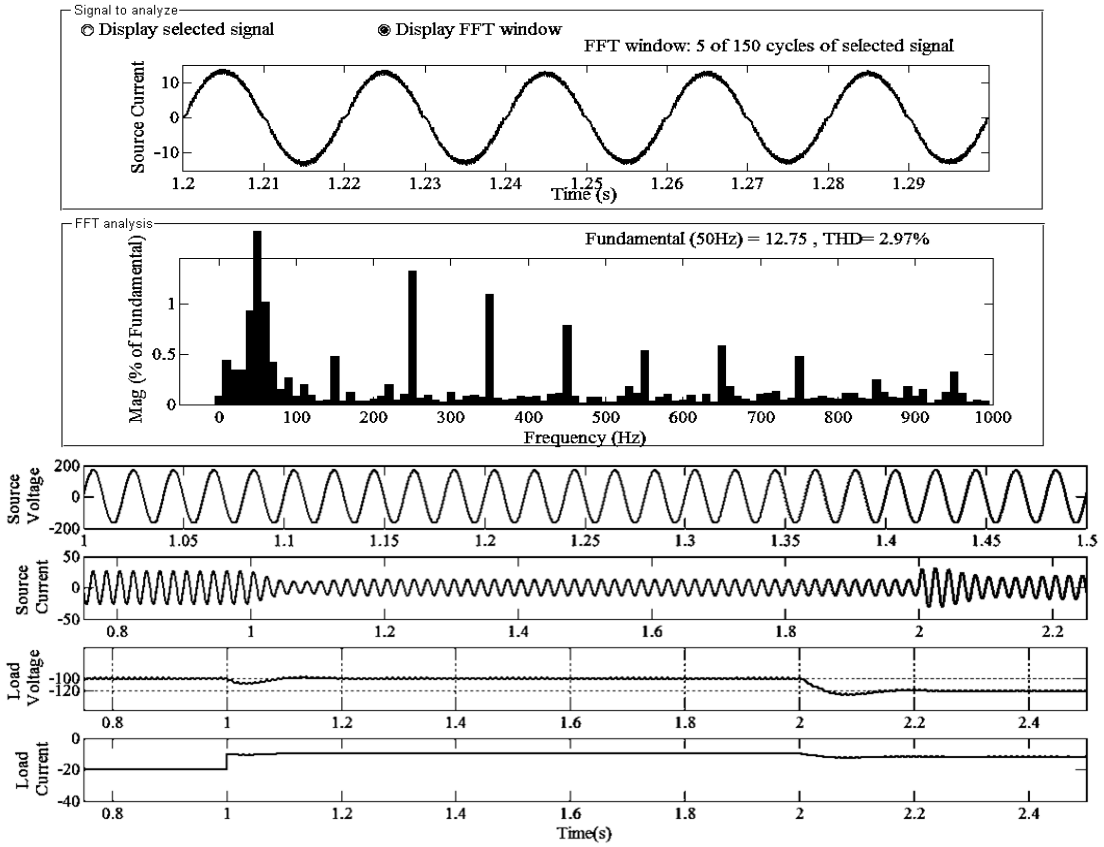

Figure 9. Wave shapes of FOPIDC Cuk PFRC

Likewise, in the following phase, SEPIC PFRC is integrated into the framework, involving PIDC & FOPIDC regulators in the response path. Different wave shapes, for example, supply current FFT examination, supply voltage, and load voltage/current of FOPIDC based SEPIC PFRC are portrayed in Figure 10. For strength testing, alongside load variation a reference variation (100 V to 120 V for SEPIC PFRC and -100 V to -120 V for Cuk PFRC) is used at 2 sec. Again, it tends to be noticeable, as seen in Figure 10, that FOPIDC SEPIC PFRC produces preferable performance over PIDC SEPIC PFRC. Again, a comparative study is also done from the previous work [17] and [13] to ensure the superiority of the proposed work. A proportional integral controlled (PIC) and fuzzy logic controlled (FLC) Cuk PFRC is proposed, and the supply PF, %THD is found to be 0.9990, 3.13% and 0.9991, 2.87% separately for PIC and FLC based Cuk PFRC [17]. Samarth and Gemlawala [13] have proposed a PIC based boost PFRC and found the 0.9997, 6.81% as the supply PF, %THD. Contrasting all 10 contextual investigations FOPIDC Cuk PFRC produces superior execution

parameters, for example, the least %THD, decreased load voltage ripple and further developed supply PF. Different outcomes acquired in various contextual analyses are organized in Table 4.

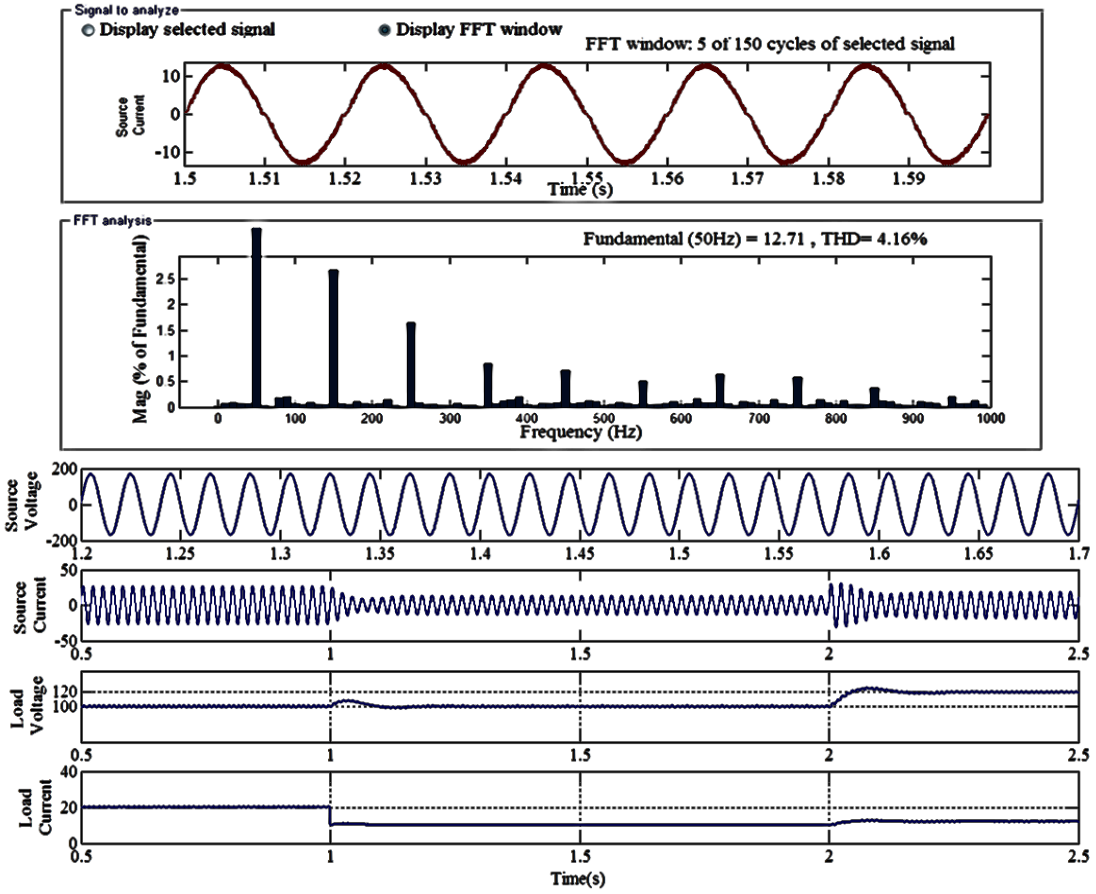

Figure 10. Wave shapes of FOPIDC SEPIC PFRC

4. CONCLUSION

In this work for PFR, 2 PFRC converters, SEPIC and Cuk, using ACC method are utilized to be specific. The main advantages of the proposed control method are unvarying switching frequency, does not require any reparation ramp and because of current filtering, the method is fewer perceptive to commutation noise. The output voltage of the converter has the same polarity as that of the input voltage. Similarly, the SEPIC has unique features, such as non-inverted output, continuous input and output currents, and better performance. The projected PFRC is performed employing the Simulink tool. The simulated results show the enhancement in supply current %THD with nearly UPF at the supply and diminished ripple load voltage. When contrasted with PIDC, FOPDIC gives further developed results, for example, supply current %THD and PF. Besides, FOPDIC-based Cuk conveys a well-desired voltage, the least %THD (2.97%) during the unsettling influences of load and deviation of reference. The estimated PFRC SEPIC and Cuk are to be investigated in real-time, for better insight into the same and will be our future work.

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