

Battery integrated three input high gain DC-DC converter for renewable energy sources

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ABSTRACT

In this work, a battery-integrated three-input converter is proposed. The topology combines a traditional boost converter on one side with a non-coupled inductor-based buffer stage on the other side. Some merits of the converter are a high voltage gain, a high output voltage in the battery discharging mode, and a wide range of output voltage. The bidirectional port makes it attractive for renewable energy (RE) sources like solar and fuel cells. The converter can operate in three modes that are determined by the availability of renewable energy (RE) sources and the battery state of charge (SOC). The power management algorithm enabled the converter to work in either single-input, double-input, or three-input configurations. The duty ratios of assigned power switches controlled the output voltage and the battery charge/discharge. Steady-state analyses and dynamic modeling are presented and discussed. At 12 V and 24 V input voltage, the output voltage of 315.52 V was delivered in the battery-excluded mode. The battery discharging mode delivered 311.57 V while the battery charging mode delivered 301.32 V. The proposed converter can serve low to medium power voltage/power applications. The hardware experiments verify the workings of the proposed converter.

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1. INTRODUCTION

The adoption of renewable energy (RE) sources has been on the increase in recent times. The major driving force behind the agitation of the utilization of RE sources is the call to scale down the emission of greenhouse gases from the burning of fossil fuels [1]. It has also been determined that fossil fuel reserves are gradually diminishing [2]. The pursuit of cleaner, sustainable energy resources does not end in the power generation sector. Studies show that the transportation sector contributes significantly to environmental pollution [3]. Although hybrid electric vehicles are gradually gaining ground, efforts are directed at summarily replacing gasoline vehicles with electric vehicle alternatives in the coming decades via legislation. Unfortunately, the RE sources face impediments to their optimal power delivery and performance. Their electrical characteristics waver with time, and availability relies on factors like sun irradiance, ambient temperature, wind speed profile, or water velocity [4]. These variations result in low voltage levels.

A scheme to mitigate the dilemma of capricious power delivery faced by RE sources is to incorporate more than one RE source to improve reliability. Regarding the low output voltage of RE sources, the DC-DC converters take center stage in power conversion to deliver regulated power to the load. They can step up or

step-down voltage levels as desired. Conventionally, applications of DC-DC converters are in a single-input source scenario. With the demerits of RE sources, using multiple RE input sources demands a multiple-input converter (MIC). In the early MIC, all input sources have their dedicated DC-DC converter, and the respective outputs are linked to a common DC bus. Apart from the bulky nature and high cost of such a setup, this configuration faces problems of difficult switching, voltage, and current control. For the contemporary multiple-input DC-DC converter, the independent RE sources are connected to a single DC-DC converter. This results in reduced cost and size. Hence, the MIC receives energy from all the input sources and delivers power to the load as desired, irrespective of the individual RE voltage levels. The MIC is widely used due to its capability to draw power individually and simultaneously from RE sources and deliver to a load.

A multiple-input converter that eliminates the deployment of an inductor in the topology was been proposed in [5], [6]. This topology employed the switched capacitors technique. While this converter achieved reduced voltage and current stresses, high output ripple and output leakage voltage persist. In [7], [8], a lone inductor has been added before the switched-capacitor-diode configuration. The high voltage gain was achieved in [9] by using coupled inductors and a clamping circuit. The high voltage gain MIC [10] can eliminate input current ripples and has low voltage stress. The MIC based on the flyback converter can deliver a high voltage gain in buck or boost mode [11]. The output voltage is non-inverted.

The double-input converter in [12] applied the boost cascaded charge pump method. It has the advantage of continuous current on the input ports, which is good for a photovoltaic source. A Z-Quasi Resonant network was proposed to reduce the voltage stress of the dual-input converter [13]. The converter is suitable for electric vehicles and microgrids. The converter introduced in [14] is suitable for PV storage. Two unidirectional ports suffice. Buck and buck-boost techniques are used at the energy buffer stage.

The application of the voltage multiplier cell as a means of attaining high voltage gain in MICs has been investigated [15]. The voltage multiplier stages follow an interleaved boost stage. A bidirectional function for a storage element was added [16] by looping a battery-based PVSC input. Mohseni *et al.* [17] explained that multiple output ports were added after the diode-capacitor stages. These converters suffer from high dissipation loss due to the increased number of passive elements. To reduce losses, an auxiliary ZVT circuit was added [18]. The coupled inductor technique was used to facilitate ZCS [19].

A double-input and double-output boost converter has been proposed in [20]. The converter achieved acceptable efficiency. However, has a high number of passive components. A bridge-type double-input topology was proposed in [21]. The boost converter has a simple structure and low cost. Low voltage gain is a drawback of the converter. Athikkal *et al.* [22] described a switched inductor module positioned after the dual input stage was employed to improve the voltage gain. In the modular converter proposed in [23], each additional input port is connected to an interleaved inductor branch in a cascaded structure. The primary input port is a boost converter lifted by a capacitor. It has a low voltage stress. The MICs discussed in [5]–[23] have no directional battery port. As such, they cannot serve the load when all the RE sources are low in power.

For MICs having a battery storage, [24] has a low voltage gain, and the battery can only be charged by one RE source. The modular switched inductors were investigated in the multi-input boost converter [25]. The drawback is increased size and cost. Another converter that possesses an energy storage element has been adapted for PV, fuel cell, and battery inputs [26]. It used a buck-boost configuration on one unidirectional input and the boost configuration on the other input. The boost configuration was used on both inputs to ensure continuous input current for RE sources [27]. Some weaknesses of these converters are the low voltage gain, especially in the battery discharging mode. There is also low efficiency due to passive elements. The output voltage of the converters in [24]–[27] during the battery discharging mode is lower.

This work proposes a non-coupled inductor/boost converter configuration to achieve high voltage gain for the operation modes of the battery-integrated three-input converters highlighted in the literature. Existing literature has ignored the output voltage during battery discharging operation. The proposed converter combines two RE sources and a battery. The non-coupled inductor configuration helps deliver a wide output voltage range and high voltage output despite the reduced input power levels in the battery discharging mode. This paper is organized as follows: i) The background and literature review are presented in the first section; ii) The second section shows the proposed converter, steady-state analysis, dynamic modeling, and power management; iii) Experimental results and comparisons are shown and discussed in the third section; iv) Section four provides conclusions to the paper.

2. METHOD

In this section, the configuration of the proposed converter will be presented. In addition, the operation modes and respective switching states will be discussed. The section will conclude with the steady-state analysis, component design, dynamic modelling, and power management algorithm.

2.1. Topology of the proposed converter

The proposed structure is presented in Figure 1(a). The right side of this converter is a conventional boost converter. On the left side is a non-coupled inductor-based converter configuration. There are three inputs that can be identified as V_1 , V_2 , and V_b . V_1 is tied to the simple boost converter, V_2 serves the uncoupled inductor-based converter. V_b is a battery source sandwiched between the two component converters. There are four power switches, S_1 , S_2 , S_3 , and S_4 in the circuit. Switches S_1 and S_2 serve the conventional boost converter and the non-coupled inductor-based boost converter, respectively. Switches S_3 and S_4 serve to charge or discharge the battery as well as complete the flow of current. Other components of the converter include three inductors (L_1 , L_2 , L_3), five diodes (D_o , D_1 , D_{b1} , D_{b2} , D_m), and four capacitors (C_o , C_1 , C_2 , C_3). While the traditional boost converter delivers voltage as expected, the non-coupled inductor/capacitor pairing contributes to producing greater output voltage. This inductor/capacitor pair is formed by inductors L_2 , L_3 , and capacitors C_2 , C_3 . Diode D_m is dedicated to freewheeling purposes.

2.2. Operation mode one (battery bypassed)

The first operation mode occurs when the supply voltage for V_1 and V_2 can satisfy the existing load. This mode of operation involves four switching states. Also, at this point, the battery is fully charged. The battery is cut off by turning off either pair of S_4 and D_{b1} or S_3 and D_{b2} . The switching states are described.

- Switching state 1 ($t_0 - t_1$): S_1 , S_2 and S_3 are turned on. S_4 stays turned off with D_{b1} to cut off the supply to the battery. The equivalent circuit is depicted in Figure 1(b). L_1 is charged by V_1 through S_1 . Similarly, L_2 is charged by V_2 through S_2 . C_3 charges L_3 and C_2 . C_1 is in the idle state. C_o serves the load during this switching state. D_o , D_1 , and D_m do not conduct.
- Switching state 2 ($t_1 - t_2$): The circuit is illustrated in Figure 1(c). S_1 is turned off while S_2 stays on, like previously. D_o conducts, hence L_1 and C_1 discharge in consonance with V_1 to deliver energy to the load.
- Switching state 3 ($t_2 - t_3$): The circuit is as shown in Figure 1(d). S_1 is turned on, S_2 and S_3 are turned off. S_4 and D_{b1} conduct. D_o is turned off while D_1 and D_m are conducted. L_1 is charged by V_1 . C_3 is charged by V_2 and L_2 . L_3 charges C_1 , and C_o serves the load.

Switching state 4 ($t_3 - T$): S_1 and S_2 are turned on. D_o is turned off. The components exhibit the same pattern as in switching state 1. C_o serves the load. The relevant equations are shown in (1)-(8). Where, d_1 is the duty ratio of switch S_1 ; d_2 is the duty ratio of switch S_2 ; V_{C1} is the voltage across capacitor C_1 ; V_{C2} is the voltage across capacitor C_2 ; V_{C3} is the voltage across capacitor C_3 ; T_s is the total period; V_o is the output voltage; and G_V is the voltage gain.

$$L_2: V_2 d_2 T_s + V_2 - V_{C3}(1 - d_2)T_s = 0 \quad (1)$$

$$L_2: V_2 d_2 T_s + V_2 + V_{C2} - V_{C1}(1 - d_2)T_s = 0 \quad (2)$$

$$L_1: V_1 d_1 T_s + V_1 + V_{C1} - V_o(1 - d_2)T_s = 0 \quad (3)$$

$$V_{C3} = \frac{2V_2}{1 - d_2} \quad (4)$$

$$V_{C2} = \frac{3V_2}{2 - 2d_2} \quad (5)$$

$$V_{C1} = \frac{3V_2}{2 - 2d_2} + \frac{2V_2}{1 - d_2} \quad (6)$$

$$V_o = \frac{V_1 + (V_{C1}(1 - d_1))}{1 - d_1} \quad (7)$$

$$G_V = \frac{V_o}{V} = \frac{1 + ((\frac{3}{2 - 2d_2} + \frac{2}{1 - d_2})(1 - d_1))}{1 - d_1} \quad (8)$$

2.3. Operation mode two (battery discharging)

In this operation mode, the load cannot be served by the RE sources alone. Hence, the battery storage, V_b is engaged to support the power delivered to the load. S_3 and S_4 play the role of allowing or disallowing the battery to deliver power to the load. S_3 is perpetually turned on during this operation mode. The respective switching states are described hereafter.

- Switching state 1 ($t_0 - t_1$): The circuit is represented in Figure 2(a). All switches are turned on. D_{b1} and D_{b2} are turned off. $V_b + V_1$ charges L_1 while $V_b + V_2$ charges L_2 . C_1 is idle. D_o and D_1 are off. C_o delivers power to the load.
- Switching state 2 ($t_1 - t_2$): The equivalent circuit is shown in Figure 2(b). S_1 is turned off while all other

switches stay on. $V_b + V_I + V_{C1}$ supplies power to the load via D_o .

- c. Switching state 3 ($t_2 - t_3$): The circuit is shown in Figure 2(c). S_3 and S_4 remain turned. V_b charges L_1 and L_2 .
- d. Switching state 4 ($t_3 - T$): Switching state 4 of operation mode 1 is replicated here. Relevant equations are shown in (9)-(17), where, d_4 is the duty ratio of switch S_4 ; i_b is the battery current; P_b is the battery power; i_{L1} is the current for inductor L_1 ; i_{L2} is the current for inductor L_2 ; and i_{L3} is the current for inductor L_3 .

$$L_2: V_2 d_2 T_s + V_b d_4 T_s - V_2 + V_b d_4 - V_{C3}(1 - d_2) T_s = 0 \quad (9)$$

$$L_2: V_2 d_2 T_s + V_b d_4 T_s + V_b d_4 + V_2 + V_{C2} - V_{C1}(1 - d_2) T_s = 0 \quad (10)$$

$$L_1: V_1 d_1 T_s + V_b d_4 - V_b d_4 + V_1 + V_{C1} - V_o(1 - d_1) T_s = 0 \quad (11)$$

$$i_b = d_4(i_{L1} + i_{L2} + i_{L3}) \quad (12)$$

$$P_b = V_b(d_4(i_{L1} + i_{L2} + i_{L3})) \quad (13)$$

$$V_{C3} = \frac{V_b(1+d_4)+V_2(1+d_2)}{1-d_2} \quad (14)$$

$$V_{C2} = \frac{V_2(2+d_2)+V_b(2-d_2+2d_4)}{2-2d_2} \quad (15)$$

$$V_{C1} = \frac{V_b(1+d_4)+V_2(1+d_2)}{1-d_2} + \frac{V_2(2+d_2)+V_b(2-d_2+2d_4)}{2-2d_2} \quad (16)$$

$$V_o = \frac{V_1+(V_b(1-d_1+d_4))+(V_{C1}(1-d_1))}{1-d_1} \quad (17)$$

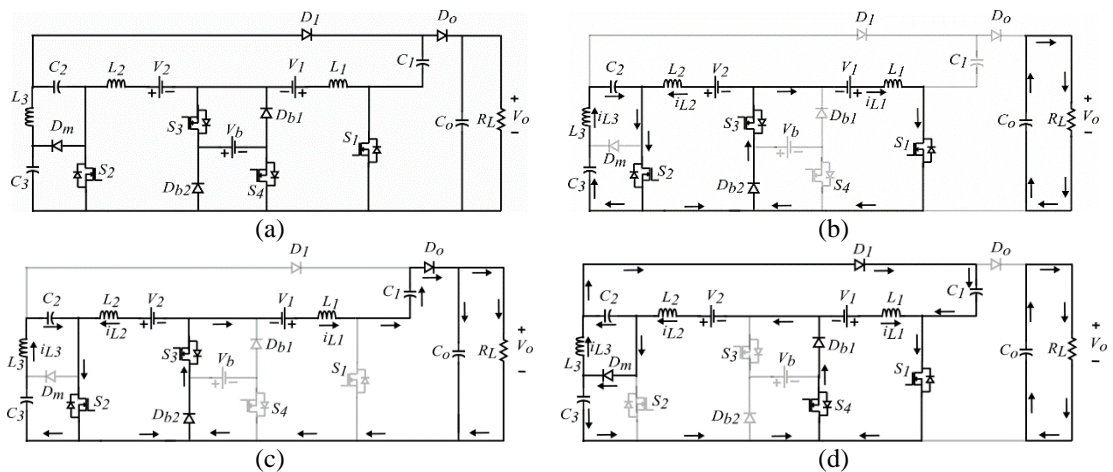


Figure 1. Proposed converter and operation mode 1 current paths (a) proposed converter, (b) switching state 1, (c) switching state 2, and (d) switching state 3

2.4. Operation mode three (battery charging)

In this working mode, the battery state of charge (SOC) is low, and the RE sources have the capacity to charge the battery while serving the load. Switch S_4 regulates the charging of the battery. S_3 is turned off during this operation mode. The switching modes are described:

- a. Switching state 1 ($t_0 - t_1$): Switching state 1 of operation mode one is replicated here. No battery charging.
- b. Switching state 2 ($t_1 - t_2$): Switching state 2 of operation mode one is repeated here. No battery charging.
- c. Switching state 3 ($t_2 - t_3$): The circuit is shown in Figure 2(d). Only S_2 is turned on. D_{b1} and D_{b2} conduct. V_b is charged along with C_3 by both V_1 , V_2 , and energy is discharged from L_2 . C_o deliver power to the load.
- d. Switching state 4 ($t_3 - T$): Switching state 4 of the first operation mode is replicated. No battery charging. The equations are shown in (18)-(26).

$$L_2: V_2 d_2 T_s - (V_2 - V_{C3} - V_b(1 - d_4))(1 - d_2) T_s = 0 \quad (18)$$

$$L_2: V_2 d_2 T_s + V_2 + V_{C2} - V_{C1}(1 - d_2) T_s = 0 \quad (19)$$

$$L_1: V_1 d_1 T_s - V_b(d_1 - d_4) - V_1 + V_{C1} - V_o(1 - d_1)T_s = 0 \quad (20)$$

$$i_b = i_{L1}(d_1 - d_4) + i_{L2} + i_{L3}(d_2 - d_4) \quad (21)$$

$$P_b = V_b(i_{L1}(d_1 - d_4) + i_{L2} + i_{L3}(d_2 - d_4)) \quad (22)$$

$$V_{C3} = \frac{V_2 + V_b(1 - d_2 + d_4 + d_2 d_4)}{1 - d_2} \quad (23)$$

$$V_{C2} = \frac{V_2 + V_{C3}(1 - d_2)}{2 - 2d_2} \quad (24)$$

$$V_{C1} = \frac{V_2 + \frac{V_2 + V_b(1 - d_2 + d_4 + d_2 d_4)}{1 - d_2}}{2 - 2d_2} + \frac{V_2 + V_b(1 - d_2 + d_4 + d_2 d_4)}{1 - d_2} \quad (25)$$

$$V_o = \frac{V_1 + (V_b(d_1 - d_4)) + (V_{C1}(1 - d_1))}{1 - d_1} \quad (26)$$

Figure 3(a) shows the switching pattern for operation mode one. The switching patterns for modes two and three are depicted in Figure 3(b) and Figure 3(c), respectively. The waveforms of the inductor currents and capacitor voltages are shown in Figure 3(d).

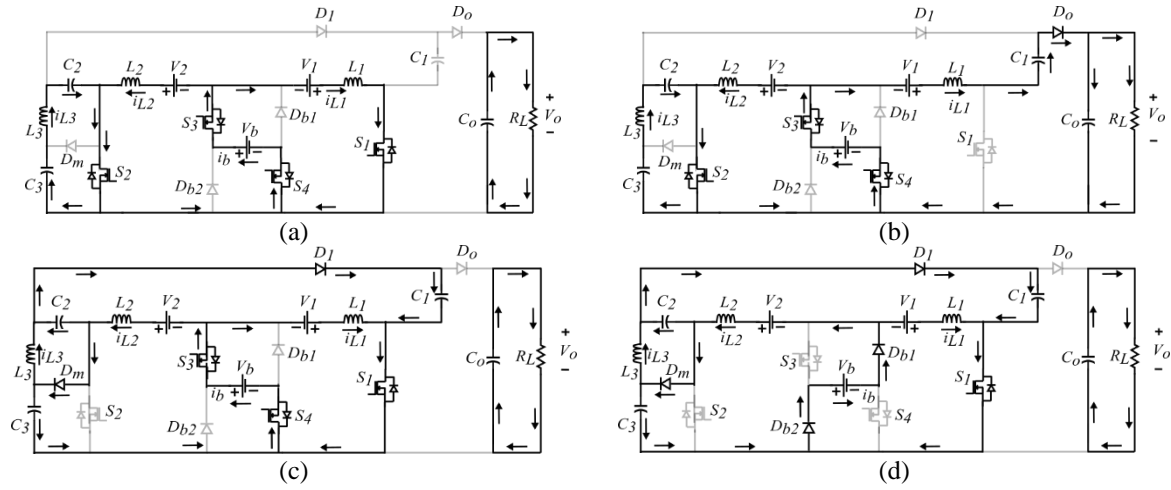


Figure 2. Current paths for operation modes 2 and 3 (a) switching state 1, (b) switching state 2, (c) switching state 3, and (d) switching state 3 of operation mode 3

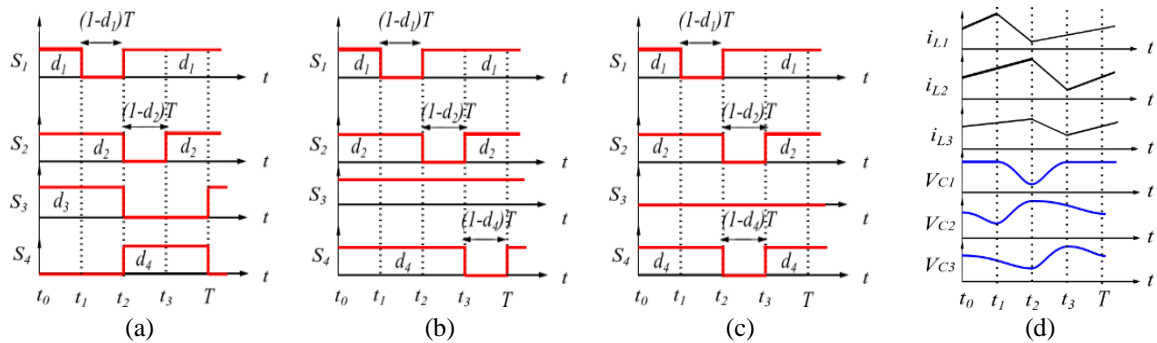


Figure 3. Key waveforms (a) mode 1, (b) mode 2, (c) mode 3, and (d) i_{L1} , i_{L2} , i_{L3} , V_{C1} , V_{C2} & V_{C3}

2.5. Design of inductors and capacitors

The design of the inductors is akin to that of the conventional boost converter. To ensure continuous conduction mode (CCM), the inductor average current must be greater than half of the inductor ripple current. Hence, for inductors L_1 and L_2 .

$$I_{L1} \geq \frac{\Delta i_{L1}}{2}, I_{L2} \geq \frac{\Delta i_{L2}}{2} \quad (27)$$

By applying ampere-second balancing on the respective capacitors, the average current of L_1 and L_2 is I_{L1} and I_{L2} , respectively. These depend on the output current, I_o , and duty ratio of the switches and are expressed as (28).

$$I_{L1} = \frac{2I_o}{1-d_1}, I_{L2} = \frac{4I_o}{1-d_2} \quad (28)$$

The inductor currents of the boost and non-coupled inductor sides of the converter, are shown by (27) and (28), can be controlled by varying d_1 and d_2 , respectively. In addition, the average current of L_3 is the same as the output current of the converter.

In calculating the minimum value of the inductors, the second operation mode is to be considered. This is because V_1 and V_2 generate the lowest energy in this mode. Such a scenario could result in the converter operating in discontinuous conduction mode (DCM). The inductors' current ripples in the second operation can be found as in (29).

$$\Delta i_{L1} = \frac{d_1 V_1 + d_4 V_b}{L_1 f_s}, \Delta i_{L2} = \frac{d_2 V_2 + d_4 V_b}{L_2 f_s} \quad (29)$$

Hence, the values of the inductors, L_1 , L_2 , and L_3 , can be obtained as (30).

$$L_1 \geq \frac{d_1 V_1 + d_4 V_b}{\Delta i_{L1} f_s}, L_2 = L_3 \geq \frac{d_2 V_2 + d_4 V_b}{\Delta i_{L2} f_s} \quad (30)$$

It can be seen from (29) and (30) that the required inductance reduces when the switching frequency, f_s , is increased. In practice, the higher inductance values are applied to reduce the inductor ripple current.

In order to properly design the converter, it is essential that the voltage and current stress of the semiconductor devices are taken into cognizance. The voltage stress of the device is also known as peak inverse voltage. It is the maximum voltage encountered by the device without being destroyed when it is turned off. During CCM, the voltage stress and current stress of the devices are given in Table 1. It is vital that the capacitors, C_o , C_1 , C_2 , and C_3 can permit a change in the charge and voltage variations during their respective charging ranges. To ensure CCM, the inductor average current must be greater than half of the inductor ripple current. The capacitances can be obtained by (31).

$$C_1 \geq \frac{2i_o}{f_s(1-d_1)\Delta V_{C1}}, C_2 = C_3 \geq \frac{i_{L2}-i_o}{f_s(1-d_1)\Delta V_{C2,3}}, C_o \geq i_o \frac{d_1}{f_s \Delta V_{Co}} \quad (31)$$

Table 1. Voltage and current stress of the devices

Device	Voltage stress	Device	Current stress
S_1, D_1	$V_o - V_{C1}$	S_1	$I_{L1max} + I_{L2max}$
S_2, D_m	V_{C3}	S_2	$I_{L2max} + I_{L3max}$
D_2	$V_o - V_{C1} + V_{C3}$	S_3, D_3	$I_{L1max} + I_{L2max} + I_{L3max}$
S_3, S_4, D_3, D_4	V_{FD}	D_1	I_{L1}
		D_2	$I_{L2} + I_{L3}$
		D_m	$I_{L2} + I_{L3} - I_{L1}$

2.6. Dynamic model of the converter

The first operation mode uses two active-duty ratios (d_1 , d_2), while the second and third operating modes use three alternate duty ratios (d_1 , d_2 , d_4). The topology description indicates that there are seven passive elements in the proposed converter. These are L_1 , L_2 , L_3 , C_1 , C_2 , C_3 , and C_o . There are six state variables adopted. These are L_1 , L_2 , C_1 , C_2 , C_3 , and C_o .

In performing small-signal modelling, it is assumed that two components make up the state variables, duty ratios, and input voltages [28]. These are perturbations (\tilde{x} , \tilde{d} , \tilde{v}) and dc values (\bar{X} , \bar{D} , \bar{V}) expressed as in (32).

$$x = \bar{X} + \tilde{x}; d = \bar{D} + \tilde{d}; v = \bar{V} + \tilde{v} \quad (32)$$

By ignoring the second-order elements and assuming that the perturbations are modest and do not change dramatically over the course of a single switching period, small-signal models are produced. The small-signal models in matrix form are as in (33).

$$\dot{x} = A\tilde{x} + B\tilde{u}, y = C\tilde{x} + D\tilde{u} \quad (33)$$

In (33), \tilde{x} is the state variable vector, \tilde{u} is the control variables vector and \tilde{y} is the output vector. The matrix forms of the small-signal models are presented. For the first operation mode, the small-signal model is (34) and (35).

$$A = \begin{bmatrix} 0 & 0 & \frac{1-\bar{D}_1}{L_1} & 0 & 0 & \frac{\bar{D}_1-1}{L_1} \\ 0 & 0 & 0 & 0 & \frac{\bar{D}_2-1}{L_2} & 0 \\ \frac{1-\bar{D}_2}{c_1} & \frac{1-\bar{D}_2}{c_1} & 0 & 0 & 0 & \frac{2-2\bar{D}_1}{R_L c_1} \\ \frac{\bar{D}_2}{c_2} & \frac{2\bar{D}_2-2}{c_2} & 0 & 0 & 0 & 0 \\ -\frac{\bar{D}_2}{c_3} & \frac{1-\bar{D}_2}{c_3} & 0 & 0 & 0 & 0 \\ \frac{2-2\bar{D}_1}{c_o} & 0 & 0 & 0 & 0 & -\frac{1}{R_L c_o} \end{bmatrix}, B = \begin{bmatrix} \frac{\bar{V}_O - \bar{V}_{C1}}{L_1} & 0 \\ 0 & \frac{\bar{V}_{C3}}{L_2} \\ \frac{\bar{I}_{L1}}{2c_1} & \frac{\bar{I}_{L2} - \bar{I}_{L1}}{c_1} \\ 0 & \frac{2\bar{I}_{L2}}{c_2} \\ 0 & -\frac{\bar{I}_{L2}}{c_3} \\ -\frac{\bar{I}_{L1}}{c_o} & 0 \end{bmatrix} \quad (34)$$

$$C = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}, \tilde{x} = \begin{bmatrix} \tilde{I}_{L1} \\ \tilde{I}_{L2} \\ \tilde{V}_{C1} \\ \tilde{V}_{C2} \\ \tilde{V}_{C3} \\ \tilde{V}_o \end{bmatrix}, \tilde{u} = \begin{bmatrix} \tilde{d}_1 \\ \tilde{d}_2 \end{bmatrix}, D = 0 \quad (35)$$

For the second operation mode, the small-signal model is (36) and (37).

$$A = \begin{bmatrix} 0 & 0 & \frac{1-\bar{D}_1}{L_1} & 0 & 0 & \frac{\bar{D}_1-1}{L_1} \\ 0 & 0 & 0 & 0 & \frac{\bar{D}_2-1}{L_2} & 0 \\ \frac{1-\bar{D}_2}{c_1} & \frac{1-\bar{D}_2}{c_1} & 0 & 0 & 0 & \frac{2-2\bar{D}_1}{R_L c_1} \\ \frac{\bar{D}_2}{c_2} & \frac{2\bar{D}_2-2}{c_2} & 0 & 0 & 0 & 0 \\ -\frac{\bar{D}_2}{c_3} & \frac{1-\bar{D}_2}{c_3} & 0 & 0 & 0 & 0 \\ \frac{2-2\bar{D}_1}{c_o} & 0 & 0 & 0 & 0 & -\frac{1}{R_L c_o} \end{bmatrix}, B = \begin{bmatrix} \frac{\bar{V}_O - \bar{V}_{C1}}{L_1} & 0 & \frac{2\bar{V}_B}{L_1} \\ 0 & \frac{\bar{V}_{C3}}{L_2} & \frac{\bar{V}_B}{L_2} \\ \frac{\bar{I}_{L1}}{2c_1} & \frac{\bar{I}_{L2} - \bar{I}_{L1}}{c_1} & 0 \\ 0 & \frac{2\bar{I}_{L2}}{c_2} & 0 \\ 0 & -\frac{\bar{I}_{L2}}{c_3} & 0 \\ -\frac{\bar{I}_{L1}}{c_o} & 0 & 0 \end{bmatrix} \quad (36)$$

$$C = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}, \tilde{x} = \begin{bmatrix} \tilde{I}_{L1} \\ \tilde{I}_{L2} \\ \tilde{V}_{C1} \\ \tilde{V}_{C2} \\ \tilde{V}_{C3} \\ \tilde{V}_o \end{bmatrix}, \tilde{u} = \begin{bmatrix} \tilde{d}_1 \\ \tilde{d}_2 \\ \tilde{d}_4 \end{bmatrix}, D = 0 \quad (37)$$

For the third operation mode, the small-signal model is (38) and (39).

$$A = \begin{bmatrix} 0 & 0 & \frac{1-\bar{D}_1}{L_1} & 0 & 0 & \frac{\bar{D}_1-1}{L_1} \\ 0 & 0 & 0 & 0 & \frac{\bar{D}_2-1}{L_2} & 0 \\ \frac{1-\bar{D}_2}{c_1} & \frac{1-\bar{D}_2}{c_1} & 0 & 0 & 0 & \frac{2-2\bar{D}_1}{R_L c_1} \\ \frac{\bar{D}_2}{c_2} & \frac{2\bar{D}_2-2}{c_2} & 0 & 0 & 0 & 0 \\ -\frac{\bar{D}_2}{c_3} & \frac{1-\bar{D}_2}{c_3} & 0 & 0 & 0 & 0 \\ \frac{2-2\bar{D}_1}{c_o} & 0 & 0 & 0 & 0 & -\frac{1}{R_L c_o} \end{bmatrix}, B = \begin{bmatrix} \frac{\bar{V}_O - \bar{V}_{C1} - \bar{V}_B}{L_1} & 0 & \frac{\bar{V}_1 - \bar{V}_B}{L_1} \\ 0 & \frac{\bar{V}_2}{L_2} & \frac{\bar{V}_2 - \bar{V}_{C3} - \bar{V}_B}{L_2} \\ \frac{\bar{I}_{L1}}{2c_1} & \frac{\bar{I}_{L2} - \bar{I}_{L1}}{c_1} & 0 \\ 0 & \frac{2\bar{I}_{L2}}{c_2} & 0 \\ 0 & -\frac{\bar{I}_{L2}}{c_3} & 0 \\ -\frac{\bar{I}_{L1}}{c_o} & 0 & 0 \end{bmatrix} \quad (38)$$

$$C = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}, \tilde{x} = \begin{bmatrix} \tilde{L}_{L1} \\ \tilde{L}_{L2} \\ \tilde{v}_{C1} \\ \tilde{v}_{C2} \\ \tilde{v}_{C3} \\ \tilde{v}_o \end{bmatrix}, \tilde{u} = \begin{bmatrix} \tilde{d}_1 \\ \tilde{d}_2 \\ \tilde{d}_4 \end{bmatrix}, D = 0 \quad (39)$$

2.7. Power management algorithm of the converter

It is crucial to create an algorithm to choose the proper operation mode for hybrid MICs. The first input port is the PV port, and the second input port is the FC port. The operation scenarios could happen if the PV produces insufficient electricity or if the load requirements are higher. As long as there is enough power in the battery storage and any of the input sources, the proposed converter should be able to handle the load.

Determining the minimal power levels necessary for the converter modes to function properly is crucial. The lowest power from the PV (P_{PV}) and the power from the FC (P_{FC}) are identified. Also, upper and lower SOC references (B_L and B_U) are identified for the battery. The load power requirement, P_L , is considered. Figure 4 shows the proposed algorithm for energy management. It is important to note that the operating logic in Figure 4 handles how an operation mode is chosen in the first instant. Switching between operation modes will depend on a monitoring circuit and battery management system, which are not within the scope of this study.

The process for managing power is explained:

- When there is a reduced load, P_L is contrasted with either P_{PV} and P_{FC} or $P_{PV} + P_{FC}$. P_{PV} is given priority in the algorithm. The SOC is examined to see if it is more than B_U if P_{PV} is able to meet the load, P_L . The first operation mode kicks in when the SOC exceeds the B_U and bypasses the battery.
- When P_{PV} , P_{FC} , or $P_{PV} + P_{FC}$ cannot serve the load, the algorithm checks the SOC status. If $SOC > B_U$, the second operation mode is adopted and the battery discharges. It further checks if $SOC < B_L$. So long as $SOC > B_L$, the battery discharging mode continues. If $SOC < B_L$, the algorithm returns to the start position or command.
- As can be seen from the algorithm, the third operation mode is adopted when P_{PV} , P_{FC} or $P_{PV} + P_{FC}$ is greater than P_L and $SOC < B_L$.

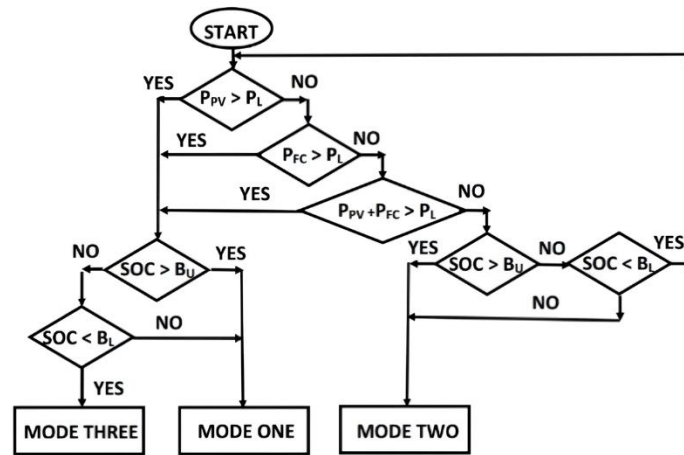


Figure 4. Algorithm for power management of the proposed converter

3. RESULTS AND DISCUSSION

In this section, the results will be presented. The output voltage range will also be established. Finally, the proposed converter will be compared with similar previous investigations.

3.1. Experimental results

In validating the performance of the proposed converter, a hardware prototype has been implemented as depicted in Figure 5(a). RE sources, V_1 at 12 V, and V_2 at 24 V, were replicated by DC power supplies, while a 12 V rechargeable lead acid battery sufficed as the energy storage device. The dSPACE DS1104 digital controller board was used to generate the switching pulses for all the switches. In accordance with the derived equations, the other component ratings are chosen as listed in Table 2. Switches

S_1 to S_4 are Infineon G25H1203 IGBTs, while the diodes are Cheng-Yi IN5400 axial silicon rectifier diodes. Based on (30), the critical inductances at a chosen frequency of 15 kHz and 10 % ripple, $L_1 \geq 300.6$ mH, $L_2 = L_3 \geq 157.6$ mH are obtained. Consequently, $L_1 = 350$ mH, $L_2 = L_3 = 200$ mH are selected. For the capacitors, using (31) with permitted voltage ripple of 1%, $C_1 \geq 78.1$ μ F, $C_2 \geq 42.5$ μ F, $C_3 \geq 31.8$ μ F, and $C_o \geq 50$ μ F are selected. Hence, $C_1 = C_2 = C_3 = 100$ μ F (100 μ F, 400 V, Elite PF2G101MNN1832). The output capacitor, $C_o = 270$ μ F (270 μ F 400 V, Nichicon LGL2G271MELZ35).

At duty ratios of 0.75 and 0.7 for d_1 and d_2 , respectively, the output voltage obtained in mode one is 315.53 V. Figure 5(b) shows V_1 , V_2 , and V_o during operation mode one. The duty ratios of S_3 and S_4 are set to 0.5 each. The capacitor voltages, V_{C1} , V_{C2} , and V_{C3} are shown in Figure 5(c). It can be seen that the voltages are 127.19 V for V_{C2} , 139.54 V for V_{C3} . V_{C1} is 266.69 V and is the sum of V_{C2} and V_{C3} . C_1 is idle during the switching states 1 and 3. The waveforms of the inductor currents are presented in Figure 5(d). When S_1 and S_2 are conducting during the first switching state, i_{L1} and i_{L2} increase linearly as a result of the L_1 and L_2 being charged by V_1 and V_2 , respectively. At t_2-t_1 , i_{L1} decreases while i_{L2} and i_{L3} continue increasing. Inductor currents, i_{L2} and i_{L3} , linearly decrease with a negative slope during the third switching state when S_2 does not conduct, while i_{L1} increases for two consecutive switching states. The approximate inductor currents are 2.12 A, 4.23 A, and 0.305 A for i_{L1} , i_{L2} , and i_{L3} , respectively.

Table 2. Experimental parameters

Parameter	Value/part number	Parameter	Value/part number
Input voltage	$V_1 = 12$ V, $V_2 = 24$ V, $V_b = 12$ V	Capacitors	$C_o = 270$ μ F, $C_1, C_2, C_3 = 100$ μ F
Frequency	15 kHz	Diodes	20 A10 20 A 1000 V
Power switch	Infineon G25H1203 IGBT	Load	1000
Inductors	$L_1 = 350$ mH, $L_2, L_3 = 200$ mH		

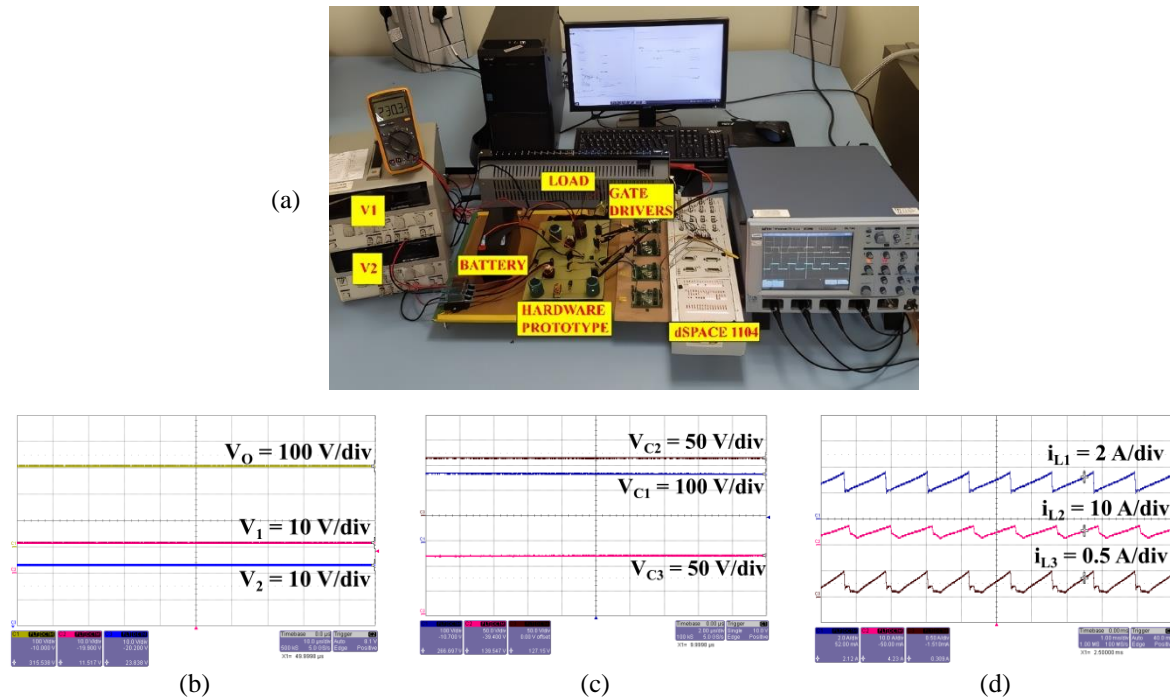


Figure 5. Operation mode 1 results: (a) setup, (b) V_1 , V_2 & V_o (c) V_{C1} , V_{C2} & V_{C3} , and (d) i_{L1} , i_{L2} & i_{L3}

The output voltage of the second operation mode is shown in Figure 6(a). V_1 and V_2 have been reduced to 6 V and 12 V, respectively. Duty ratios of 0.75, 0.7, and 0.75 for d_4 , d_2 and d_1 have been applied. The output voltage is 311.57 V. Since the same switching pattern is applied to S_1 and S_2 in all three operation modes, the inductor currents (i_{L1} , i_{L2} , i_{L3}), output current, capacitor voltages, switch voltage stress, V_{S1} and V_{S2} , for all the modes differ only in magnitude and not by waveform. The waveforms of i_{L1} and i_{L2} are shown in Figure 6(b). The voltage stress on S_3 and S_4 are shown in Figure 6(c). V_{S4} is equal to the battery supply voltage, $V_b = 12$ V. V_{S3} is the forward voltage of 0.8 V. The battery current, i_b is displayed in Figure 6(d). It rises to about 5.49 A during the first three switching states and drops in the last state. It is the product of the duty ratio of switch S_4 by the summation of the inductor currents.

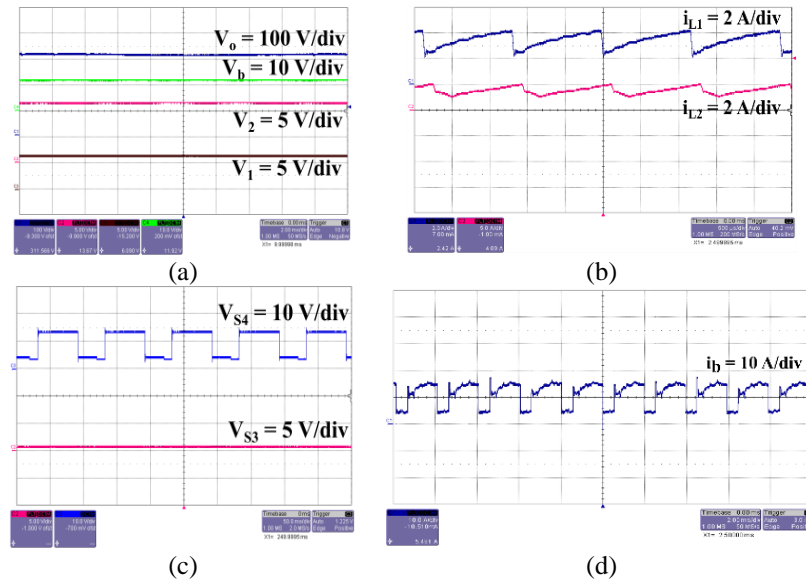


Figure 6. Operation mode 2 results (a) V_1 , V_2 , V_b & V_o , (b) i_{L1} & i_{L2} , (c) V_{S3} & V_{S4} , and (d) i_b

For the third operation mode, the duty ratio, d_4 is set to 0.75. The measured output voltage is about 301.32 V. Figure 7(a) shows the output voltage and the voltage on C_1 . The voltage on C_1 is about 277.69 V. While the converter serves the load, the battery is charged during the third switching state when there is a negative slope on the signal. The voltage stress of the switches is shown in Figure 7(b). It can be observed that the appearance of the voltage across S_1 occurs during the second switching state and during the switching state for S_2 . The voltage stresses, V_{S1} and V_{S2} , across S_1 and S_2 are about 64.87 V and 119.54 V, respectively.

The voltage stress on S_3 and S_4 is depicted in Figure 7(c). V_{S3} goes to zero in the third switching state and returns to about 10 V, which is the voltage of the depleted battery. The voltage spike in V_{S3} occurs during switching state three when turning off S_3 and S_4 forces the current to charge the V_b through diodes, D_{b1} and D_{b2} . The i_{L1} , i_{L2} , and i_b are shown in Figure 7(d). It indicates a spike in i_b to about 1 A when D_{b1} and D_{b2} conduct.

The experimentally measured output voltage range was measured. At $V_1 = 12$ V, $V_2 = 24$ V, the duty ratio $d_1 = d_2 = d$, was varied from 0.05 to 0.75. The output voltage ranges between 84 V and 381 V. The lowest voltage of 21.4 V was recorded when V_1 is isolated at a 0.05 duty ratio. This confirms the wide output voltage range of the proposed converter.

3.2. Comparison with similar topologies

Table 3 shows a comparison of the proposed converter with similar topologies. Each of the compared converters has two input ports in addition to a battery port. The voltage gain and the number of components have been compared. The converters' voltage boosting method has been established. The three-input version of the MIC in [25] is considered. Although the proposed converter appears to have more capacitors than the others, the capacitors on the non-coupled inductor side of the converter help to enhance the high output voltage delivery.

The converter by [26] shows a smaller voltage gain than the proposed converter, despite boasting lower total component counts. The [25] claimed a large voltage gain, however, this can also be attributable to the maximum component count. Therefore, it can be speculated that [25] will have the highest cost. In conducting a cost comparison between the proposed converter and the contemporary converters, the price estimates of the reported components of each converter have been culled from the Mouser website. For the reported converters, [25] has been confirmed to have the highest cost, while [26] has the lowest cost. The cost of the proposed converter is lower than that of [25] but is 31.6 % higher than [26]. It should be noted that the voltage output of [26] is lower than that of the proposed converter.

The converter proposed in [24] has the lowest voltage gain and the second-highest parts count. The [27] system, in comparison, has a high voltage gain while having the fewest parts, a tie with [26]. Due to the high voltage stress on the semiconductor devices and the large number of passive parts (mostly resistors) in the converter described by [26], [27]. These converters have high losses. The output voltage during the operation mode 2 has been computed for the compared converters. It can be concluded that the proposed converter delivered the highest output voltage during the battery discharging operation mode.

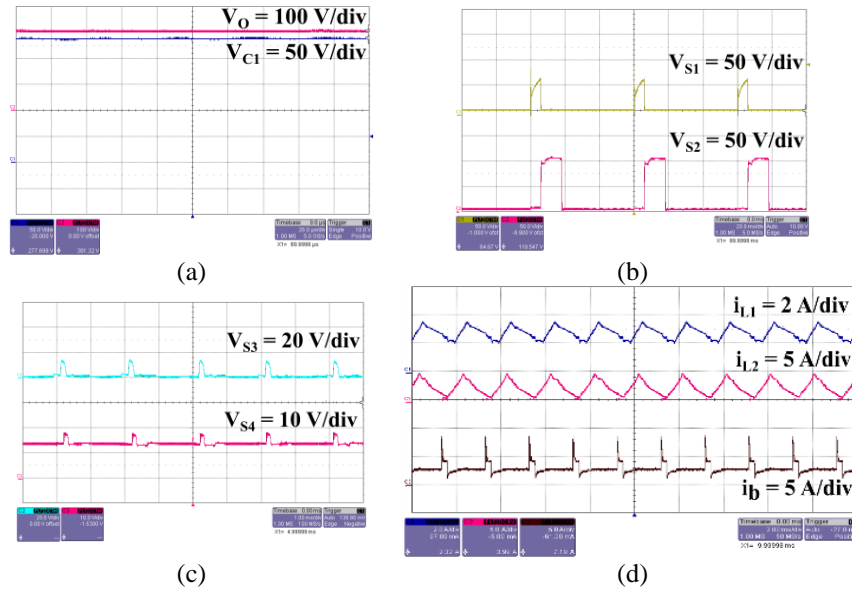


Figure 7. Operation mode 3 results (a) V_o & V_{C1} , (b) V_{S1} & V_{S2} , (c) V_{S3} & V_{S4} , and (d) i_{L1} , i_{L2} & i_b

Table 3. Comparison between the proposed converter and similar topologies

Three inputs converter	Switch count	Inductor count	Capacitor count	Diode count	Total count	Voltage gain	$V_{o,mode2}$, $V = 12$ V, $d = 0.7$	Total cost
Boost/ switched capacitor-inductor [24]	5	5	5	7	22	$\frac{1}{1-d}$	226.66 V	Not reported
Switched inductor [25]	4	4	3	10	23	$\frac{1+2d}{(1-d)}$	102.45 V	\$ 97.32
Buck-boost/ Boost [26]	4	2	2	4	12	$\frac{1+d^2-d}{(1-d)^2}$	198.66 V	\$39.25
Boost/ boost [27]	4	2	2	4	12	$\frac{1+d}{(1-d)^2}$	161.33 V	Not reported
This work is Boost/non-coupled inductor	4	3	4	5	16	$\frac{9}{2(1-d)}$	324 V	\$ 51.67

4. CONCLUSION

In this paper, a battery-integrated three-input high-gain converter has been presented. The topology is based on the non-coupled inductor/ boost technique. The cor

merit of the converter is high voltage gain in the battery bypassed and battery discharging modes due to the non-coupled inductor topology. There is also a wide output voltage range. The battery port makes it suitable for RE applications. The operation modes have been defined. The output voltages in all modes are derived in the same way as the inductor/battery currents and voltage stresses. A power management algorithm has been proposed to switch the converter between working states, dependent on the available RE sources. The proposed converter can serve PV/FC and battery inputs. The experimental results conform to the theoretical analysis of the converter. Future research may focus on mitigating losses associated with voltage stresses and current spikes during converter operation while maintaining the advantage of high voltage gain. Also, a model predictive control and battery management system could be investigated.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration. Azuka Affam conceptualized the idea

while all authors were involved in the methodology. Yonis M. Yonis Buswig and Azuka Affam carried out the software simulations and experiments and also responsible for data curation. Hazrul Mohamed Basri and Al-Khalid Othman did the validation. Formal analysis and investigation were majorly executed by Azuka Affam and Yonis M. Yonis Buswig with assistance from Norhuzaimin Julai and Hazrul Mohamed Basri. Resources were handled by Yonis M. Yonis Buswig, Al-Khalid Othman, Shanti Faridah Salleh, and Hazrul Mohamed Basri. Azuka Affam took the lead in writing the manuscript. Review and editing of the manuscript were led by Shanti Faridah Salleh, Kasumawait Lias and Al-Khalid Othman. Finally, Yonis M. Yonis Buswig, Al-Khalid Othman, Shanti Faridah Salleh, and Noruzaimin Julai were responsible for supervision, project administration, and funding acquisition. These details are presented in the table below.

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
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C : Conceptualization

M : Methodology

So : Software

Va : Validation

Fo : Formal analysis

I : Investigation

R : Resources

D : Data Curation

O : Writing - Original Draft

E : Writing - Review & Editing

Vi : Visualization

Su : Supervision

P : Project administration

Fu : Funding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

Derived data supporting the findings of this study are available from the corresponding author, [AA], upon request.




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