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System-on-chip design for improved switching angle driven 35-level LUO progression-based multi-level inverter

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ABSTRACT

This article concentrates on the development of the IC layout for the driving switches of the inverter with improved switching control. This work uses the improved non-carrier switching pattern algorithms to have precise control of inverter switches with twin objectives of i) reducing the total harmonic distortion (THD)% and ii) developing a dedicated system on chip for the improved switching control of the 35-level switched ladder multi-level inverter. The DC voltage of the inputs to the inverter is designated based on the LUO progression, which consists of an improved mathematical formula for deriving its values. Conventionally, the multi-level inverter circuits are driven by the pulse width modulation signals by overlapping the modulating sine wave with different levels of triangle waves, such as phase disposition, phase opposite disposition, and alternate phase opposite disposition, utilized to drive various voltage source inverter topologies. Although the MLI design concentrates on minimal THD%, factors like accuracy, minimum number of switches, and cost demands for advanced switching strategy algorithms. This paper compares the improved switching angle method to the existing algorithm by considering V_{PEAK}, $V_{RMS,}$ and %THD for the 35-level LUO progression-based switched ladder inverter. The IC layout for the improved switching control is developed using the hardware description language code in the Cadence tool and validated by cross-compiling in Simulink MATLAB.

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1. INTRODUCTION

Inverters contribute to the generation of AC output by making use of power electronic circuits. The circuit topology of the inverter consists of DC sources and switches that are controlled by the drive. The multi-level inverter (MLI) circuit performance is dependent on the number of switches used in the topology, with less total harmonic distortion (THD)% [1]-[3]. The multi-level inverter topology with symmetric and asymmetric DC values has minimum cost [4]. The increased cost can be eradicated by an asymmetrical structure that gives large voltage levels with minimum switches [5]. The minimization in the switch count triggers the decrease of switching losses and the cost of the topology [6].

Conventionally, the drive for the switches involves pulse width modulation (PWM) signals for the generation of AC output. The PWM signals are generated with a low frequency to compensate for the complexity of the switching patterns [7]. The parameters of the inverter switches are manipulated mathematically to compare with the different topologies of the MLI [8].

The THD% evaluation is pivotal for the validation of any MLI topology. The reduction in the THD% of the inverter is compared with the LS and PS-based SPWM generation to implement the MLI using the lesser

switches AC output for the MLI levels is possible for both symmetrical and asymmetrical DC sources by using the double source double diode double switch [9]. The asymmetrical MLI topology can achieve high levels in the output, however, the complexity in the circuit topology demands separate voltage sources with the increase in cost [10]. Although there is a tiny reduction in the THD% with the CHB compared to the TCHB topology, the CHB topology goes under twice the stress in switching as the TCHB [11]. The selection of switches with its count and the optimized calculation of the switching angles for the MLI exhibits lower THD% [12].

Recently, there have been several inclusions and modifications in the MLI topology seeking a specified parameter. By making use of a level shifter in the fusion of cross cross-connecting switch inverter (CCSI) and a modified multilevel inverter (MMLI), higher levels of AC output were achieved [13]. The MLI with only one voltage source and a capacitor attains high voltage levels with low distortion in the harmonics [14]. The positional modification of the DC inputs will reduce the current harmonics in the MLI output [15]. The peak input energy can be harvested with a multi-input dual-output MLI topology [16]. The addition of a switch capacitor has been advantageous in the of lower ripples, lower switch count, and improved voltage gain for the hybrid-based MLI [17]. The ability to reduce the amplitude of the harmonics is achieved by the spectrum distribution in the MLI circuit and finds applications in communication and defense equipment, and heavy vehicles [18], [19].

The inclusion of the integrated boost flyback converter enhances the 31-level MLI to be efficient [20]. The fault tolerance in the MLI circuit is enhanced by the addition of redundant switches. The merit of this addition is the ability to identify multiple faults without affecting the performance of the power inverter. [21]. The use of switches with high frequency in positive levels and voltage reversed in negative levels of the MLI observed that the loss of 50% in THD% is the same as the specified output voltage [22]. The modulation-based PWM is involved in the generation of the AC output to emphasize the fluctuations and flicker in the MLI [23]. The advent of FPGA with the switching control of the MLI circuit is essential to generate the AC output with low cost and lower THD%. The accuracy and speed of switching in the MLI circuits are improved when implemented using the FPGA device [24]. The FPGA device usage in the control of cascaded MLI reduces the THD% and eliminates 3rd and 5th harmonics. This paper proposes an improved switching angle algorithm with the state of charge (SOC) layout for the 35-level LUO-based progression switched ladder inverter.

2. PROPOSED METHOD: IC LAYOUT FOR THE PROPOSED 35-LEVEL LUO PROGRESSION-BASED MULTI-LEVEL INVERTER

The proposed method concentrates on the generation of the IC layout plan for the switching patterns of the multi-level inverter (MLI) generated by the use of an improved non-carrier switching angle method. in this work, the switch patterns are produced for the MLI that has its input DC values based on the LUO progression. The LUO progression-based MLI topology consists of 14 switches to be driven to generate the AC output. The challenge lies in the precise patterning of these switches as required for the AC generation. The design flow for the proposed method is depicted in Figure 1. The proposed method could generate any level of MLI from 3 to 81. In this work, the 35-level LUO progression-based MLI is used to generate the AC output. The LUO progression-based MLI uses the power circuitry topology as given in Figure 2. The LUO progression-based multi-level inverter uses the formula as given in (1) and (2).

$$V_i = i, \quad \text{if} \quad i \leq 2; \tag{1}$$

$$= 7 \text{ X } 3^{i-2}, \text{if } i \geq 3 \tag{2}$$

Where Vi is the input voltages of the LUO progression inverter.

For the 35-level LUO progression-based MLI circuit, the voltage sources of 1 V, 2 V, 7 V, and 21 V are used to give 17 positive levels, 17 negative levels, and 1 zero level for the AC output. The level voltages combined for the generation of AC output are given in Table 1. The algorithm utilizes an improved non-carrier angle evaluation method to derive the levels of the multi-level inverter. In this work, the angles are produced based on the improved Half Height Event manipulation method which can present the angles in sequence till the half and in alternate sequence after the half of the positive and negative cycles with an addition of Integer value '1'. The equation for the HHM algorithm is given in (3).

$$\alpha_i = sin^{-1}\left[\left(\left(i - \frac{1}{2}\right)\frac{2}{m-1}\right) + 1\right] \tag{3}$$

Where i = 1,2,….$\frac{m-1}{2}$.

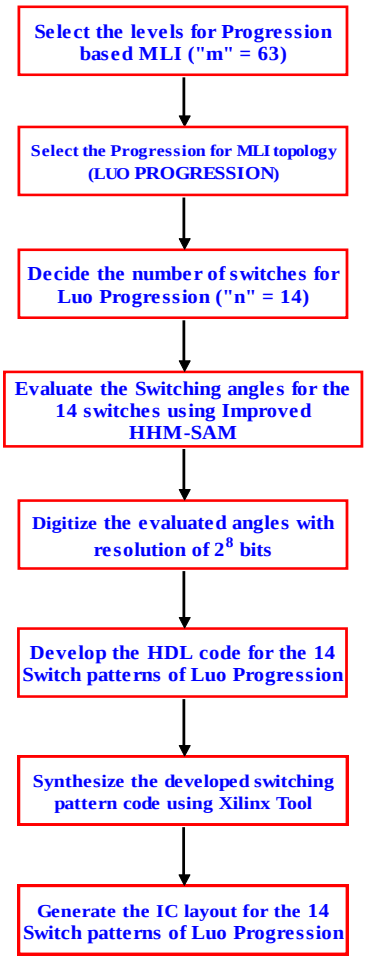

Figure 1. Design flow for the proposed 35-level LUO progression-based SLI

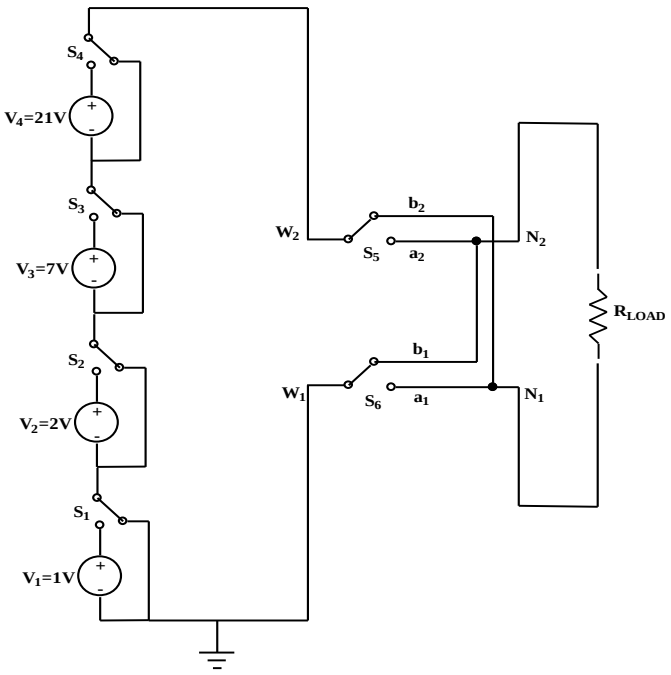

Figure 2. Circuit diagram for the LUO progression-based switched ladder multi-level inverter

The (3) presented formula is manipulated in the floating point for the angles. These angles are translated into digital values with 2^8 resolutions. The x-axis angles from 0° to 360° of a cycle are converted as 0 to 255 bits in digital format. The LUO progression-based inverter consists of two parts of the voltage switches namely DC voltage ladder switches and polarity switches as shown in Figure 2. The DC voltage ladder switches combine the DC voltages through the switches as required for the level in the inverter design.

As shown in Figure 1, the code for the proposed method is developed using the HDL language. The behavioral style of the HDL code is used to generate the switch patterns of the MLI. The synthesis of the developed code is validated using the EDA tools namely Xilinx and cadence. The IC layout is obtained by making use of the genus and innovus tools in the cadence.

Table 1. Voltage level combination for the 35-level LUO progression-based MLI

Positive levels	Voltages	Negative levels	Voltages
0	0	0	0
1	1 V	-1	-1 V
2	2 V	-2	-2 V
3	1 V +2 V	-3	-1 V -2 V
4	7 V -2 V -1 V	-4	-7 V + 2 V + 1 V
5	7 V -2 V	-5	-7 V + 2 V
6	7 V -1 V	-6	-7 V +1 V
7	7 V	-7	-7 V
8	7 V + 1 V	-8	-7 V -1 V
9	7 V + 2 V	-9	-7 V -2 V
10	7 V + 2 V + 1 V	-10	-7 V -2 V -1 V
11	21 V -7 V -2 V -1 V	-11	-21 V + 7 V + 2 V + 1 V
12	21 V -7 V -2 V	-12	-21 V + 7 V + 2 V
13	21 V -7 V -1 V	-13	-21 V + 7 V + 1 V
14	21V -7 V	-14	-21 V + 7 V
15	21 V -7 V + 1 V	-15	-21 V + 7 V -1 V
16	21 V -7 V + 2 V	-16	-21 V + 7 V -2 V
17	21 V -7 V + 2 V + 1 V	-17	-21 V + 7 V -2 V -1 V

3. RESULTS AND DISCUSSION

The proposed method for the development of IC layout for the 35-level LUO progression switched ladder multi-level inverter is validated using MATLAB and EDA cadence tool. The MATLAB tool is utilized to verify the functionality of the algorithm to correctly generate the switch patterns of the MLI circuit. The Switch patterns in digital form are developed using the HDL code and translated into Xilinx Simulink Block to be cross-compiled as given in Figure 3. This cross-compiling option provides an opportunity to interlink the developed non-carrier-based switch patterns in HDL with the analog topology of the switched ladder inverter. The execution of the cross-compiled setup produces the AC output for the 35-level LUO progression-based SLI as depicted in Figure 4. The parametric evaluation for the proposed method is carried out for the THD% and is shown in Figure 5. The THD% value for the 35-level LUO progression SLI is 2.59% which is relatively low compared to the [25] that used 8 bits of resolution for the HDL in the switching of H-bridge CMLI topology. Table 2 proves the merit of the THD% for the proposed method is low in comparison with the HCMLI circuit. Also, the number of switches utilized is only 6 for the LPSLI whereas the HCMLI uses 12 switches. The objective of this paper is attained lower THD% for the given 35-level LUO based SLMLI by making use of the improved HHM-SAM. Table 3 validates the enhancement of the proposed method with the value of 2.59% in THD compared to the 2.64% in THD for the conventional SAM algorithm. The other object of developing the SOC is depicted in Figure 6. The IC layout plan for the 35-level LPSLI switching algorithms is developed by making use of cadence EDA tools. Overall, three tools are used for the IC chip layout design namely incisive, genus, and innovus for simulation, synthesis, and IC layout respectively.

Table 2. Comparison of the proposed 35-level LPSLI circuit with the H-bridge CHMLI

Methods	Level	No of switches	Resolution	THD%
[25]	35	12	2^8 & 2^{12} bits	3.28%
Proposed method	35	6	2^8 bits	2.59%

Table 3. Comparison of the proposed improved HHM-SAM with the conventional HHM-SAM

Methods	Level	V_{RMS}	V_{PEAK}	THD%
Existing HHM	35	12.05	17.04	2.64%
Improved HHM	35	12.03	17.01	2.59%

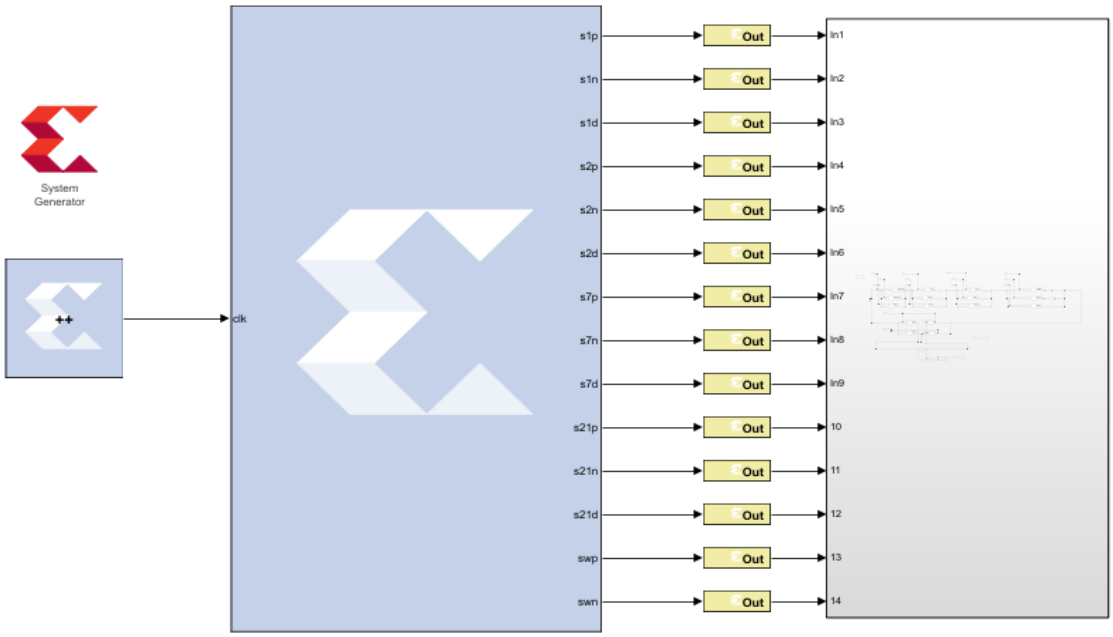

Figure 3. Simulink model for the proposed 35-level LUO progression-based Xilinx block

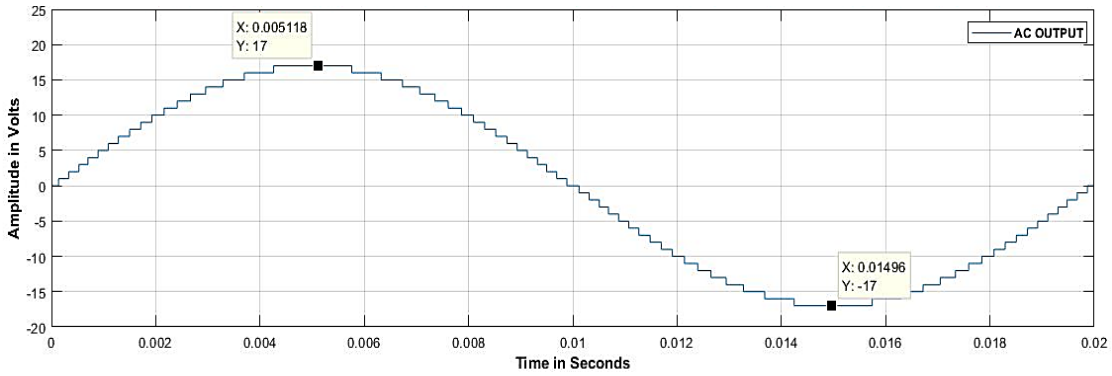

Figure 4. AC output for the 35-level LUO progression-based MLI using the Xilinx Simulink blocks

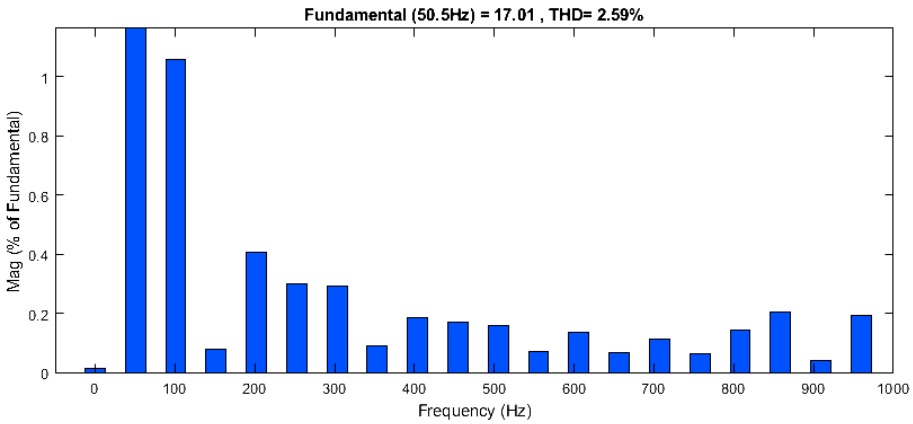

Figure 5. THD% calculation for the 35-level LUO progression-based MLI using the Xilinx Simulink blocks

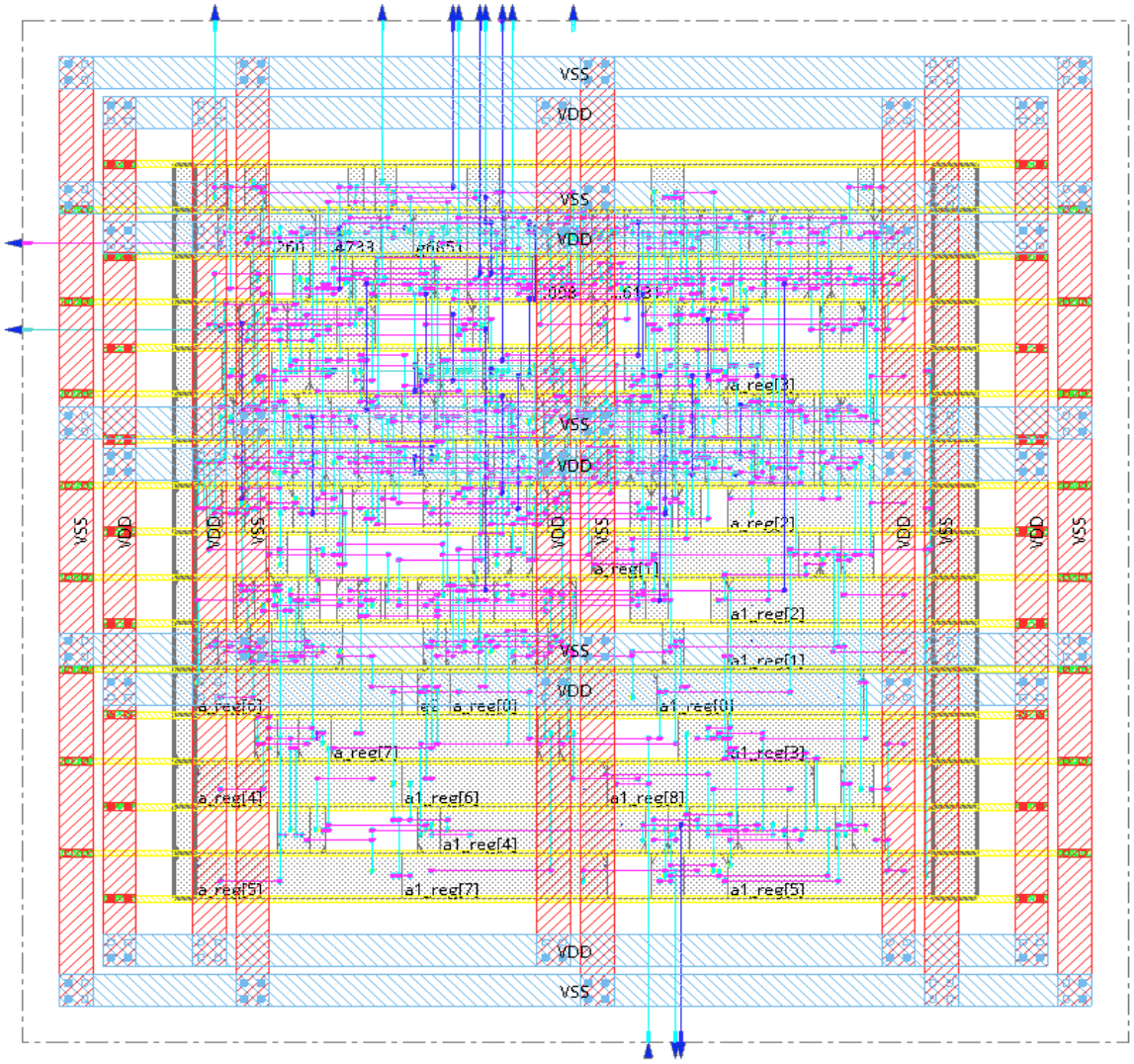

Figure 6. IC chip layout for the 35-level LUO progression-based MLI using cadence tool

4. CONCLUSION

The proposed 35-level LUO based switched ladder multi-level inverter is driven by the improved switching angle method driven switch patterns to exhibit THD% as low as 2.59% compared to the conventional angle formulation method with the THD% of 2.64%. The application-specific SOC is successfully designed for the proposed improved non-carrier switching patterns of the 35-level LUO progression-based switched ladder inverter. Future work could be invested in the fault analysis of these driving switches using a deep learning algorithm.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Joseph Anthony Prathap	✓	✓	✓	✓	✓	✓			✓	✓	✓	✓	✓	
J. Kanti Prasad		✓	✓		✓	✓		✓	✓	✓			✓	
Vivekananda Reddy		✓	✓		✓	✓	✓			✓				
Chinthapalli Suheil		✓	✓		✓	✓			✓					

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author, [JAP], upon reasonable request.

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