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Power factor correction converters overview with PSIM simulation-based systematic control design for the totem-pole topology

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ABSTRACT

The need for power factor correction (PFC) is inevitable due to the distortion of the supply current that results from the widely used switched mode power supplies (SMPSs). This paper first introduces the effects of SMPSs on the grid and the concept of PFC, followed by a review of the different ways to achieve this correction. Due to its numerous benefits, the totem-pole topology is chosen. A complete design of a totem-pole power factor correction (TPPFC) converter for universal use is demonstrated with the aid of the PSIM software and its SmartCtrl tool for a step-by-step design, achieving a simulated power factor (PF) as high as 0.99984 for normal full loading and a sinusoidal input current with a total harmonic distortion (THD) as low as 1.8038%. This work is the first complete, concise, and easy-to-follow PSIM simulation-based design guide for the TPPFC converter.

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1. INTRODUCTION

The demand for DC loads like PCs, laptops, electronic devices, and home appliances is rising. These loads obtain power from AC mains in two stages, as shown in Figure 1(a). First, AC is rectified into DC using a full-wave bridge rectifier and then filtered with a capacitor [1]. The second stage, the DC-DC stage, utilizes switches to adjust the voltage according to the application. These supplies are referred to as switched-mode power supplies (SMPSs) and boast high efficiencies that surpass 90%, leading to the replacement of linearly regulated power supplies.

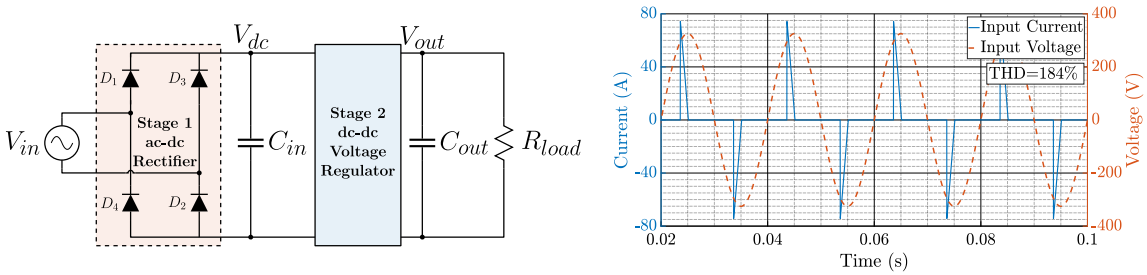
The DC link in SMPS, C_{in}, helps maintain the output DC voltage close to the peak value of the input voltage until the next charging cycle. As a result, the capacitor experiences brief moments of high input voltage for charging. This causes current spikes around the input voltage peaks, as depicted in Figure 1(b). The non-sinusoidal nature of this input current, leads to a poor power factor (PF). The total harmonic distortion of the input current (THDi) in Figure 1(b) is 184%.

The relatively large number of SMPSs used daily reflects poorly on the power quality and stability of the grid. The reduction in PF due to the harmonic content of the distorted current is not desirable as it increases the current withdrawal from the mains for the same amount of real power. Thus, these supplies must comply with international standards, such as the IEC 61000–3–2 and the IEEE-519, before connecting to the grid. The THDi must be less than 5% to comply with the IEEE-519 standard to prevent the continuous reduction in power quality with the increased use of SMPSs and to limit the high harmonic content generated.

Improving the PF by drawing a sinusoidal current in phase with the voltage reduces the harmonic content and enhances the power quality. This can be realized through power factor correction (PFC) techniques, which alleviate the effects of poor PF on the grid. This work will focus on the first stage of these SMPSs, namely, a technique to rectify AC signals into DC quantities in a relatively harmless way to the grid compared to the traditionally used bridge highlighted in Figure 1(a). PFC techniques are classified into passive and active circuits, where passive circuits use energy storage elements (inductors and capacitors). In contrast, active circuits utilize different power electronic topologies and control methods to correct the PF. Active PFC techniques, which will be overviewed in this work, are preferred over passive ones because of the much higher PF achieved and smaller circuitry [1].

Active PFC converters utilize electronic elements with feedback control, regulating output voltage level and correcting the PF to a value very close to unity. They are suitable for high-power applications and can operate across a universal voltage input range. Using high-frequency switching, these converters shape the current to the desired sinusoidal form, significantly reducing their size compared to passive techniques. Many topologies are used to achieve active PFC, with and without the rectification bridge, as in conventional SMPSs; they are classified into bridged and bridgeless topologies [2]-[7]. Figure 2 shows some of the most common topologies to achieve active PFC.

The totem-pole topology is chosen here for the design and simulation due to its numerous advantages over conventional bridged PFC topologies and other bridgeless topologies [8]-[16]. The rest of the paper is arranged as follows: i) Section 2 provides a brief overview of the active PFC topologies, presented in Figure 2, with emphasis on the recently re-emerging totem-pole topology enabled by advancements in state-of-the-art gallium nitride (GaN) transistors; ii) Section 3 offers a simple yet thorough step-by-step design guide for a TPPFC converter that is easy to follow and implement using the PSIM software and the SmartCtrl tool; iii) In section 4, the performance of the designed TPPFC converter is validated through simulation and tested under different input voltage levels and loading conditions. A momentary short circuit is also introduced to verify that the output voltage is maintained above a predetermined level; and v) Lastly, the results are discussed, and conclusions are drawn.



(a) (b)

Figure 1. Typical SMPS: (a) general power supply circuit diagram and (b) input current spikes vs input voltage at V_{in} = 230 V, 50 Hz

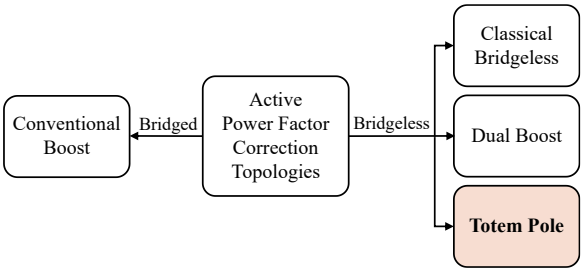


Figure 2. Active PFC topologies classification

2. POWER FACTOR CORRECTION TOPOLOGIES OVERVIEW

The efficiency, power density, and ease of control of AC-DC power supplies are continuously being challenged. Therefore, in this section, the different PFC topologies mentioned in Figure 2 are briefly reviewed along with a discussion of their pros and cons. The circuit of each topology is shown in Figure 3. The first topology to be reviewed is the traditional bridged PFC topology.

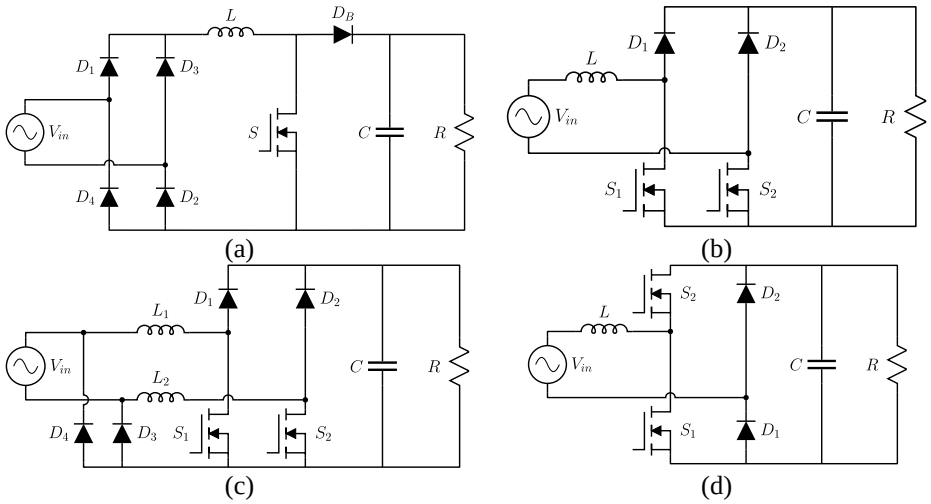


Figure 3. Different PFC topologies: (a) bridged conventional boost, (b) classical bridgeless boost, (c) dual boost, and (d) totem-pole

2.1. Bridged PFC

The most common active PFC circuit is the conventional boost PFC shown in Figure 3(a), where a boost DC-DC converter is connected in series with the full bridge diode rectifier. The reason for using a boost converter is the inductor at the input, which filters high-frequency components in the input current. When the switch is closed, the inductor is charged from the AC mains with the input voltage applied across it and a positive left-side polarity. When the switch opens, the inductor opposes the decrease in its current by changing polarity, and together with the rectified AC input, charges up the output capacitor, and the output voltage is boosted [2].

This PFC method is widely used for its simplicity and high PF, reaching up to 0.99. In addition, it has less common-mode (CM) electromagnetic interference (EMI) compared to other bridgeless topologies. However, it has significant drawbacks concerning efficiency, size, and cost. Compared to bridgeless topologies, the full bridge rectifier incurs more conduction losses due to the higher number of diodes in the conduction path and the relatively more components used; hence, it has a higher cost and a lower power density. In addition, the reverse-recovery characteristics of the diodes in this topology result in lower efficiency [3].

2.2. Bridgeless PFC

The poor heat management of the bridged conventional boost PFC makes it harder to attain high power densities. The bridge rectifier in the bridged PFC circuits results in 2-3% losses of the overall output power [4]. Bridgeless PFC circuits became popular because of the absence of the input bridge rectifier, resulting in reduced power losses due to the decrease of the overall conduction losses of the semiconductor devices. The main bridgeless PFC topologies include:

2.2.1. Classical bridgeless PFC

This basic topology shown in Figure 3(b) can be derived from the bridge rectifier by replacing the bottom two diodes with MOSFET switches, taking advantage of their intrinsic body diode, and placing the boost inductor, L, at the input side. In the positive half cycle, D_1 and S_1 work together as a boost converter to charge and discharge the inductor, with the body diode of S_2 providing the return path of the current. Similarly, in the negative half cycle, D_2 and S_2 do the boosting action while the body diode of S_1 provides the return current path.

The conduction path in the bridgeless topology has two semiconductor devices compared to three semiconductors in the conventional boost PFC. This results in a lower voltage drop in the line current path, increased efficiency and reduced the number of components. On the other hand, this topology suffers from increased CM noise compared to the conventional boost PFC [5], [6].

2.2.2. Dual boost PFC

To reduce the CM noise, the classical bridgeless-boost PFC's topology is modified by adding two slow recovery diodes, D_3 and D_4, and another inductor, L_2, as in Figure 3(c). This arrangement replaces the

high-frequency pulsating voltage source with a low-frequency path between the ac input and output terminals, reducing the CM noise to a level similar to the conventional boost PFC, but this comes at the additional cost and size of the extra inductor and two diodes, reducing the power density of the converter [7].

2.2.3. Totem-pole PFC

The totem-pole PFC (TPPFC) topology has a simple design, as shown in Figure 3(d). This topology is similar to the classical bridgeless-boost PFC but with the bottom switch and opposite diode swapped. The name comes from the fact that the two switches are stacked on top of each other, looking similar to a "totem-pole" [4]. The TPPFC topology has the leg with the diodes operating at line frequency and the switches operating at high frequency. During the positive half cycle of the input voltage, switch S_1 is turned on and off, and the diode D_1 always conducts the input current. The input inductor L, the switches S_1 and S_2, along with the diode D_1, form a typical boost converter; S_1 acts as the active switch, and the body diode of S_2 as the diode of the boost converter. This remains true in the negative cycle, with S_1 and S_2 reversing functionality [8], [9]. Figures 4(a) and 4(b) illustrate the current paths during the positive half-cycle of the input voltage, while Figures 4(c) and 4(d) depict the current paths during the negative half-cycle, respectively.

The TPPFC has several advantages over other PFC topologies [10]-[13], these mainly being the following: i) achieves relatively the lowest conduction losses, ii) better CM EMI performance, iii) easier input-voltage measurement; and iv) simple circuitry at high device utilization, resulting in higher power densities.

Although its conduction losses are among the minimum of all PFC topologies, the main issue is that this topology can only be operated in discontinuous-conduction mode (DCM) or critical-conduction mode (CrM). If operated in continuous-conduction mode (CCM) without more complex control, the reverse recovery of the body diodes of the silicon MOSFETs can cause very high losses. This is due to the much longer recovery time of the MOSFET's body diode than that of a standard fast-recovery diode, resulting in excessive reverse recovery losses and significantly reducing the efficiency.

However, with the development of wide-bandgap semiconductor devices, especially gallium nitride (GaN) transistors, the TPPFC topology is attracting much more attention and becoming the most promising topology. The absence of an intrinsic body diode, and effectively any PN junction in the GaN device, leads to no minority carrier injection and, as a result, no stored charge. This translates to zero recovery charge ($Q_{rr} \approx 0$) in GaN transistors and no reverse recovery operation when used as a rectifier [14]. Furthermore, the lateral structure of GaN switches, together with the reduction in the chip size and the reduced R_{on}, results in the reduction of the junction capacitance and the total capacitance of the device.

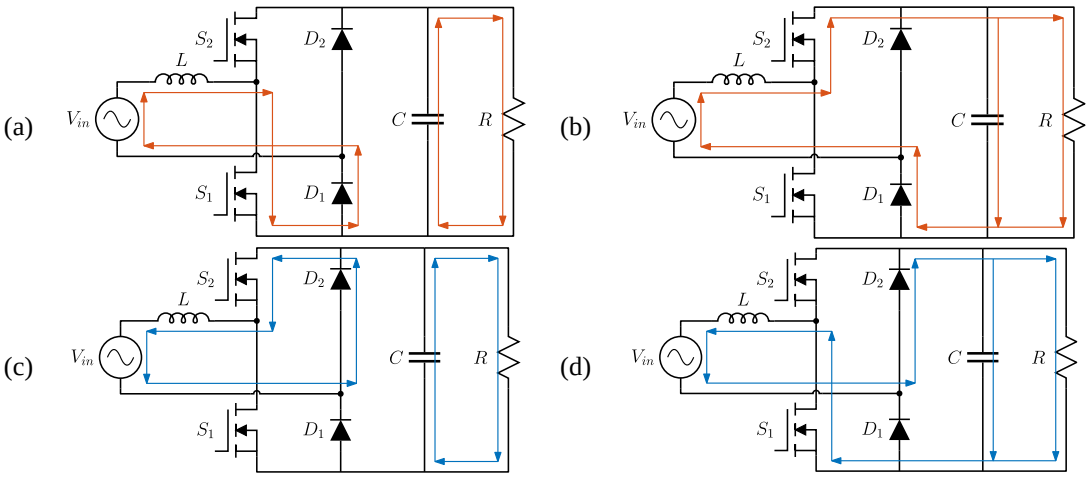


Figure 4. Current path during the positive line cycle when S1 is (a) on, (b) off, during the negative line cycle when S2 is (c) on, and (d) off

This makes the GaN high-electron mobility transistor (HEMT) operate more like an ideal high-frequency switch by decreasing the gate charge, which allows for faster switching and lower drive losses [14]-[16]. The driving scheme of GaN HEMTs must be properly addressed, as several challenges, like signal oscillations and potential malfunctions, could arise due to parasitic capacitance [17]. The advantages mentioned above of GaN switches enable the utilization of the TPPFC topology in the CCM. Therefore, a great

deal of attention is being directed onto this topology; hence, it is important to lay out a well-structured and quick design guide for the converter to shift the focus into enhancing the topology and solving other anticipated hardware-related difficulties. The design process discussed in the following section aids in achieving a solid yet quick design of the TPPFC converter.

3. TPPFC CONVERTER COMPLETE DESIGN GUIDE

This section covers important design considerations for the TPPFC. First, the plant components of the low-frequency leg and the available closed-loop control methods are discussed. Then, a detailed design procedure for the TPPFC converter is presented.

3.1. Design considerations

3.1.1. Low-frequency leg components

Referring back to Figure 3(d) and as mentioned earlier, the TPPFC has two legs; the one on the left, comprised of switches S_1 and S_2, operates at the high switching frequency, while the other leg on the right, made up of diodes D_1 and D_2, operates at the low line frequency. It is common practice in this topology to replace the diodes of the low-frequency leg with silicon MOSFETs to take advantage of their lower conduction losses, compared with slow recovery diodes, thereby improving efficiency. However, this adds more control requirements to turn these switches on and off and increases the cost. Another problem with using transistors instead of diodes is their output capacitance, C_{oss}. This output capacitance is one of the main reasons behind the inductor current spikes at the zero crossing [18], [19].

Referring to Figure 4(d), during the negative half cycle of the line voltage and when S_2 is off, it is evident that D_1 is subject to the full output voltage in reverse bias mode. If there were a switch instead, its output parasitic capacitance C_{oss} would thus be charged to the full output voltage. When the input voltage changes polarity after the zero crossing and S_1 turns on, as in Figure 4(a), the charged C_{oss} is now allowed to discharge through the inductor, creating a positive current spike at the zero-crossing moment. The same logic applies to the switching between the negative and positive cycles of the input voltage. Spikes of this kind are hugely alleviated if diodes are used because their junction capacitance values are magnitudes of order less than in MOSFETs. Overall, diodes offer fewer control requirements, more mitigation of zero-crossing current spikes, and are cheaper, while MOSFETs provide higher efficiency. For the advantages above, and since the increase in efficiency is not considerable, diodes were chosen for this design.

3.1.2. Control method

It is impossible to achieve a near-unity PF using an active PFC converter without an adequate control method. This is achieved by having two control loops: an inner current loop that shapes the inductor current into the desired sinusoidal waveform while keeping it in phase with the input voltage and an outer voltage loop to keep the output voltage at a constant level. The inner loop achieves the desired sinusoidal shape by producing the pulse width modulation (PWM) switching signals that control the two high-frequency switches of the TPPFC circuit [20].

The current controller (inner control loop) can result in any of the three conduction modes depending on the design parameters. DCM and CrM both require a bigger input filter, which results in a higher input RMS current than the CCM operation due to the larger ripple in the current, making CCM a more desirable mode of operation for higher power levels. CCM can be realized through different control methods, such as peak current control, hysteresis current control, and average current control [20]-[22]. Other methods, such as sliding mode control (SMC) and predictive current control (PCC), are also used [23]-[25]. The average current control method provides a constant switching frequency, does not need a ramp compensator, and results in a better input current waveform than other control methods; thus, it is the most commonly used control method for PFC converters [25]. Figure 5 depicts this method's resulting inductor current and the current reference. For these reasons, operation in the CCM using the average current control method is chosen for this design.

3.2. Detailed design procedure

The PFC converter's design is typically divided into two steps, guided by the design specifications. First is the sizing of the plant components, where the inductance, capacitance, and resistive load values are calculated, and second is designing the feedback control loops. Each of these steps is carried out in a dedicated sub-section. The flow chart shown in Figure 6 illustrates the overall design process followed in this section. This work includes all the design steps shown in the figure using bold border lines. However, the final step of physical implementation, shown in a dashed border line, is not included due to limited access to resources.

Starting with the specifications and design requirements, Table 1 summarizes the converter's design specifications to be achieved based on values typically used in different industrial application notes similar to [26]-[28], according to which the first step of sizing the components is carried out. For the controller to follow

the reference current as closely as possible, the inner loop must have the highest crossover frequency possible, given that it is less than half of the switching frequency (Nyquist rate limit). As for the outer loop's crossover frequency, it is limited to only a few hertz because the output voltage has a ripple that is at twice the line frequency (100-120 Hz), which, if corrected in the voltage loop, will result in a third harmonic component in the input current [20]. To avoid this, the crossover frequency should be at least ten magnitudes less than the 100 Hz ripple.

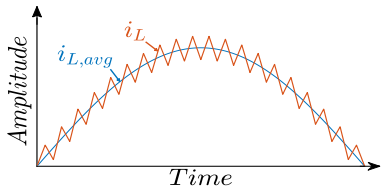


Figure 5. Average current control method waveforms

Table 1. Design specifications

System	System characteristic parameters	Parameter values
Plant	Input voltage (AC in RMS)	85-265 V, 50-60 Hz
	Output voltage (DC)	400 V
	Output voltage ripple	5% of DC voltage = 20 V_{pp}
	Rated output power	3000 W
	Inductor current ripple	10% at low-line voltage/full load
	Switching frequency	500 kHz
Control loops	Hold-up time and minimum voltage	0.5 cycle @ 50 Hz = 10 ms, $V_{o,min}$ = 350 V
	Input power factor	> 0.95
	Inner loop crossover frequency	< 250 kHz
	Outer loop crossover frequency	< 10 Hz

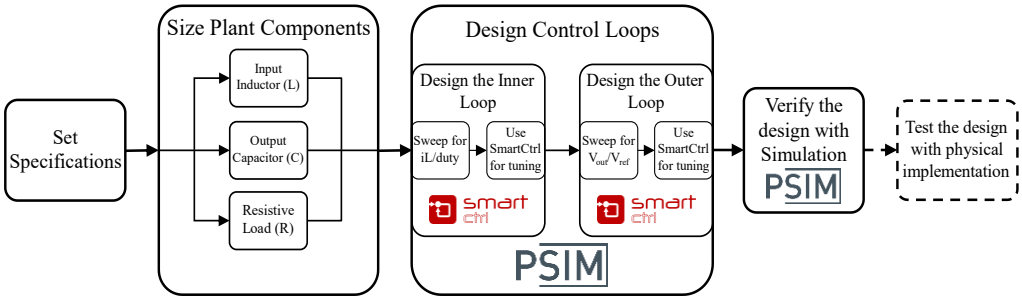


Figure 6. Design process flow

3.2.1. Components sizing

The three main passive components of the TPPFC are shown in Figure 3(d) the input inductor, the output capacitor, and the resistive load. Each of these components has a detailed design illustrated in its respective section below. Important considerations are given for the inductor and capacitor sizing.

a) Input inductor

The minimum inductance needed for CCM operation depends on the desired input current ripple, the high-line voltage, the output power, the output voltage, and the switching frequency. This is shown in (1) [26].

$$L_{min} = \frac{1}{\%\Delta I_L} \cdot \frac{{V_{ac,HL}}^2}{P_o} \cdot \left(1 - \frac{\sqrt{2} \cdot V_{ac,HL}}{V_o}\right) \cdot \frac{1}{f_{sw}} \quad (1)$$

Where, $\%\Delta I_L$ is the percentage input current ripple, $V_{ac,HL}$ is the high-line input voltage, P_o is the output power, V_o is the output voltage, and f_{sw} is the switching frequency. Plugging the desired values for each quantity yields a minimum inductance of 66 µH.

To ensure operation in CCM all the time and decrease the time spent in DCM around the zero-crossing, this minimum value is multiplied by a factor of 1.5, resulting in the final value of about 100 µH. This is a valid increment as the inductance value is in the low ranges of microhenries, making it practical even if implemented in real life. As a result, the current ripple is expected to be less than the intended 10% at low-line voltage, the THD should be improved, and the PF should be closer to unity.

b) Output capacitor

The output capacitance value is restricted by two main constraints: the desired output voltage ripple and the required hold-up time. The (2) and (3) by [26] hereby are the two equations that quantify these constraints.

$$C_o \geq \frac{2 \cdot P_o \cdot t_{\text{hold}}}{{V_o}^2 - {V_{o,min}}^2} \quad (2)$$

$$C_o \geq \frac{P_o}{2\pi f_{line} \cdot \Delta V_o \cdot V_o} \quad (3)$$

Where, P_o is the output power, t_{hold} is the hold-up time, V_o is the output voltage, $V_{o,min}$ is the minimum allowed output voltage during a fault at the input, f_{line} is the input line frequency, and ΔV_o is the output voltage ripple. Using (2) and (3) with the values previously listed in Table 1, and considering that the minimum line frequency results in the maximum capacitance value, yields a result of 1600 µF and 1194 µF for the output capacitance, respectively. Taking the larger value among these two, a capacitor with a magnitude of 1600 µF shall be used. Since this value resulted from the hold-up time constraint and is larger by almost 400 µF from that resulting from the voltage ripple constraint, there is no need to multiply it by a factor to ensure the voltage ripple remains within 20 V as it is already 33% larger.

c) Resistive load

The output resistive load could be easily calculated using the relationship between the voltage across the resistance and the power it consumes. When delivering the full output power of 3 kW at 400 $V_{dc,}$ the equivalent resistive load value comes to 53.33 Ω.

3.2.2. Control design

The TPPFC is designed to function similarly to a boost converter operating in CCM during each half-line cycle. As mentioned before, the CCM operation is preferable for higher power operations. The average current control method is the most widely adopted for CCM PFC converters to attain a near-unity PF.

A double negative feedback loop is required to achieve this and ensure a stable system for the given design specifications. An inner current control loop produces a control voltage signal that is then used to generate the switching signal for the switches. This inner current loop ensures that the measured inductor current follows a generated current reference, shaping the input current waveform into a sinusoidal waveform to achieve a PF that is very close to unity.

In addition, an outer voltage loop is needed to keep the output DC voltage of the PFC regulated to the pre-determined reference voltage. The outer voltage control loop is also responsible for determining the amplitude of the generated current reference, which is then used in the inner current loop [20]. The TPPFC converter control block diagram is shown in Figure 7. In this control scheme, it should be noted that the sensed output voltage, input voltage, and current are normalized by their respective RMS values. The voltage controller provides the current reference magnitude multiplied by the rectified, normalized input voltage to produce the current reference signal. This feedforward of the input voltage guides the input current to track it and avoids propagating the input voltage disturbance through the PFC feedback loops [20]. The output of the current controller is the duty ratio (D), which is used to generate the switching signals for the converter. To avoid extreme values for D (near 100%), which occur at the zero crossings, a limiter is used with a margin of 2%, i.e., 0.02 – 0.98.

a) Inner loop design

The inner loop controller needs to be fast enough to make the input current track the input voltage and as a result, the inner current control loop is required to have a very large bandwidth relative to the outer voltage control loop. Thus, each loop shall be designed separately [29]. The design of the inner current loop and the tuning of the proportional-integral (PI) compensator in the control loop will be illustrated in the steps to follow hereafter.

- Inner loop-Step 1: Since the PFC operates as a boost converter during each half-line cycle, the first step is to determine the duty ratio (D) of the boost converter that results in an output voltage of 400 V as per the design specifications. The boost converter is designed to provide an output of 400 V from a 230 V DC input. The duty ratio is found using (4), which gives a result of 0.425.

$$V_o = \frac{V_{in}}{1-D} \quad (4)$$

As in the boost converter, the PWM signal is generated by comparing a triangular wave with a constant DC reference through a comparator, where the triangular wave varies between 0 V and 1 V at f_{sw}. The reference of the PWM modulator should be set at 0.425 and a small signal perturbation is introduced to this reference as an AC sinusoidal source. An AC sweep is performed on the added perturbation source, and the input

current is measured to obtain the open-loop bode plot. The circuit used to obtain the bode plot in PSIM is shown in Figure 8(a), and the resulting bode plot is displayed in Figure 8(b).

- Inner loop-Step 2: The bode plot in Figure 8(b) is then imported into the SmartCtrl software used in this work, which will help tune the compensator. After importing it, the current-controlled mode single loop with a current sensor and a PI regulator is chosen.

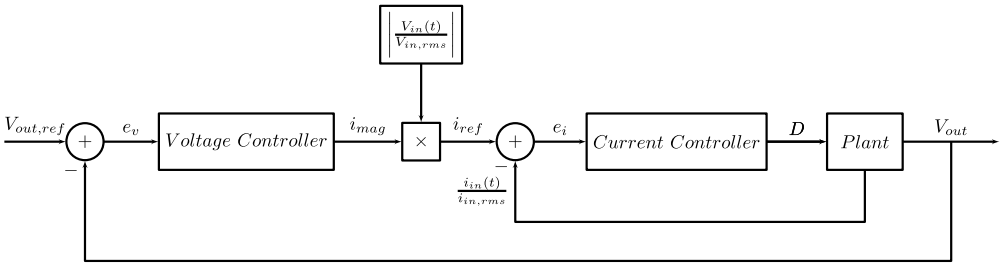
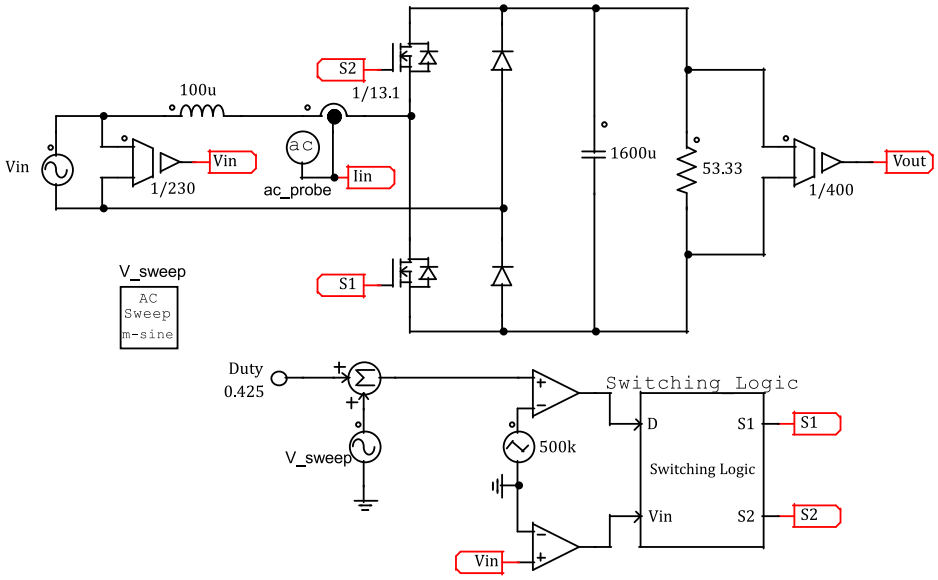


Figure 7. TPPFC converter control block diagram

(a)



(b)

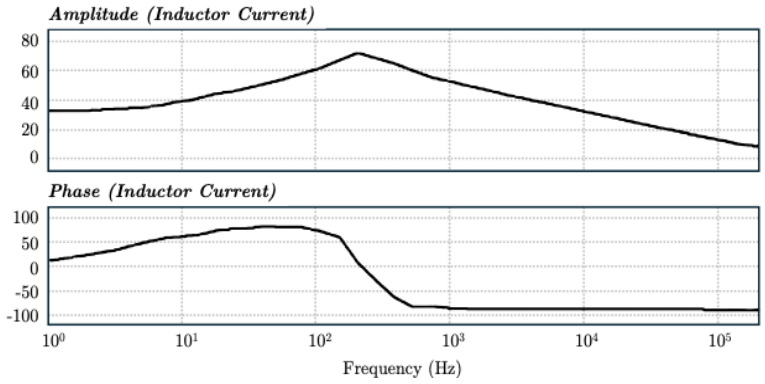


Figure 8. Inner loop-Step 1: (a) inner current loop sweep circuit and (b) current control open-loop bode plot

SmartCtrl provides a solution map with pairs of crossover frequencies (f_{cv}) and phase margins (Φ_m). It identifies stable controller combinations and potential instabilities. A crucial factor in selecting a stable solution is ensuring that the closed-loop phase response is nearly zero between 100 and 120 Hz to achieve a good power factor. This allows the inner loop to track the input voltage, a rectified sinusoid at either 100 or

120 Hz in a universal input 50-60 Hz PFC design. Figure 9 depicts the inner closed-loop phase response [20]. SmartCtrl calculates the PI compensator constants (k_p and k_i) based on the chosen crossover frequency (f_{cv}) and phase margin (Φ_m). With an inner loop crossover frequency of 200 kHz and a phase margin of 40°, the controller values are determined as k_p = 2.99929 and k_i = 651.235 n.

b) Outer loop design

The outer voltage control loop has two objectives: determining the peak inductor current reference and stabilizing the output voltage. The output voltage contains a second harmonic component, causing pulsation at twice the main frequency (50 Hz or 60 Hz). To regulate the average output voltage at 400 V, the voltage control loop must suppress the second harmonic ripple from the feedback path [30]-[31]. This results in a lower bandwidth than the inner loop, with a crossover frequency below 100 Hz. The voltage loop control is designed in two main steps, as outlined below:

- Outer loop-Step 1: The circuit in Figure 10(a) (see Appendix) generates the output voltage's bode plot with a 1 V reference and a small signal perturbation, similar to the current loop. The resulting bode plot is shown in Figure 10(b) (see Appendix).
- Outer loop-Step 2: The bode plot is imported into SmartCtrl to tune the voltage controller compensator. The PI is adjusted to regulate the output voltage at 400 V while attenuating 100-120 Hz open-loop frequencies and avoiding third harmonic distortion in the input current [20]. Figure 11 shows the open-loop response of the output voltage with a crossover frequency of 5.7 Hz and a phase margin of 42.5°, resulting in $k_{p,V}$ = 0.0685427 and $k_{i,V}$ = 626.568 µ. Figure 12 shows the control stage design in PSIM, while Table 2 summarizes the component and control parameter design results used for the subsequent simulation presented in the next section.

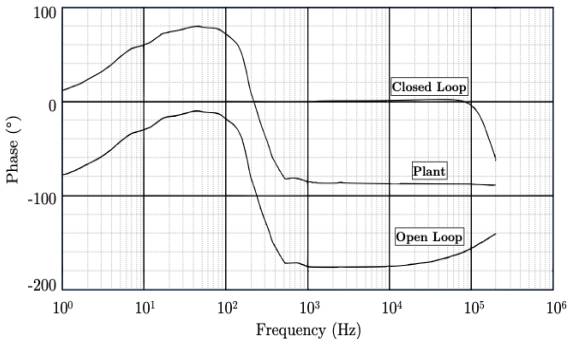


Figure 9. Input current closed-loop phase response (brown line)

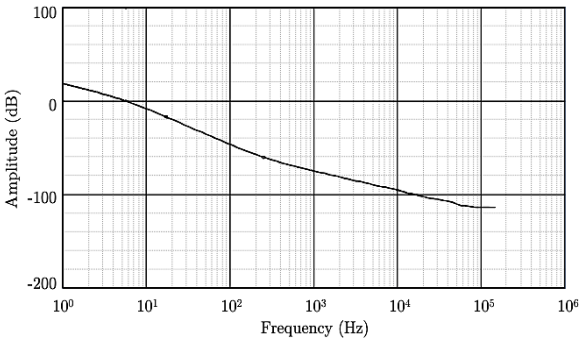


Figure 11. Output voltage open-loop magnitude plot after tuning

Table 2. Design results summary

Components sizing	Input inductor (µH)	Output capacitor (µF)		Resistive load (Ω)
	100	1600		53.33
Inner loop design	$f_{cv,I}$ (kHz)	$\Phi_{m,I}$ (°)	$k_{p,I}$	$k_{i,I}$
	200	40	2.99929	651.235 n
Outer loop design	$f_{cv,V}$ (Hz)	$\Phi_{m,V}$ (°)	$k_{p,V}$	$k_{i,V}$
	5.7	42.5	0.0685427	626.568µ

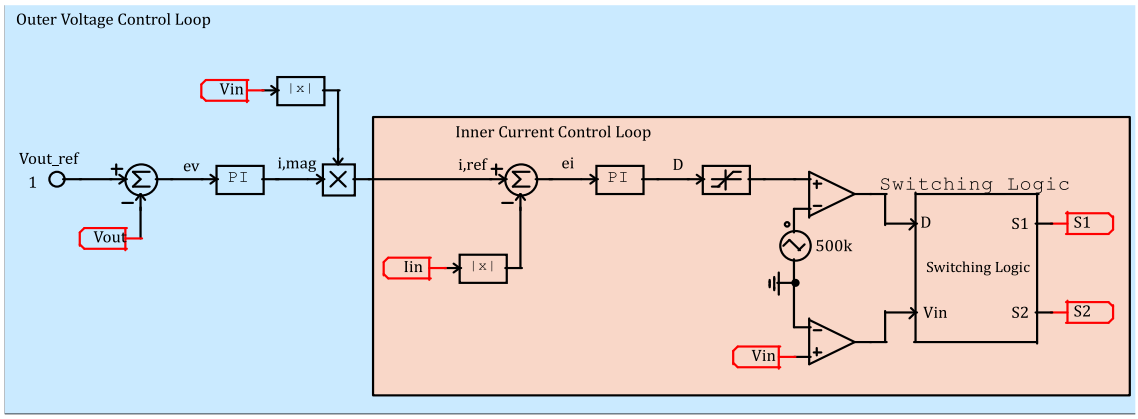


Figure 12. Complete control design

4. SIMULATION RESULTS AND DISCUSSION

After determining component sizes and designing the two control loops, the PFC converter design was simulated using PSIM. Ideal MOSFETs represented the GaN switches, and all other components were considered ideal for the results in this section. The converter underwent tests for full loading at rated input requirements and various scenarios to validate the system specifications. All data was obtained from PSIM and graphed in MATLAB.

4.1. Full load tests at various input voltage levels and frequencies

In the first simulation, the performance of the TPPFC converter was assessed under various input voltages, representing the universal and common ranges worldwide. The converter was tested with four input voltages: 85 V and 120 V at 60 Hz and 230 V and 265 V at 50 Hz. At each level, graphs were obtained for the input current and output voltage. Fast Fourier transform (FFT) was used to calculate the percentage of total harmonic distortion (THD) of the input current. The power factor (PF) was found to be equal to the distortion factor (DF) since there was no phase difference between the input current and voltage. Input current and output voltage ripples were also measured. Figure 13 displays these graphs for the 230 V at 50 Hz input voltage. Table 3 summarizes the results for the four levels previously mentioned to help interpret the outcomes of this test.

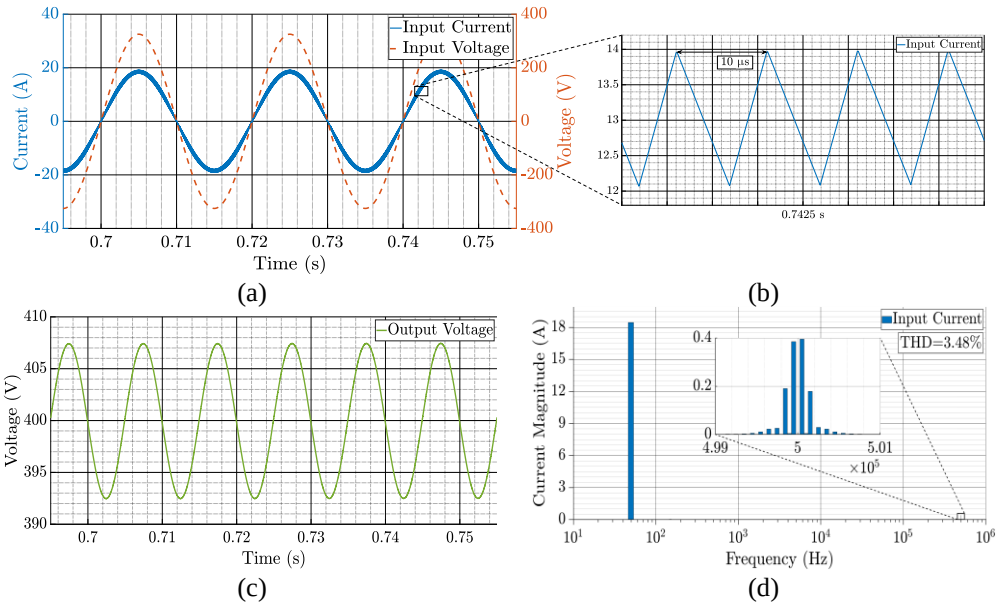
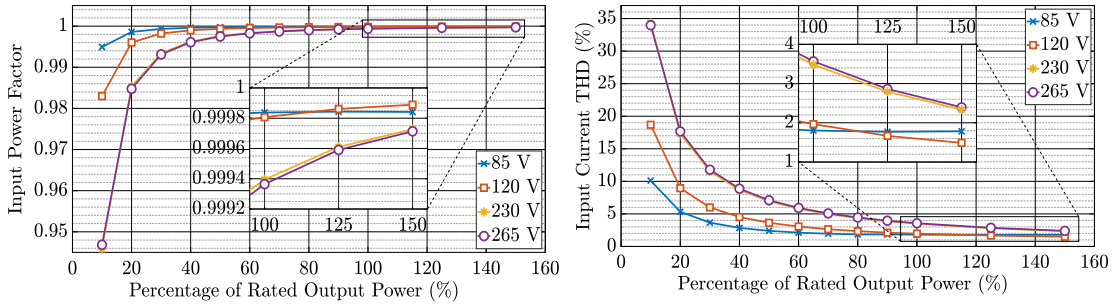


Figure 13. Steady-state operation results at V_{in} = 230 V, 50 Hz: (a) input voltage and current, (b) input current ripple, (c) output voltage, and (d) input current harmonics

In this test, the output load resistance was varied to simulate different loading levels: 10% to 100% in 10% increments and overloading levels of 125% and 150%. For each level, the input current's THD and PF were calculated and plotted against the load level, resulting in Figures 14(a) and 14(b). Looking at the PF variation, it is obvious that as the power loading increases, the PF increases. It could also be seen that it remains above 0.95 for all loading percentages at all input voltage levels except for 230 V and 265 V, where it is slightly under at 0.946 and 0.947, respectively, for 10% loading. As for the overloading conditions, the PF improves, going from 100% to 125% and 150% loading for all levels, except for the 85 V, where it remained constant. The maximum PF with a value of 0.99989 is achieved for 150% loading at 120 V input voltage.

Table 3. Summary of simulation results for the TPPFC converter main operation

Voltage level and frequency	85 V, 60 Hz	120 V, 60 Hz	230 V, 50 Hz	265 V, 50 Hz
Input current ripple (A)	1.675	1.95	1.9	1.725
Percentage input current ripple (%)	3.356	5.515	10.300	10.775
Output voltage ripple (V)	12.25	12.5	15	15
Input current THD (%)	1.8038	1.9656	3.4807	3.5674
Input PF	0.99984	0.99981	0.99939	0.99936



(a) (b)

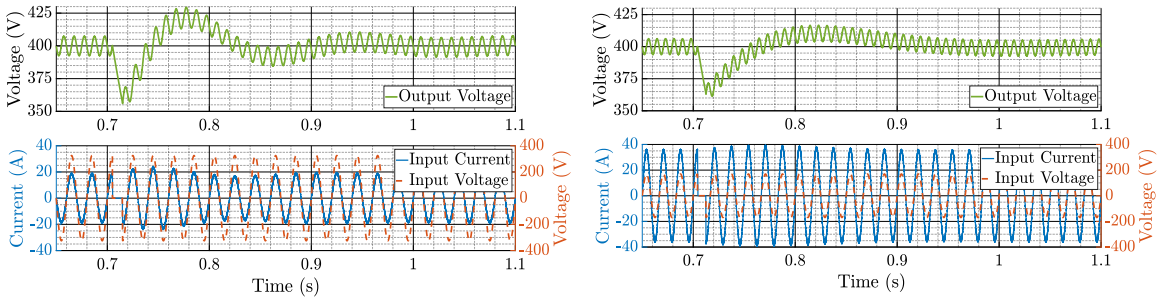
Figure 14. Input (a) PF and (b) current THD against loading percentage

The change in the current THD is inversely related to the PF, causing the THD to decrease as the loading level increases. For the 85 V and 120 V levels, it drops below 5% at around 22% and 36% loading, respectively. As for the 230 V and 265 V levels, the THD reaches the 5% mark at around 70% of the load. Again, the converter shows very good performance even as the load goes beyond 100%, where the THD decreases for 25% and 50% above the full load, achieving a minimum value of 1.5%.

4.2. Momentary short circuit

A half-cycle short circuit at the input voltage was introduced to test whether the capacitor maintains the output voltage above 350 V for that period. This test was done on the two standard voltage levels: 120 V and 230 V. The short circuit duration was 0.01 s for the 230 V, 50 Hz input voltage and 0.00833 s for the 120 V, 60 Hz input voltage. The graphs in Figure 15 show how the input current and output voltage react to a brief short circuit in the input voltage.

The primary motivation behind this test is to observe whether the capacitor holds the output voltage above 350 V for half a cycle in case a short circuit occurs at the mains, resulting in a 0 V input voltage. As Figure 15(a) shows, when the input voltage changes drastically from a peak voltage of 325 V to 0 V, the output voltage is maintained above 355 V for the complete half-cycle duration of the short circuit. As for the other case, when the input voltage was 120 V, as shown in Figure 15(b), the output voltage is maintained at an even higher voltage than in the first case. Here, the output voltage does not drop below 360 V. This test verifies the capacitor's design as it is required to hold a voltage of at least 350 V when a short circuit occurs for a duration equivalent to half a cycle.



(a) (b)

Figure 15. Effect of a momentary short circuit on the output voltage and input current for (a) Vin = 230 V, 50 Hz and (b) Vin = 120 V, 60 Hz

This section verified that the designed PFC converter meets all the design specifications that were initially set. It can also be seen that the closed-loop performance is stable, fast, and rigid enough to bring the system back to stability when it faces disturbances such as a momentary short circuit. Even though the performance of the PI controller is satisfactory, implementing more complex compensators in the TPPFC converter can also be investigated [32], [33].

In addition to that, it is worth mentioning that several additional tests have been carried out to examine the behavior, robustness, and responsiveness of the controller further to external changes at the load or the mains. The converter was tested at a sudden load change (from full to half load and vice versa) amidst its normal operation at different voltage levels. Another test observed the effect of a highly inductive load on the converter at full

power rating. The final test was to monitor the effect of a voltage dip or swell in the grid on the operation of the PFC converter. The closed-loop system showed rigid robustness and maintained stability to the tested external factors. The results of the tests are available in the [34] repository, along with the simulation files.

5. CONCLUSION

This work briefly reviewed different topologies, technologies, and performance of PFC converters. The utilization of the zero reverse-recovery capability of GaN devices is then achieved through the design and simulation of a totem-pole PFC. The designed PFC converter is suitable for various input voltage levels ranging from 85-265 V. It is also convenient for a wide range of loads reaching an overload of up to 4.5 kW. The designed PFC converter achieves a PF as high as 0.99989 and a THD as low as 1.5%; thus, the PFC converter is appropriate for different types of applications, even beyond the powering of servers and in different parts of the world.

This paper serves as a reference for achieving a quick yet thorough design of a TPPFC converter. This will enable future researchers to focus on advancing the emerging TPPFC topology rather than spending more time on the design process. This work can be further expanded by exploring design improvements that achieve a lower THD across a wider range of loads, a solution for the issue of the high inrush current spikes, and the implementation of the achieved design for physical verification of the results obtained through simulation.

APPENDIX

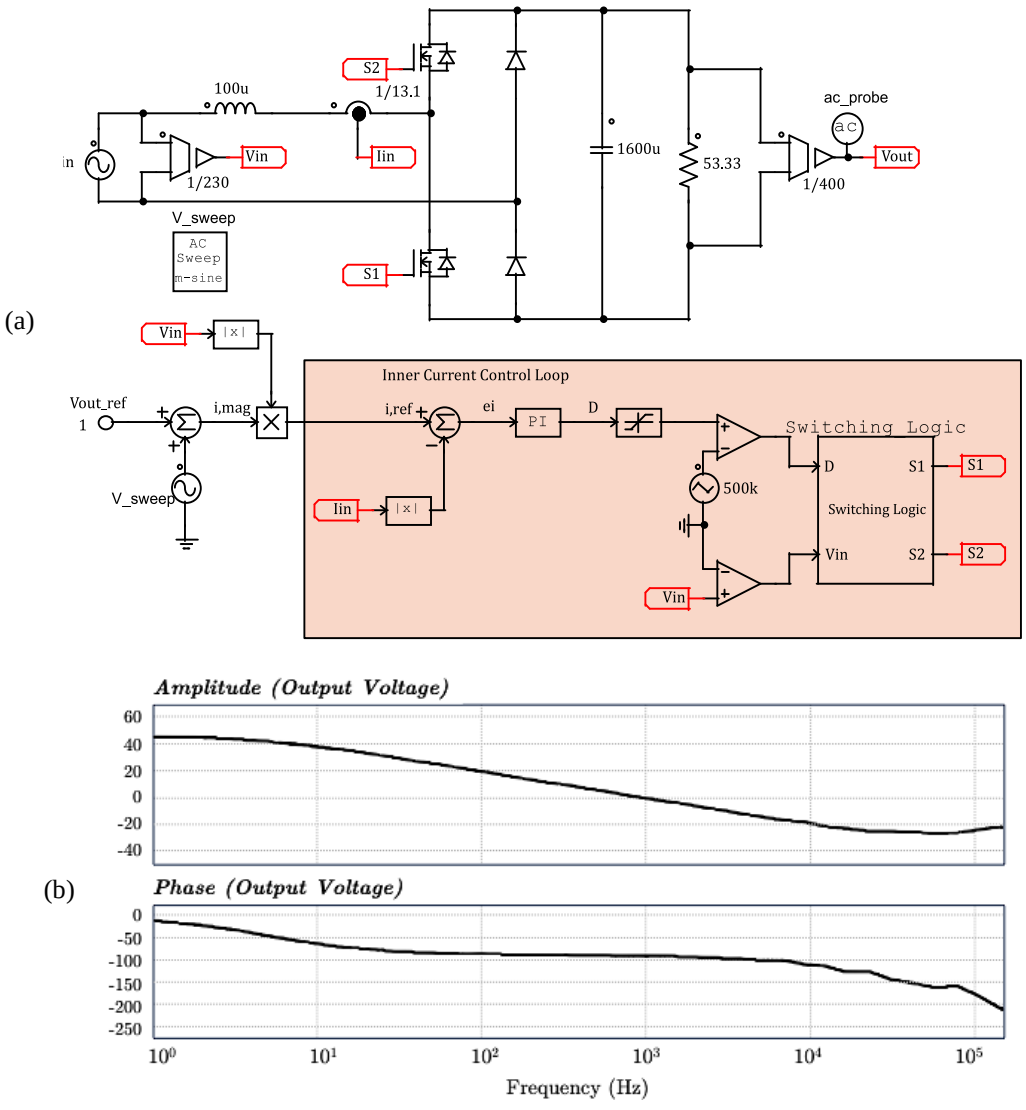


Figure 10. Outer loop-Step 1: (a) outer voltage loop sweep circuit and (b) voltage control open-loop bode plot

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