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Harmonic reduction techniques in renewable energy distribution systems using cascaded multilevel inverters: a comparative analysis

Nayana Gangadhara[1], Savita D. Torvi[2]
[1]Department of Electrical and Electronics Engineering, Sri Siddhartha Institute of Technology, Tumkur, India
[2]Department of Electronics and Telecommunications Engineering, Sri Siddhartha Institute of Technology, Tumkur, India

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ABSTRACT

Penetration of renewable energy in distribution generation increases power quality in the output. The harmonics inherent in the inverters are a major contributor to the power quality issues in the distribution system. Multilevel inverters are used to get rid of the harmonics inherent in the inverter output. Among the multilevel inverter topology cascaded multilevel inverters have taken center stage due to their simple topology and control with lesser components. This paper reviews different multilevel inverter topologies that have led to cascaded multilevel inverter topology and applies pulse width modulation (PWM) techniques to the topology. Phase disposition PWM technique is applied on the cascaded H-bridge multilevel inverter (MLI) topology for 5-level, 7-level, and 9-level inverter topologies. The total harmonic distortion (THD) obtained for these topologies is compared with and without the use of an LC filter in the inverter output. PWM techniques including phase disposition, for five-level, seven-level, and nine-level MLI methods are applied on the cascaded multilevel inverter and results are compared for harmonic reduction in the inverter output.

Corresponding Author:

Nayana Gangadhara
Department of Electrical and Electronics Engineering, Sri Siddhartha Institute of Technology
Tumkur, Karnataka, India
Email: nayanassittumkur@gmail.com

1. INTRODUCTION

Renewable energy source (RES) applications, high voltage DC transmission (HVDC), uninterruptible power supply (UPS), electric vehicles (EV) and microgrid applications with battery storage applications uses inverters as its important power processing unit [1], [2]. Performance of the square wave inverters are improved using advanced topologies and different PWM techniques. Multilevel inverter topologies and sinusoidal two-level pulse width modulation (PWM) techniques are few of them [3], [4]. Higher penetration of RES in the distribution systems have made the higher surge in the use of DC-DC converters, inverters and other related power electronics devices. Since the RES power generation is a costly phenomenon, the converters used in these applications are expected to have excellent performance and dependable [5]. Inverters are expected to generate voltage that can generate near sinusoidal voltage waveform so that it can be connected and synchronized [6] to the distribution system. The basic inverter that generates wave that produces positive half with $V0=+(Vdc/2)$, and the negative half with $V0=-(Vdc/2)$ [7], [8] thus producing the square wave.

Switching losses and total harmonic distortion (THD) are high for these inverters and they are not fit for synchronization without adopting sophisticated PWM techniques [9]. Both stress on the switch and the harmonic distortion is evident in these traditional inverters, and thus it loses it feasibility to connect to the

distribution network [10], [11]. Reduction of harmonic distortion and generating near sinusoidal waveform from the inverters are the challenges that is to be addressed to make the inverters grid ready. various multilevel inverter (MLI) topologies which deliver improved performance are introduced [12]. Reduced harmonics in high switching frequency and low switching losses and near sinusoidal output waveform are the primary characteristics of the MLIs. Higher number of switches included in the MLI topologies increases the system complexity due to addition of driver circuits for each switch. However, each switch has to have its own gate driver for implementing MLI, which adds to the system's complexity. Thus, the reduction of number of switches were attempted by changing the topology of MLI that could work in the same manner but with reduced switches [13], [14].

The topological improvement of the MLIs led to its usage in industrial applications that reckons high power [15], [16]. The transition of the topological variation of the MLIs involves the Diode-clamped topology, flying capacitor (capacitor-clamped), to the cascaded H-bridge multilevel topologies [17]. In the diode clamped MLI topology to obtain n-level output n-1 capacitors, 2(n-1) switches, (n-1) (n-2) clamping diodes are required [18]-[22]. The control of both real and reactive power due to topological advantage, no further use of filters to reduce harmonics, lesser stress on the switches due to split voltage across switches are few of the important advantages of the diode clamped topology [23]-[25]. There is another similar topology as that of the diode clamped MLI called the capacitor clamped topology which uses capacitor to restrict the voltage unlike diode clamped MLI where diode is used for the purpose [26], [27]. Even the voltage levels are one and the same for both these topologies [28], [29].

Capacitor clamped MLIs are popularly known as flying capacitor MLIs. To obtain n-level output in this topology n-1 capacitors, (n-1) (n-2) number of flying capacitors, and total 2(n-1) switches are required [30], [31]. Although the flying capacitor topology gets rid of the clamping diode problems including higher stress on the diodes, reverse recovery of diodes have the disadvantage of higher cost due to usage of more capacitors [32]-[34]. Thus, in order to solve these problems in the flying capacitor topology further improvement in the topology is carried out with the introduction of cascaded H-bridge topology [35]-[37]. By connecting the series of H-bridges the cascaded H-bridge MLIs are articulated for different voltage levels [38]-[40]. Cascaded MLI design does not have the problems encountered in both the diode clamped and the flying capacitor topologies since it does not have the diodes and capacitors for clamping. The number of voltage levels is the sum of all the voltage levels generated by each of the H-bridges [41]. Although this topology has the advantage of implementing soft switching method for reducing the switch stress and all the advantages of the previous topologies, it requires independent dc sources for power conversions in each H-bridge [42]-[44]. Topological variations are coupled with the variations in the PWM techniques to obtain the better harmonic reduction in the MLI topologies. Thus, to facilitate this improvement multi-carrier modulation techniques got introduced. Multi-carrier PWM methods including phase disposition, phase opposition and alternate phase opposition are methods used for the purpose [45].

This paper presents the implementation of the phase disposition method on a cascaded multilevel inverter (MLI) across three different levels of the topology: five-level, seven-level, and nine-level cascaded H-bridge inverters. The objective is to compare the total harmonic distortion (THD) obtained from each inverter level when applying the phase disposition technique. Additionally, a comparative analysis is performed to evaluate the inverter output THD with and without the use of an LC filter for each MLI level. Section 2 provides a detailed discussion of the phase disposition method, elaborating on its operational principles and the role of various filters in improving the MLI output. This section also covers the theoretical background and the implementation specifics of the LC filter in the inverter circuit. Section 3 discusses the results and discussion, offering a thorough quantitative analysis of the THD measured at each level of the cascaded topology. The analysis includes a comparison of THD values with and without the incorporation of the LC filter in the inverter output. The results are systematically tabulated, highlighting the extent of improvement achieved at each MLI level and the additional benefits realized through the use of the LC filter. Finally, the paper concludes with a summary of the findings, emphasizing the effectiveness of the phase disposition method in reducing THD in cascaded MLIs and the significant impact of using LC filters. The conclusion is followed by references to relevant literature and studies that support the research.

2. PROPOSED IMPLEMENTATION

The proposed implementation compares the performance of the phase disposition PWM method on five, seven and nine level inverters. Phase disposition PWM method is a sinusoidal PWM method which uses different levels of triangular carrier waves to generate the pulses for the 3-phase inverter. Phase disposition method is a level-shifting type of PWM technique applied on MLI to reduce the harmonic distortion in the cascaded multilevel inverter (CMLI) topology. Comparison of CMLI with three different levels is analyzed to assess the THD improvement for each level and tabulated in the implementation.

The phase disposition method uses multiple carrier wave to generate PWM for the MLI topology. All the triangular carrier waves are in phase with each other but are vertically displaced to obtain the multilevel PWM output. The reference signal is a modulating signal which is sinusoidal wave with 50Hz frequency. The carrier waves are the group of triangular waves displaced vertically for each level of the MLI output. For a N-level inverter working on the phase disposition method there are N-1 carrier waves with the carrier frequency fc. The vertical displacement of the carrier wave is by a value of Vs/N-1 where Vs is the total output voltage. Considering Vm(t) as the instantaneous modulating wave and Vc,I(t) as the instantaneous carrier wave at time 't' for 'ith' carrier. The output voltage Vout obtained from the multilevel inverter is calculated using the (1).

$$V_{out}(t) = \sum_{i=1}^{N-1} \left[sgn\left(V_m(t) - V_{c,i}(t)\right) + 1 \right] . \frac{V_s}{2(N-1)} \quad (1)$$

Where $sgn(x)$ is the sign function that takes the value of '+1' when x>0 and '-1' when x<0 and '0' if x=0. The PWM generated from the comparison of the modulating signal and the carrier signal is used to trigger the appropriate metal-oxide-semiconductor field-effect transistor (MOSFETS) of the cascaded multilevel inverter. The results obtained by applying the phase disposition, implementation is as given in the following. These methods are applied on 5 level, 7 level and 9 level cascaded multilevel inverter. The THD obtained from these methods and different levels are as given in the following. The MATLAB model is developed for all 5,7 and 9 level inverters. The H-bridge cascaded to form the multilevel inverters. The model of the H-bridge that is cascaded is as given in Figure 1.

The H-bridge given in Figure 1 is cascaded to get the topology that provides the seven-level output from the inverter topology. The specifications of the inverter used are given in Table 1. The cascaded H-bridge inverter used for the quantitative analysis of the MLI with phase disposition method is as given in Figure 2. The phase disposition method uses the sinusoidal wave with phase variation for each phase and triangular wave with higher frequency as the carrier wave with the level shift technique. The triangular waves are generated with different amplitudes to create PWM comparing with the sinusoidal wave at those amplitudes.

Table 1. Specification of 5 level, 7 level, and 9 level inverters

Levels	Parameter	Value
Five level	Number of switches per phase	8
	DC voltage per bridge	100 V
	L, C values	R=100 ohms and L = 314 micro Henry
Seven level	Number of switches per phase	12
	DC voltage per bridge	100 V
	L, C values	R = 100 ohms and L = 314 micro Henry
Nine level	Number of switches per phase	16
	DC voltage per bridge	100 V
	L, C values	R = 100 ohms and L = 314 micro Henry

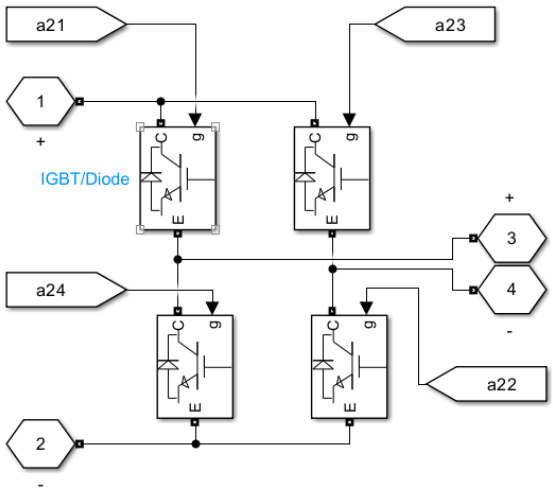

Figure 1. H-bridge of cascaded multilevel inverter

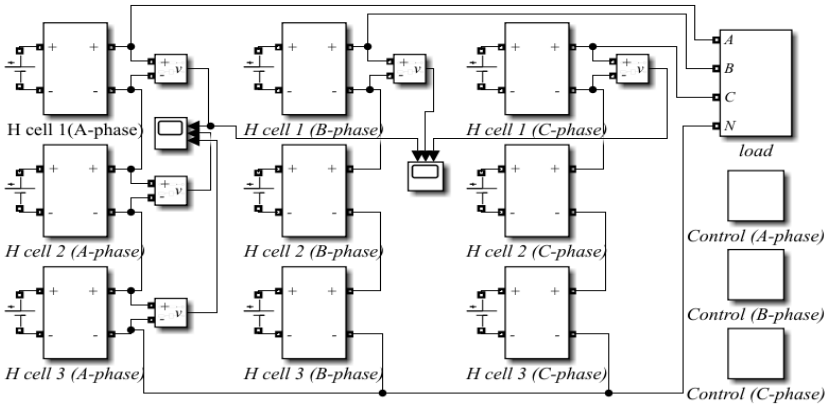

Figure 2. Complete simulation diagram 7-level inverter

3. RESULTS AND DISCUSSION

The multilevel output is obtained by comparing the phase disposed triangular wave with the sinusoidal wave as given in Figure 3. PWM is generated from the comparison of the triangular wave with the sinusoidal wave and the generated PWM is given as the input to the switches of the cascaded multilevel inverter. Although Figure 3 shows the PWM generation for phase A of the cascaded inverter it is extended to all the three phases with the phase angle of the sinusoidal wave changed according to each phase.

The PWM generated from the comparison of the modulating wave and the carrier wave is given to the appropriate switches of each phase and the output obtained from the 3 phase legs of the cascaded MLI is as given in Figure 4. The THD obtained from the 5-level inverter line to line output voltage is as given in Figure 5. It can be observed that the THD is 17% for the 5-level inverter output voltage.

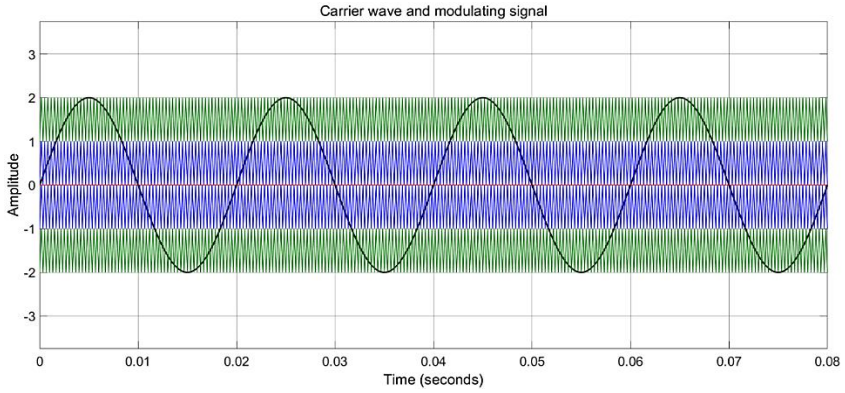

Figure 3. Phase a 5-level inverter-carrier wave and modulating wave

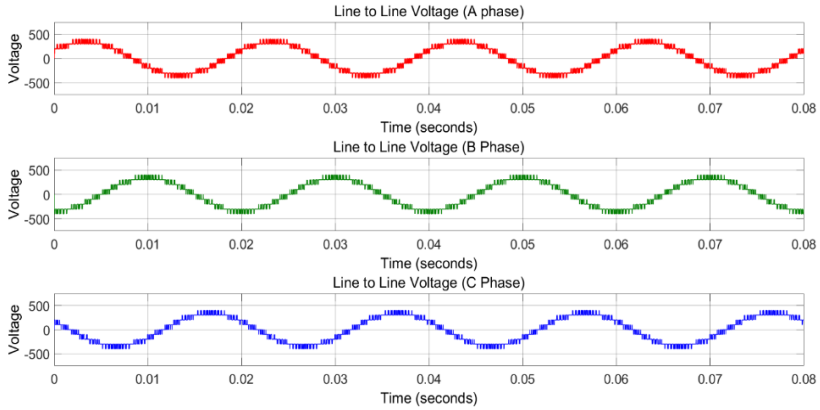

Figure 4. 3 phase wave 5 level inverter

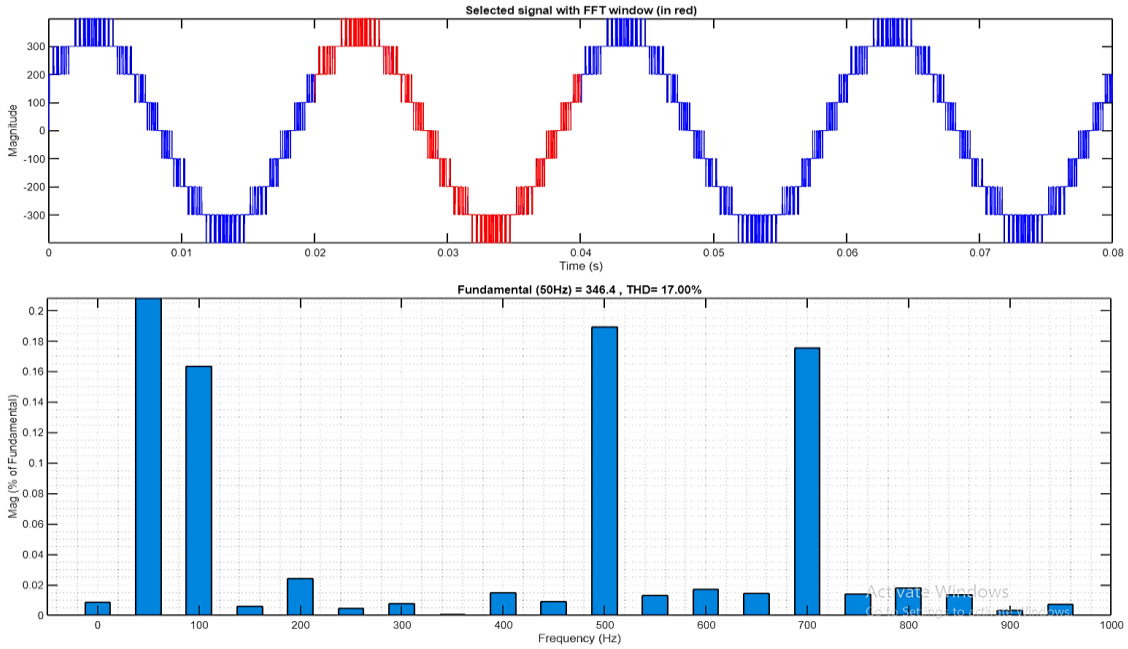

Figure 5. THD 5 level inverter

The LC filter used at the output of the inverter further filters the waveform to obtain a sinusoidal output and gets a better THD than the one obtained at the inverter output. The THD obtained after filtering from LC filter is as given in Figure 6. Figure 7 shows the PWM generation for seven level inverter's phase A of the cascaded inverter it is extended to all the three phases with the phase angle of the sinusoidal wave changed according to each phase.

The PWM generated from the comparison of modulating wave and the carrier wave is given to the appropriate switches of each phase and the output obtained from the three phase legs of the cascaded MLI is as given in Figure 8. The THD obtained from the seven level inverters line to line output voltage is as given in Figure 9. It can be observed that the THD is 10.72% for the 7-level inverter output voltage.

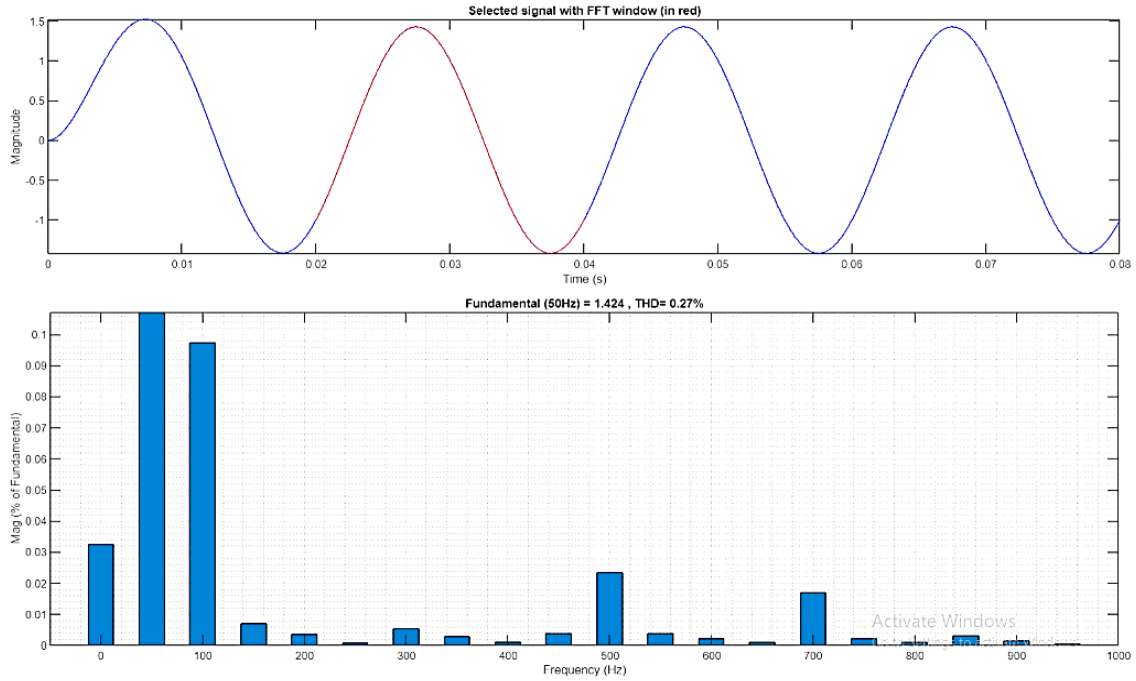

Figure 6. THD after LC filter

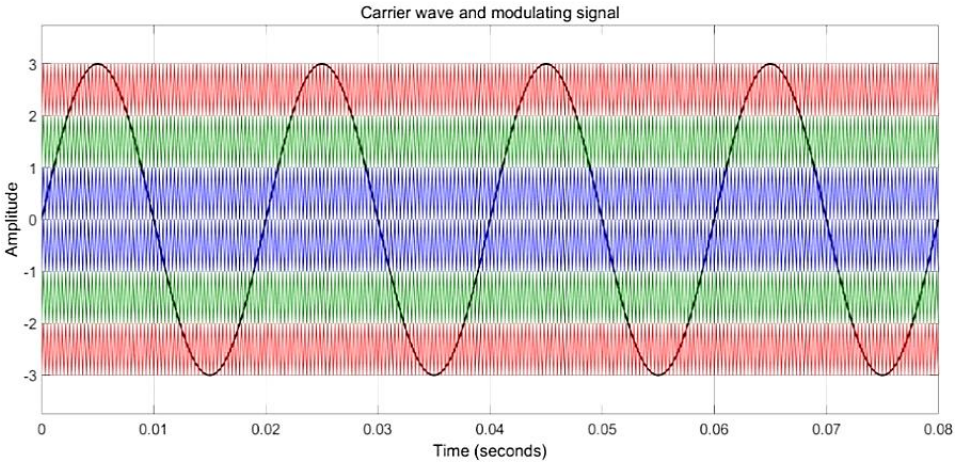

Figure 7. 7 level inverter carrier and modulating wave

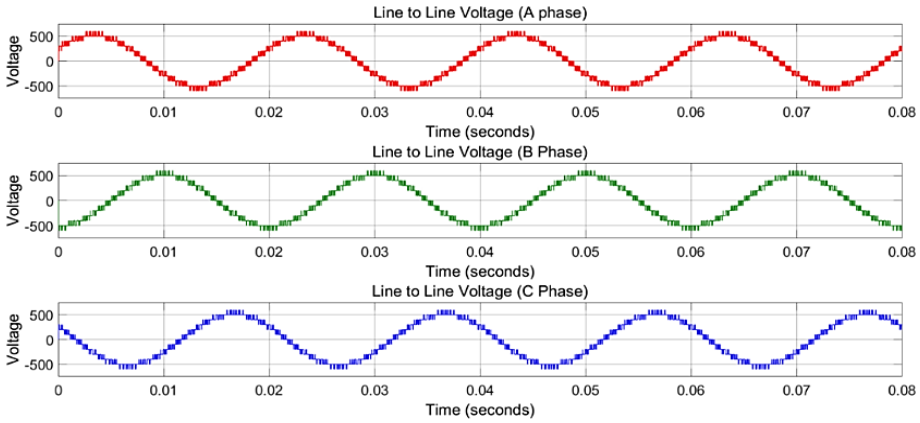

Figure 8. 7 level multilevel output

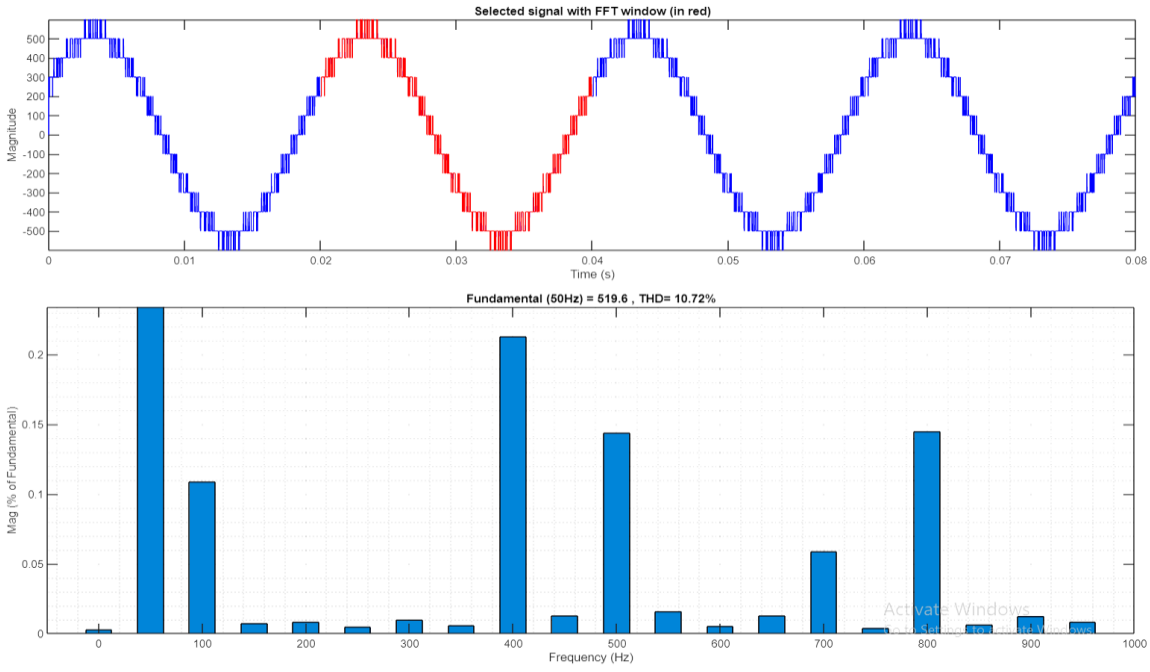

Figure 9. 7 level THD

The LC filter used at the output of the inverter further filters the waveform to obtain a sinusoidal output and gets a better THD than the one obtained at the inverter output. The THD obtained after filtering from LC filter in the 7-level inverter is as given in Figure 10. Figure 11 shows the PWM generation for nine level inverter's phase A of the cascaded inverter it is extended to all the three phases with the phase angle of the sinusoidal wave changed according each phase.

The PWM generated from the comparison of modulating wave and the carrier wave is given to the appropriate switches of each phase and the output obtained from the three phase legs of the 9 level cascaded MLI is as given in Figure 12. The THD obtained from the nine level inverters line to line output voltage is as given in Figure 13. It can be observed that the THD is 8.28% for the 9-level inverter output voltage. The LC filter used at the output of the inverter further filters the waveform to obtain a sinusoidal output and gets a better THD than the one obtained at the inverter output. The THD obtained after filtering from LC filter in the 9-level inverter is as given in Figure 14. It can be observed from the results obtained from the 5, 7 and 9 level inverters that there is a progressive improvement in the THD obtained for increase in the level of the multilevel inverter. A substantial reduction in the THD when the LC filter is used.

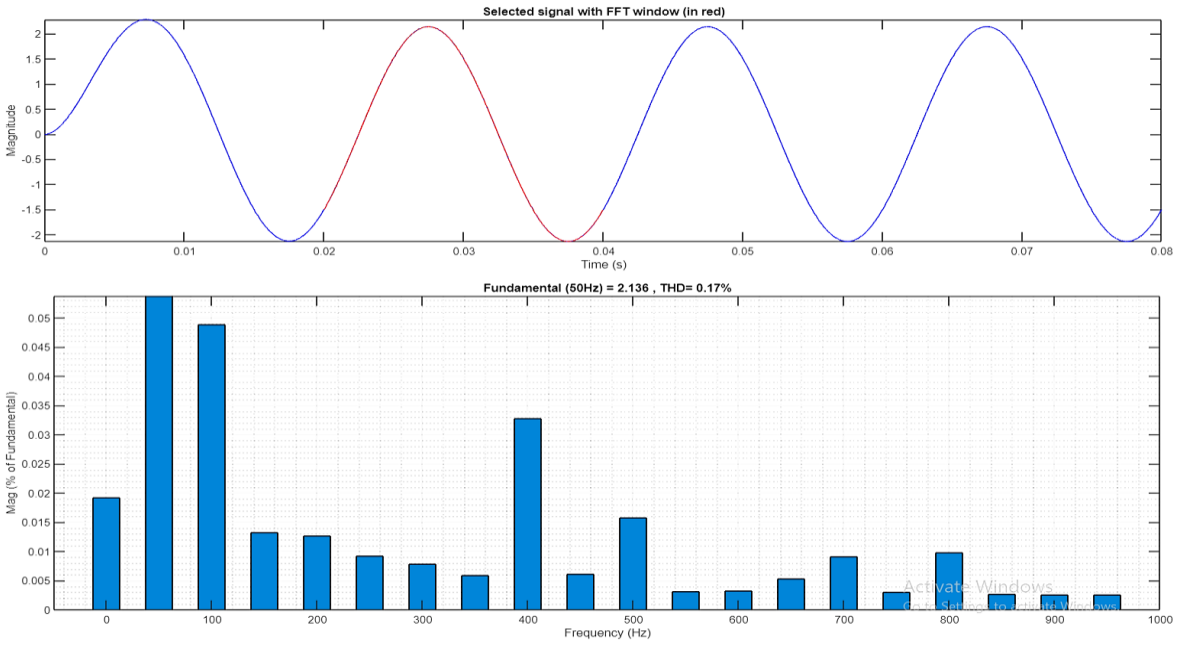

Figure 10. THD after LC filter 7 level

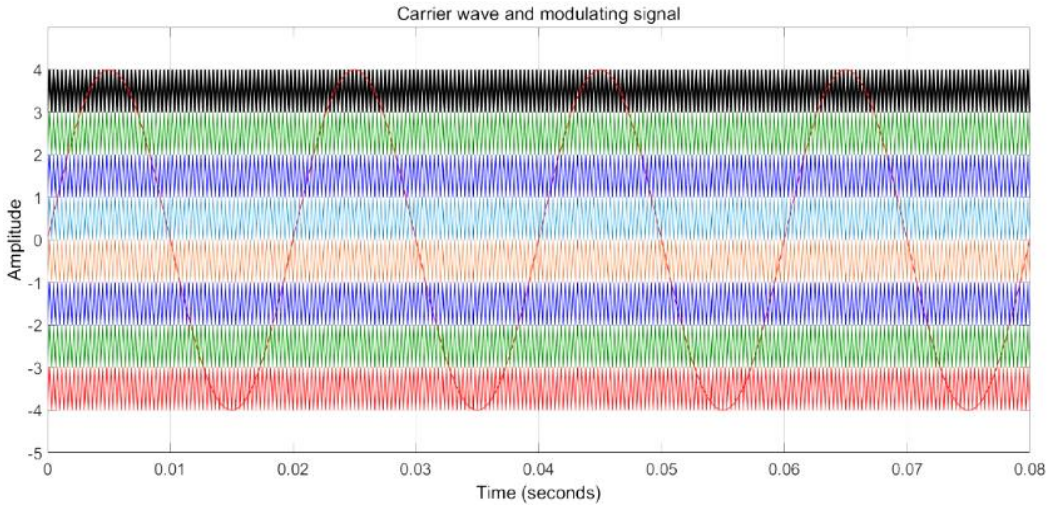

Figure 11. 9 level inverter carrier and modulating wave

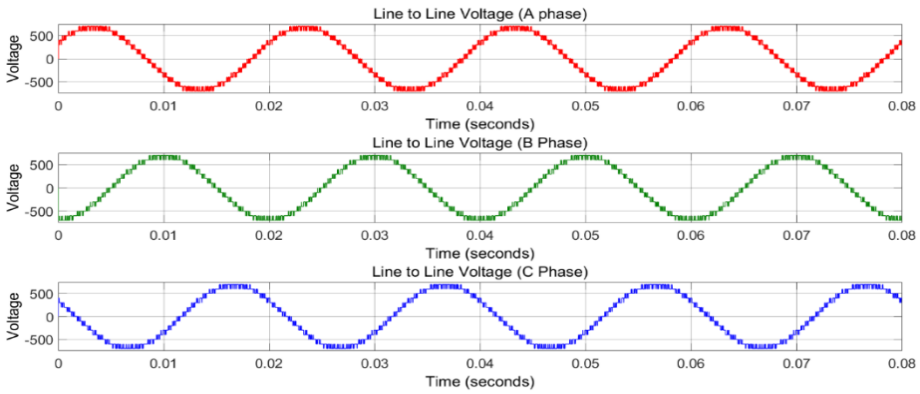

Figure 12. 9 level multilevel output

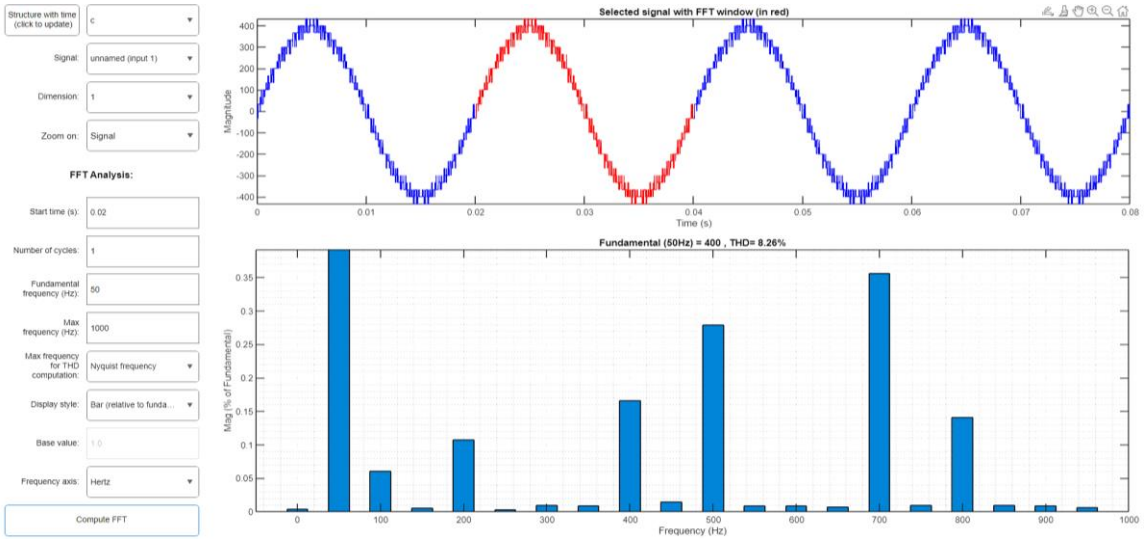

Figure 13. 9 level THD

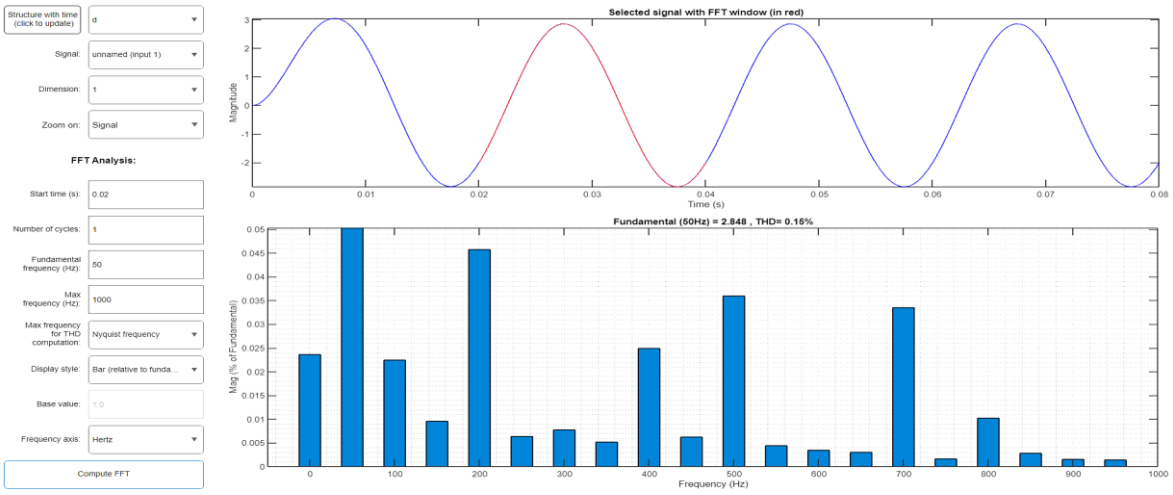

Figure 14. THD after LC filter 9 level

4. CONCLUSION

The implementation of the phase disposition, on 5-level, 7-level, and 9-level cascaded multilevel inverters has yielded significant insights into their performance. The MATLAB models developed for each inverter

configuration facilitated a comprehensive analysis of the total harmonic distortion (THD) outcomes across different levels. The results demonstrate that as the number of levels in the cascaded multilevel inverter increases, the THD decreases, indicating an improvement in the quality of the output waveform. Specifically, the phase disposition technique consistently provided the lowest THD across all levels, showcasing its effectiveness in minimizing harmonic distortion. The phase opposition method also performed well, although it exhibited slightly higher THD compared to phase disposition. The variable frequency carrier wave method showed promising results, particularly in dynamic applications where frequency variations are prevalent. In summary, this implementation confirms that advanced modulation techniques, when applied to higher-level cascaded multilevel inverters, significantly enhance output waveform quality by reducing THD. These findings underscore the importance of selecting appropriate modulation strategies to optimize the performance of multilevel inverters in various applications.

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BIOGRAPHIES OF AUTHORS

Nayana Gangadhara is currently pursuing her doctoral degree at Sri Siddhartha Academy of Higher Education, Tumkur, India. She has been a faculty member in the Department of Engineering at Sri Siddhartha Institute of Technology, Tumkur since September 2012. She holds a master's degree in Energy System Engineering from Visvesvaraya Technological University (VTU), Belgaum, India (2012), and a bachelor's degree from VTU, Belgaum, India. With 12 years of experience in teaching and research, her areas of interest include power electronics, power systems, and energy systems. She can be contacted at email: nayanassittumkur@gmail.com.

Savita D. Torvi is a professor in the Department of Electronics and Telecommunication Engineering since 1999. She holds a master's degree in digital Electronics from Karnataka University, India (1997), and completed her Ph.D. in security using image steganography from Sree Siddhartha University, India. With over 25 years of experience in teaching and research, her areas of interest include image steganography, cybersecurity, VLSI, and embedded systems. She can be contacted at email: savitadtorvi@gmail.com.