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# Single stage boost cascaded multilevel inverter for photovoltaic applications

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**ABSTRACT**

This article discusses a high-gain five-level SL-SC-based cascaded multilevel qSBI (qSBMLI) for photovoltaic applications. A combination of switched inductor and switched capacitor structure produces a boost at high levels. Two identical SL-SC-based qSBI modules are cascaded and powered with two stiff DC voltage sources of 18 V each. The DC voltage of 18 V obtained from two different DC voltage sources is applied to each module. An 18 V DC voltage is supplied to a single module-A, which produces a DC link voltage ($V_{PN}$) of about 240 V at the inverter's input side. The modulation index (MI) is selected as 0.68, and the duty ratio is kept at 0.3. The boost factor is obtained as 13.3, and the load voltage of 150 V is achieved across the resistive load. Hence, the voltage gain is 6.9. The proposed topology delivers 337 W of power to the load at an efficiency of 73%. The complete circuit topology and its operations are analyzed in MATLAB/Simulink. The control signals for the power switches are produced using the field programmable gate array (FPGA) SPARTAN 3E Kit. When the proposed circuits are analyzed and compared with the existing classical topologies, the proposed one shows the superior performance.



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## 1. INTRODUCTION

In this modern era, non-conventional power-generation systems are adopted instead of conventional energy sources to generate electrical energy [1]. Due to environmental concerns, more consideration is given to energy harvesting from solar photovoltaics [2]. Semiconductor technology development paves the way for developing novel power electronic converters. In that aspect, various power conditioner circuits such as DC-DC converters, voltage and current source inverters, controlled and uncontrolled rectifiers, and AC-AC converters are utilized as power conditioners to convert the availed voltage into a useful format. The classical voltage source inverters find vast applications in industries such as uninterruptible power supplies, electrical drives, electric vehicle applications, and distributed power generation [3]. However, these inverters have a few drawbacks, including short circuit issues, the significant harmonic content of the output voltage, and power quality issues when these converters are connected to grid-connected solar systems [4]. Moreover, a voltage source inverter (VSI) reduces the available DC voltage. Whenever a voltage more than the available DC voltage is needed, classical VSI cannot be suitable [5].

The classical VSI is coupled to a simple DC-DC boost converter to provide the necessary boost and inversion action. It leads to complex two-stage circuitry in cascaded form [6]. However, the classical VSI is more significant in meeting the wide range of voltage fluctuations [7]. In a two-stage cascaded boost inverter,

a conventional DC–DC boost converter is used instead of a transformer as shown in Figure 1 which has many drawbacks mentioned in the literature.

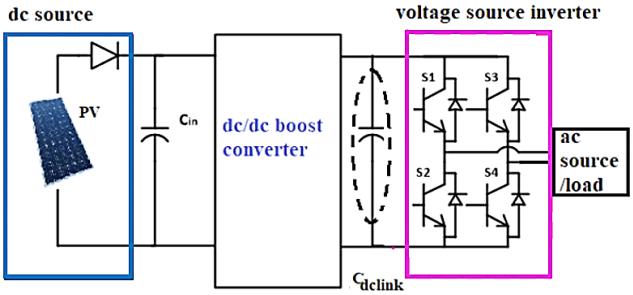


Figure 1. Dual-stage DC-DC boost voltage source inverter

The multilevel inverter (MLI) concept and its associated switching techniques are gaining more attention among researchers and manufacturers [8]. Multilevel waveforms can address large voltage transients due to dynamic loading conditions [9]. Besides, the multilevel approach provides good power quality, low switching losses, and good electromagnetic compatibility (EMC) [10]. An m-level of staircase-type voltage waveform is produced with MLIs [11]. The output voltage quality is better with more levels [12]. Different types of MLIs are available in the literature. The cascaded type MLI is better than other inverter topologies. neutral point clamped (NPC) [13] and flying capacitor (FC) [14], [15] require more significant number of active and passive switches. Hence, cascaded H-bridge (CHB) topologies are good candidates compared to NPC and FC topologies. The output load voltage of the standard MLI is lower than the source voltage, which is its primary disadvantage. MLI must be cascaded with a DC-DC boost converter to get the required voltage. However, the conventional boost converter switch becomes a major problem that raises the cost of the system. A linked inductor may occasionally replace the average inductor and capacitor used in the traditional boost converter, switched inductor cell, switched capacitor cell, or a mix of the two [16]. Galvanic isolation is necessary for some RES-based systems, which raises the system's cost and lowers its overall performance. Therefore, single-stage boost inverters can resolve the problems with the two-stage boost inverters.

To overcome the drawbacks of the DC-DC boosted VSI, Z-source inverter (ZSI) and its derivative structures are presented in [17], [18]. The ZSI and its modified structures, such as qZSI, SL-ZSI, and SC-ZSI, are presented in [19]. The ZSI and its modified structures are discussed in the literature to meet the high voltage boost and gain requirements in a single stage [20]. The specific feature of single-stage boost inverters is that they can boost and invert in a single stage due to the presence of the shoot-through state [21]. But ZSI/qZSI topologies have issues where the low input DC sources, such as photovoltaic (PV) and fuel cells, must be converted to high AC voltage [22]-[24]. Integrating the Z-source network and its modified structures with various MLI circuits is suggested to overcome the drawbacks of traditional MLI [25]-[29]. MLIs are gaining attention to meet the high-power demands. However, CHB-type ZSIs and qZSIs require multiple modules, which over-size the system. A simple inverse Watkins-Johnson topology-based inverter is proposed in [30] to overcome the issues with CHB qZSI. In [31], a thorough analysis of switched boost inverters, or SBIs, is provided. Various SL cells, SC cells, voltage multipliers, and voltage lifting techniques are added with SBI and its derived systems. The CHB-based qSBI is presented in [31]-[33]. There will be a high content of voltage ripple at the input side of the DC-link voltage due to the presence of an inductor or switched inductor in series with the source voltage. The trans switched boost inverter is suggested in [34]. The voltage fed ZS/qZSI and qSBI are proposed based on switched-inductor (SL) cells [34]. The voltage stress across switches, capacitor and diodes is high in the case of trans-qSBI [34], SL-qSBI [35], and SC-qSBI [36], [37]. The cascaded H-bridge type three-phase quasi-switched boost inverters are also proposed in [38], [39]. Mollajafari *et al.* [40] introduced a new voltage-multiplier-based converter is proposed for sustainability applications. The three-phase qSBI based on the SL-SC combination is analyzed in [41]. A five-level NPC inverter dynamic voltage boosting is presented in [42]. A non-isolated qZ-source MLI with high gain boost is suggested in [43]. A single-source cascaded MLI with a voltage-boost submodule with the specific feature of continuous source current for PV applications is discussed in [44]. In this research article, a combination of switched inductor and switched capacitor structure-based qSBMLI is presented to boost the available voltage along with the qSBI in a cascaded manner. The cascaded inverter switches are powered by switching pulses produced via the basic boost phase-shifted pulse width modulation (PWM) technique. The following is how the article is organized: i) The suggested circuit's topology and modes of operation are described in section 2; ii) The steady-state analysis is explained in section 3; and iii) The passive element design is discussed in section 4; iv) Section 5 discusses the

modulation strategy adopted in the simulation study; v) The simulation results are presented in section 6; vi) The experimental findings are presented in section 7; vii) Section 8 details the performance evaluation of the five-level SL-SC cascaded qSBMLI with other MLIs; and viii) and the references are included after the article's conclusion in the last section.

## 2. PROPOSED CIRCUIT TOPOLOGY

Figure 2 presents the single-phase five level SL-SC cascaded qSBMLI. Two identical modules are connected in a cascade in this proposed novel structure. Each module has a switched capacitor and switched inductor cells, an H-bridge inverter in each module and a LC filter connected to a resistive load. The output voltage of modules 1 and 2 combined to form a five-level AC output voltage. The output voltage levels can be increased by connecting some more identical modules. Since both the modules are identical in nature, module-A alone is considered for analysis. The circuit works in shoot through and non-shoot through states. The operating modes are shown in Figures 3(a) and 3(b). During shoot through state as depicted in Figure 3(a), both the power devices in a single leg or both legs are fired on along with $S_{01}$. Diodes D2, D4, and D6 are turned on. Also, capacitor C2 discharges through C1 and charges both inductors L1 and L2. Diodes D1, D3, and D5 are turned off. The shoot through period is DTs where D is the shoot through duty ratio and Ts is the total time period for switching. During non-shoot state, the inductors L1, L2, the capacitor C1 discharges through the capacitor C2. Diodes D1, D3, and D5 are on and D2, D4, D6 along with the boost network active switch S01 are off. Output power is available across the load in this mode as shown in Figure 3(b).

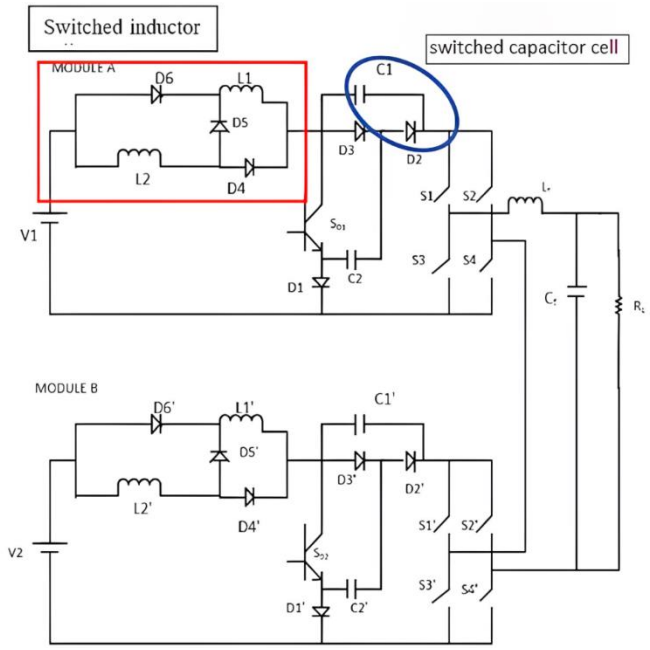


Figure 2. Cascaded five-level SL-SC-based qSBMLI

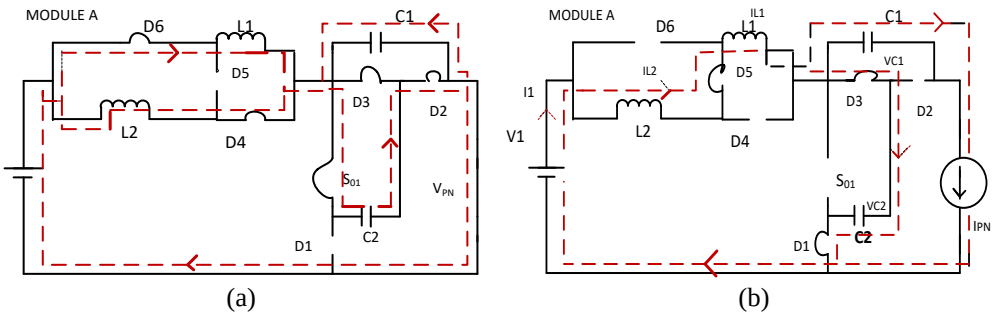


Figure 3. Modes of operation of the proposed inverter: (a) shoot-through condition-module 1 and (b) non-shoot through state condition module 1

## 3. STEADY STATE EXAMINATION OF PROPOSED TOPOLOGY

Module A of the five-level cascaded H-bridge type-based SL-SC qSBI is considered for analysis. During the shoot-through period [15], the voltage (VL1, VL2) across the inductors (L1, L2) is given by (1) and (2).

$$V_{L1} = V_{L2} = V_1 + V_{C2} \quad (1)$$

$$V_{C1} = V_{C2} \quad (2)$$

The voltage at the input side of the H-bridge inverter is obtained as (3).

$$V_{PN} = 0 \quad (3)$$

During the active period, inductor voltage (VL1) is derived by (4).

$$V_{L1} = V_1 - V_{C2} - V_{L2(NST)} \quad (4)$$

The voltage across the inductor L2 is given by (5).

$$V_{L2(NST)} = L_2 \frac{dL_2}{dt} \quad (5)$$

The current through the capacitor (C2) is given by (6).

$$I_{C2} = I_1 - I_{PN} \quad (6)$$

Peak DC link current ($I_{PN}$) is related as in (7).

$$I_{C1} = -I_{PN} \quad (7)$$

$$V_{PN} = V_{C1} + V_{C2} \quad (8)$$

The capacitor voltages VC1 & VC2 are the same, and it is derived as (9).

$$V_{C1} = V_{C2} = \frac{1+D}{1-3D} V_1 \quad (9)$$

The maximum voltage across the inverter input side during the active state is the addition of the voltage across both the capacitors (C1 and C2).

$$V_{PN} = V_{C2} + V_{C2} = \left[\frac{1+D}{1-3D} + \frac{1+D}{1-3D}\right] V_1 \quad (10)$$

The boost factor is derived as (11).

$$B = \frac{V_{PN}}{V_{in}} = \frac{2(1+D)}{1-3D} \quad (11)$$

## 4. PASSIVE COMPONENT DESIGN

Similar to conventional multilevel inverter topologies, this novel inverter also generates low-order ripple frequency content at the input side of the inverter. The (12) and (13) are used to find the high-frequency ripples. The proper adoption of closed-loop control can eliminate the low-frequency ripples.
The inductor ripple currents of L1 and L2 are given by (12).

$$\Delta I_{L_1} = \frac{V_{in} + V_{C_2}}{L_1} DT \quad (12)$$

$$\Delta I_{L2} = \frac{V_{in} + V_{C_2}}{L_2} DT \quad (13)$$

Where T is the switching period of the inductors. The capacitor ripple voltages are expressed by (14) and (15).

$$\Delta V_{C_1} = \frac{(I_{L1} + I_{L_2})}{C_1}(1 - D)T \quad (14)$$

$$\Delta V_{C_2} = \frac{(I_{PN})}{C_2}(1 - D)T \quad (15)$$

## 5. MODULATION STRATEGY AND SWITCHING PULSES

Generally, various modulation schemes are adopted to control the inverter's working [45]-[49]. This proposed work adopts a phase-shifted sinusoidal PWM method to generate the PWM signals. Figure 4 depicts the simple boost modified phase-shifted PWM referred to in [31] to generate the firing signals for the devices. The switching pulses for the boost network and the inverter bridges of module 1 are presented in Figure 5. It is evident from Figure 5 that a single leg's upper and lower devices are turned on simultaneously during the shoot-through state. It is the leading cause of boosting action. In order to generate the AC output voltage with a frequency of 50 Hz, the switching frequency of 20 kHz is selected in this study, and the triangle pulse at that frequency is compared with a sinusoidal signal at 50 Hz.

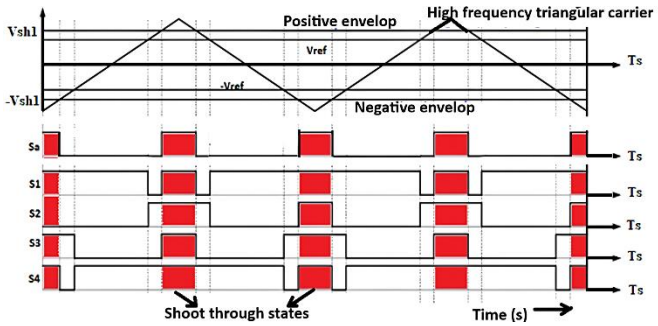


Figure 4. Illustration of the simple boost phase-shifted PWM strategy of module 1

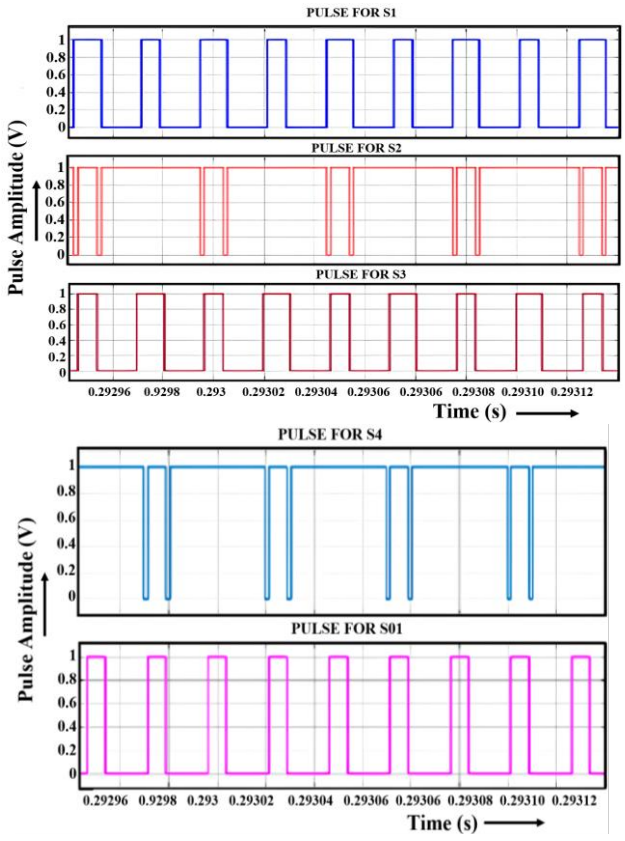


Figure 5. Pulses for the inverter bridge and boost network switches

## 6. REALIZATION OF PROPOSED INVERTER AND SIMULATION OUTPUTS

This section discusses the simulation and experimentation results of the proposed topology. The design specifications of the proposed circuit are as follows: The source voltage of each module is chosen as 18 V. The inductors L1, L2, L1', and L2' are calculated as 1.5 mH and the capacitor values C1, C2, C1', and C2' are chosen as 470 µF. The full design values are tabulated in Table 1. The inverter circuit is simulated in the MATLAB/Simulink platform using the following design specifications. The source voltage of 18 V of a single module 1 produces the DC link voltage ($V_{PN}$) of about 240 V. The duty ratio is chosen as 0.3, and the switching frequency is 20 kHz. The capacitor voltages (VC1 & VC2) are obtained as 120 V each, as shown in Figure 6. As per the theoretical validation, the sum of both capacitor voltages is available across the DC link of the H-bridge inverter bridge, as depicted in Figure 7, which gives almost a boost factor of 13.3.

The boosted DC link voltage is inverted to a peak AC voltage of about 220 V across the inverter module 1 at the modulation index of 0.68 and is presented in Figure 8. The five-level AC voltage of 420 V, combining both the modules, is available across the resistive load terminals. By optimally designing an LC filter, the total harmonic distortion (THD) content of the inverter AC output voltage can be reduced, and a proper sine wave can be obtained across the load terminals.

Table 1. Design specifications

| Design parameters | Values | Design parameters | Values |
|---|---|---|---|
| Input voltage (Vdc1, Vdc2) | 18 V | Modulation index (M) | 0.68 |
| Inductors (L1, L2, L1', L2') | 1.5 mH | Switching frequency (fs) | 20 kHz |
| Capacitors (C1, C2, C1', C2') | 470 µF | Output frequency (fo) | 50 Hz |
| Shoot through duty ratio (D) | 0.3 | | |

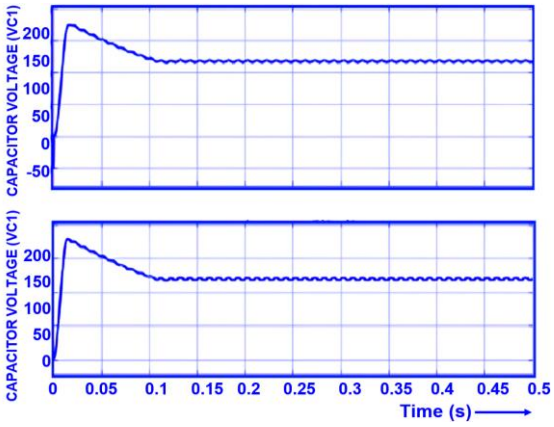


Figure 6. Capacitor voltages of module 1

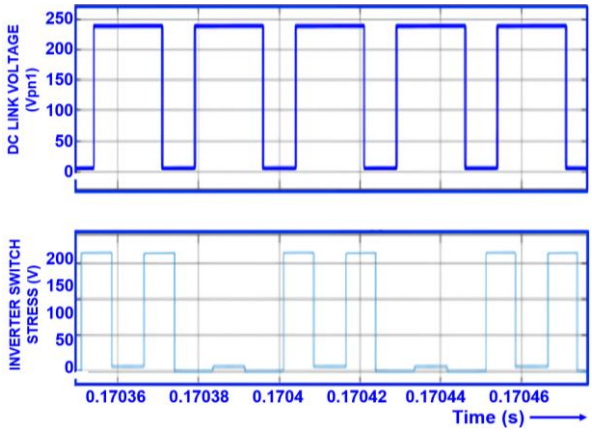


Figure 7. DC link voltage ($V_{PN1}$) and inverter voltage stress (Vs)

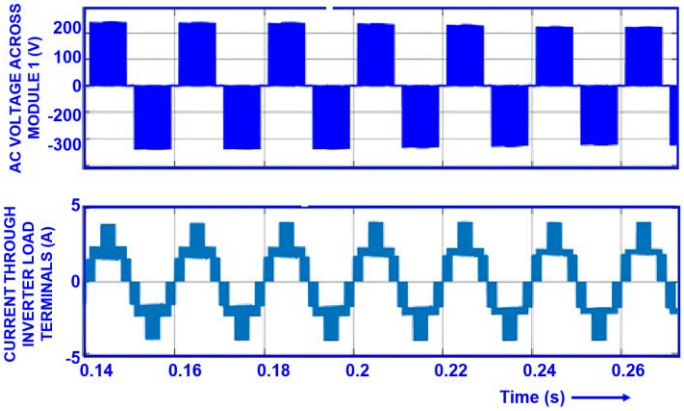


Figure 8. Unfiltered inverter terminal voltage of module 1

## 7. EXPERIMENTAL INVESTIGATION OF PROPOSED TOPOLOGY

Table 2 displays the design specifications for the inverter's prototype model. A laboratory-built prototype model of a cascaded five-level qSBI based on SL-SC is constructed to verify the effectiveness of the suggested inverter architecture. As per the expression in (12)-(15), respectively, the design values of the capacitances (C1 & C2) and inductances (L1 & L2) are selected. The (FPGA) SPARTAN 3E generates the PWM pulses for the switches, and the TLP250 driver IC is used to drive the FPGA-generated pulses.

Figure 9 depicts the implementation of the gate driver, and the experimental prototype of the cascaded five-level qSBI topology based on SC-SL is shown in Figure 10. Figure 11 displays the pulses that are used to fire the MOSFET devices. Figure 12 displays the inverter terminal voltage that was acquired through module 1. Figure 13 shows the five-level peak output voltage waveform of approximately 150 V. Two different regulated power supplies power the two inverter topology modules. Each module in the hardware implementation has a source voltage of 18 V.

Table 2. Hardware design parameters

| Parameters | Specification |
|---|---|
| Input voltage | 18 V (each module) |
| Resistor | 100 Ω |
| Power IGBT- H20R1203 | 1200 V |
| Driver circuit- TLP250 | 20V, 1.5 A |
| Switching frequency (fS) | 20 kHz |
| Duty ratio of shoot through (D) | 0.3 |
| Modulation index (M) | 0.68 |
| Inductors & capacitors | 1.5 mH, 470 µF |

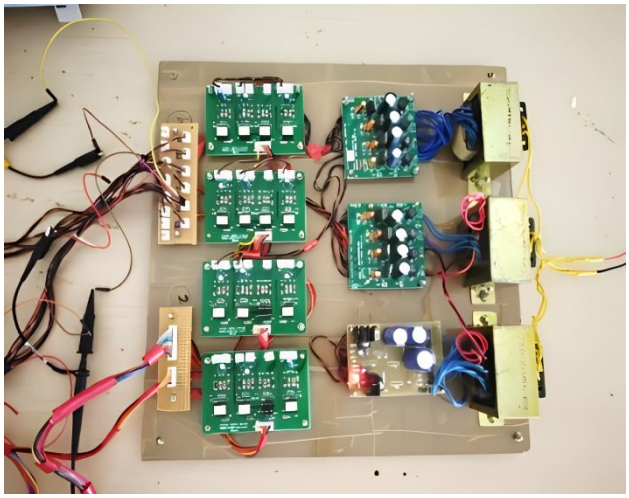

Figure 9. Gate driver implementation

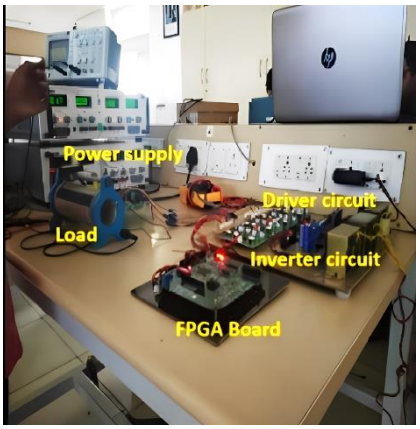


Figure 10. Experimental setup

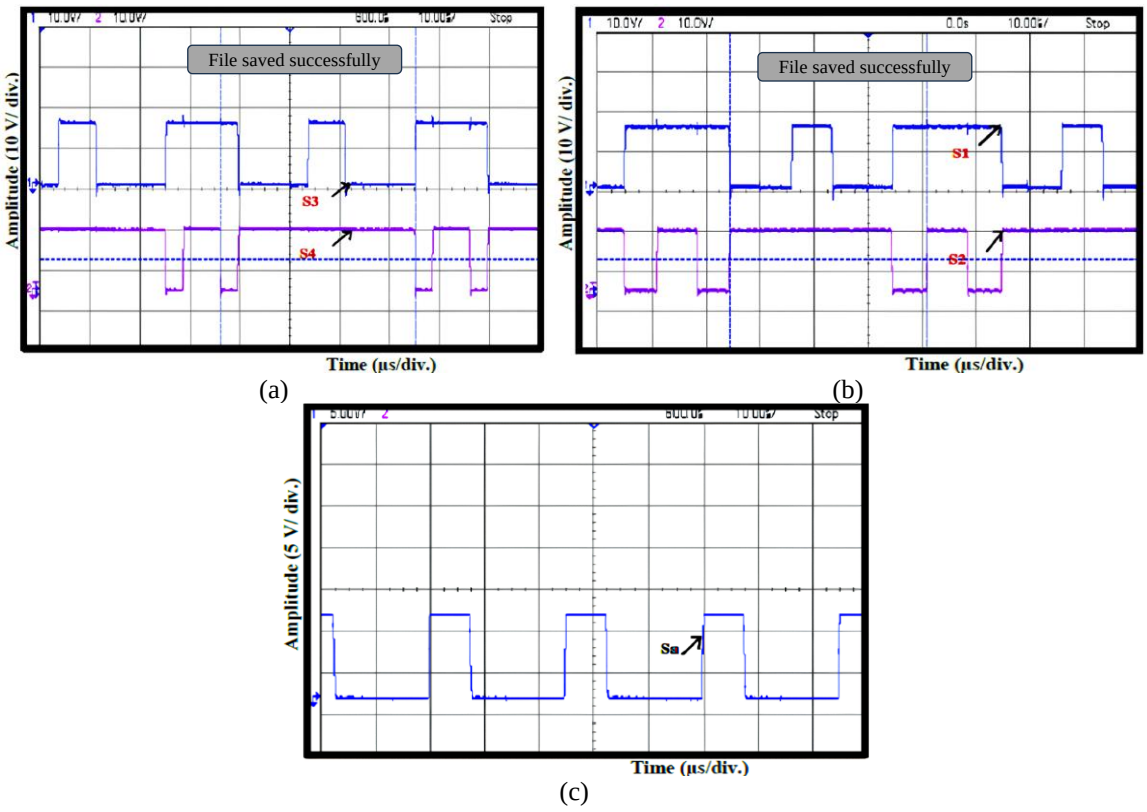


Figure 11. Pulses produced in the FPGA board: (a) pulses for S1 & S2 switches, (b) pulses for S3 & S4, and (c) pulses for the boost network switch Sa

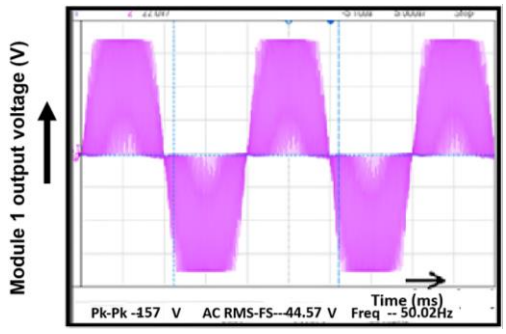


Figure 12. Inverter terminal voltage waveform of module 1

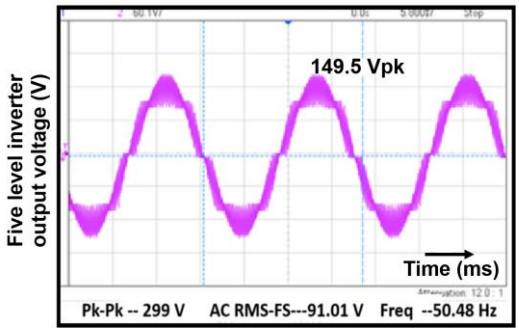


Figure 13. Five-level AC output voltage

## 8. PERFORMANCE ANALYSIS OF PROPOSED TOPOLOGY WITH OTHER CONVENTIONAL TOPOLOGIES

The performance assessment of the proposed topology is presented in this section. The comparison made with the same duty ratio (D) and modulation index (M) is discussed in the following section. Table 3 presents the components comparison of the SL-SC-based cascaded five level qSBI topology with other cascaded MLI circuits. It is inferred that the component count is not much different even if the boost factor is attained high in the proposed topology. Because the system will have fewer passive components, it will be smaller, lighter, and less expensive to attain higher voltage with more levels. Table 4 lists the performance of different topologies concerning input current profile, ripple input current, voltage gain, and boost factor.

The plot of the shoot through duty ratio (D) against the boost factor (B) for the conventional qSBI, SC-qSBI, SL-qSBI, and SL-SC qSBI single module topologies are shown in Figure 14. It is clear that the SL-SC based circuit achieves the largest boost when compared to other qSBI derived topologies with a comparable duty ratio. At a duty ratio of 0.3, the boost factor 13.3 is achieved. The boost factor for the

normal inverter circuit is high for small duty ratio value. Even if there is any unbalance, the peak DC link voltage is maintained by regulating the shoot through duty ratio value so that inverter output will remain the same. Hence, five level SL-SC based qSBMLI can overcome the issue associated with the traditional cascaded H-bridge inverter. The DC link voltage is obtained as 240 V and a five-level output peak voltage is obtained as 168 V in theoretical.

Inductor (L1) connected with the input supply produces ripple content in the input current and can cause low efficiency especially in renewable energy applications. It can be minimized by the optimal design of the inductors in the switched inductor cell. The output power (W) and efficiency (%) plot is depicted in Figure 15. Moreover, in the high boost conversion, the power devices and capacitors must withstand high voltage stress. Hence the optimum selection of the power switches and capacitors is mandated. By judiciously fixing the carrier frequency and duty ratio, the passive element's size can be further reduced. Based on the available source voltage, the proposed circuit can be used to achieve better efficiency.

Table 3. Components comparison of circuit topologies

| Components | DC-DC boosted VSI | Cascaded qZSI [31] | Five level qSBI [33] | SC based qSBI [34] | SL based qSBI [36] | SL-SC qSBI (Proposed) |
|---|---|---|---|---|---|---|
| Diodes | 10 | 10 | 12 | 14 | 10 | 12 |
| Capacitors | 2 | 4 | 2 | 4 | 2 | 4 |
| Inductors | 2 | 4 | 2 | 2 | 4 | 4 |
| Switches | 10 | 8 | 10 | 10 | 10 | 10 |

Table 4. Comparison of module 1 of various qSBI configurations

| Topological structure | Boost factor (B) | Input current (Iin) | Input current ripple (ΔIin) |
|---|---|---|---|
| Quasi ZSI [31] | $\frac{1-D}{1-2D}$ | Discontinuous | low |
| Classical qSBI [33], [44] | $\frac{1}{1-2D}$ | Discontinuous | High |
| Switched capacitor-based qSBI [34] | $\frac{2}{1-2D}$ | Continuous | Low |
| Switched inductor-based qSBI [36] | $\frac{1+D}{1-3D}$ | Continuous | High |

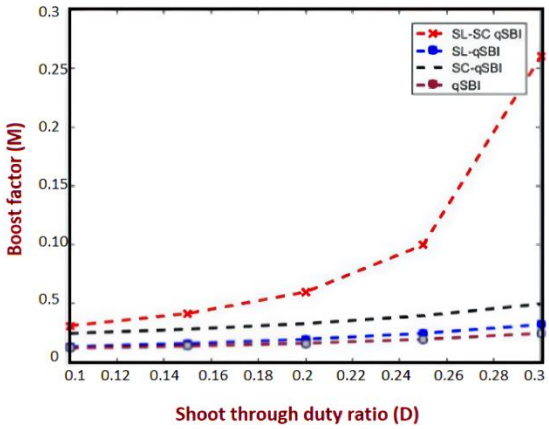


Figure 14. Shoot through duty ratio (D) vs boost factor (B)

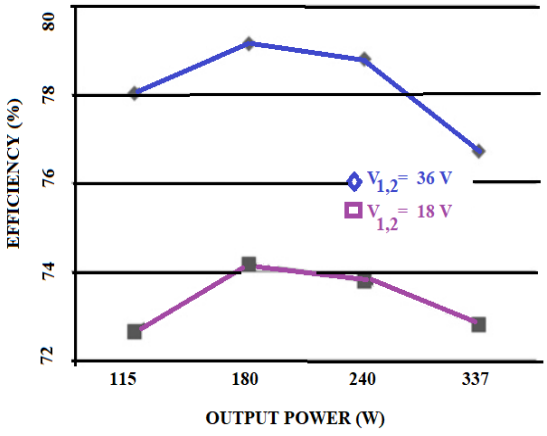


Figure 15. Output power (W) vs efficiency (%)

## 9. CONCLUSION

The present study provides a quick overview of many conventional single-stage boost inverter topologies, component counts, benefits, and drawbacks. The proposed circuit's operation, steady state, pulse width modulation method, and performance assessment are thoroughly described. The five-level cascaded qSBI based on the switched capacitor and switched inductor has the advantages of both qSBI and the SL-SC combination for achieving a high gain and high-quality output load voltage. The duty ratio of the shoot-through state is efficiently controlled using the modified simple boost phase-shifted sinusoidal PWM technique. Higher gain and boost factors can be achieved with a lower shoot-through duty ratio D of 0.3. Compared to a standard cascaded MLI, the SL-SC-based inverter has lower switch stress and high-quality

output load voltage with lower THD due to a shoot-through condition. The proposed system can be extended along with a suitable closed-loop control to overcome the voltage imbalance and load dynamics that occur in the grid-connected PV systems.

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## AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

| Name of Author | C | M | So | Va | Fo | I | R | D | O | E | Vi | Su | P | Fu |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
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| M. Sujatha | | | ✓ | ✓ | ✓ | ✓ | ✓ | | | ✓ | ✓ | | ✓ | |

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

## CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

## DATA AVAILABILITY

Data availability is not applicable to this paper as no new data were created or analyzed in this study.

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