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Proposed high gain single DC-source SC-MLI topology for solar PV grid integration applications

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ABSTRACT

Multilevel inverters (MLIs) are a key solution for converting DC to AC power. In this article, an improved single-source SC-MLI topology is developed for solar PV applications. It consists of 12 unidirectional switches, 3 capacitors, and 3 diodes to provide sextuple voltage boosting with a lower cost function. Since the capacitor's voltage is self-balanced, there is no need for an additional circuit or sensors, bringing down the circuit's complexity. A simple and fundamental frequency-based control strategy, nearest-level pulse width modulation, is applied to assess the viability of the proposed topology. As a result, the proposed topology has an efficiency of over 97%, and it can generate 13 levels with a total harmonic distortion (THD) of 6.51%. Comparative analysis is performed to show the feasibility of the proposed topology which outperformed other 13-level similar topologies in terms of component count, cost factor, and boosting factor. The proposed topology's performance is evaluated under static and dynamic loads. Furthermore, the thermal analysis is performed using PLECS software to determine the efficiency of the circuit topology. Finally, the feasibility of the proposed circuit is verified for solar PV application.

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1. INTRODUCTION

Renewable energy sources (RESs) based power generation has been a prominent area of research due to their viability and environmental concerns. Therefore, RESs-based power generation has been a key and attractive area of research due to its feasibility and concern for the environment. Hence, the demands for power electronic converters have been drastically increased with renewable energy sources to regulate the output of RESs, including solar photovoltaic arrays, electric vehicles (EVs), motor drives, and unified power flow controllers. Here, power electronic converters are interfaced with RESs to obtain a desired and controlled output for the specific applications. Power electronic converters can be divided into four types: DC/DC, AC/DC, DC/AC, and AC/AC converters. A DC/AC converter, also known as an inverter, is used for power conversion. Primarily based on the output level, the DC/AC converter or inverter can be categorized as a two-level and multilevel inverter. Compared to traditional two-level inverters, multilevel inverters (MLIs) perform better due to their improved power quality, reduced total harmonics distortions (THD), lower dv/dt stress, and

higher modularity [1]-[3]. Also, the requirements of the filters are reduced for medium voltage and higher power applications.

The classical MLIs can be categorized into three types: neutral point clamped, flying capacitor, and cascaded H-bridge [4], [5]. These traditional topologies are widely used in a wide range of industrial applications, such as electric drives, renewable energy, electric vehicles, and medium- to high-power applications. However, the NPC and FC-based MLI topologies require a higher component count and suffer from the capacitor unbalance issue. Furthermore, one of the most critical barriers with classical MLIs is that as the output level increases, the component count increases drastically. A higher component count implies higher losses, which reduces the efficiency and reliability of the converter. Although cascaded H-bridge (CHB) MLIs are reliable and have a modular structure, they require a higher number of isolated DC sources to maintain a higher output level. Therefore, the size, cost, and complexity increase as the component count increases. In addition, the traditional MLIs do not provide any boosting feature at the output, demanding two-stage conversion, which is more expensive, larger in size, and less efficient than single-stage conversion.

Therefore, recent research has shifted towards switched capacitor (SC) based MLIs to resolve constraints of traditional MLIs, including component count, capacitor voltage balancing issues, and a lack of boosting ability. The SC-MLI topologies are more efficient, offer lower dv/dt stresses, have fewer components, and provide high gain. In addition, due to their self-balancing ability, they do not require any auxiliary or complex control algorithm to balance the capacitor voltage. The SC-MLI topology's boosting ability enables it to use low-voltage sources in high-voltage applications [6]-[8]. As a result, the output voltage can be increased, eliminating the need for DC-DC converters, which brings down the overall size and cost of the system while improving the overall efficiency. The single-source 7-level inverter in [9] achieves a boosting factor of 1.5 using 2 DC-link capacitors, a floating capacitor, 8 unidirectional switches, and 2 bidirectional switches. A single-source 11-level inverter in [10] can produce a gain of 2.5 using 12 switches and 4 capacitors. The main advantage of this inverter is its low blocking voltage on semiconductors. Another single-source 7-level inverter in [11] with a single floating capacitor and 9 unidirectional switches provides a gain of 1.5 but requires a complicated strategy for charge-balancing a floating capacitor. A single-source 9-level inverter proposed in [12] uses a diode, 2 switched capacitors, and 6 unidirectional, and 2 bidirectional switches for double gain, but its main drawback is that 4 switches can withstand Vo, max, leading to a large total blocking voltage (TBV). Siddique *et al.* [13] presents a 13-level inverter with 8 switches and 3 DC sources for unity gain. In contrast, a switched capacitor single sources inverter in [14] generates a multilevel voltage by changing supplies in parallel and series mode with boosted output voltage, producing a 17-level with 13 switches and 4 capacitors. One significant problem with single DC-source SC-MLI topology is that more switches and capacitors are needed to achieve higher output voltage levels, reducing the circuit's effectiveness, and reliability. Therefore, the optimal design of the circuit is required to overcome such complexities.

The work presents an SC-MLI topology with reduced device count, offering 13-level output voltage with sextuple boosting. It uses two half bridges for negative steps and natural charge-balancing of capacitors for ease of control. The converter can be generalized for enhanced gain and levels, making it suitable for PV-based standalone systems. The paper's structure is organized as follows: the circuit's configuration, total standing voltage, capacitors sizing for efficient converter performance, and control technique are discussed in section 2. Furthermore, the performance analysis of the proposed topology using MATLAB/Simulink for different loading conditions is presented in section 3. Thermal analysis is carried out using PLECS software in section 4 to determine the efficiency of the circuit topology. To check the feasibility of the proposed circuit, a comprehensive analysis is discussed with similar existing topologies in section 5. The application of the circuit topology with solar PV and grid Integration is discussed in section 6.

2. DESCRIPTION OF THE PROPOSED SC-MLI TOPOLOGY

2.1. Circuit configuration

This work proposes an improved single-source SC-MLI topology, as shown in Figure 1. It consists of 12 unidirectional switches, 3 capacitors, and 3 diodes. Table 1 shows the different modes of switching states for the operation of the proposed topology during one complete cycle. It can generate 13-level output voltage with sextuple boosting ability in output voltage. The capacitor C_1 is charged to $V_{dc,}$ and the capacitors C_2, and C_3 are charged to 2 V_{dc} by coupling them in parallel to voltage sources and later discharged in series with the load.

2.2. Switching technique

Pulse width modulation techniques are classified into two categories based on switching frequency: low (fundamental) and high-frequency switching schemes. The nearest-level pulse width modulation technique comes under fundamental or low-frequency switching schemes [15]-[17]. Because of simplicity and lower switching losses, this control scheme is used for controlling the output voltage and verifying the viability of

the proposed circuit in fixed and dynamic load conditions, as shown in Figure 2. For obtaining 13 levels of output voltage, the switching mechanism of each switch (S_1-S_{12}) is shown in Figure 3.

2.3. Total standing voltage (TSV)

The standing voltage across the switches plays a significant role in designing the power converter [18]. A larger standing voltage requires higher-rated semiconductor switches, which significantly raises the cost of the power converter. The total sum of the maximum individual standing voltage across the switches during the off state is described as the total standing voltage. The individual maximum standing voltage across the switches is shown in Figure 4. The switches S_6, S_7, and S_8 experience the lowest standing voltages, while switches S_1, S_2, S_{11}, and S_{12} experience the highest standing voltage.

$$TSV\ p.u\ = \text{TSV} / \text{peak}\ output\ \text{voltage} = \ 43/6\ = \ 7.16$$

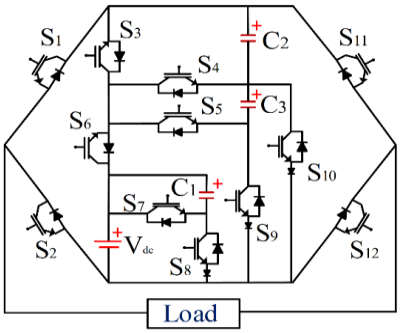

Figure 1. An improved 13-level SC-MLI topology

Table 1. Modes and switching states in one complete cycle

Modes	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	C_1	C_2	C_3	Vout
1	0	1	1	0	0	1	0	1	0	0	1	0	C	N	N	+Vdc
2	0	1	1	0	0	1	1	0	0	1	1	0	D	N	C	+2Vdc
3	0	1	0	1	0	1	0	1	1	0	1	0	C	N	D	+3Vdc
4	0	1	0	1	0	1	1	0	1	0	1	0	D	C	D	+4Vdc
5	0	1	0	0	1	1	0	1	0	0	1	0	C	D	D	+5Vdc
6	0	1	0	0	1	1	1	0	0	0	1	0	D	D	D	+6Vdc
7	0	1	0	0	0	0	0	0	0	0	0	1	N	N	N	+0Vdc
8	1	0	0	0	0	0	0	0	0	0	1	0	N	N	N	-0Vdc
9	1	0	1	0	0	1	0	1	0	0	0	1	C	N	N	-Vdc
10	1	0	1	0	0	1	1	0	0	1	0	1	D	N	C	-2Vdc
11	1	0	0	1	0	1	0	1	1	0	0	1	C	N	D	-3Vdc
12	1	0	0	1	0	1	1	0	1	0	0	1	D	C	D	-4Vdc
13	1	0	0	0	1	1	0	1	0	0	0	1	C	D	D	-5Vdc
14	1	0	0	0	1	1	1	0	0	0	0	1	D	D	D	-6Vdc

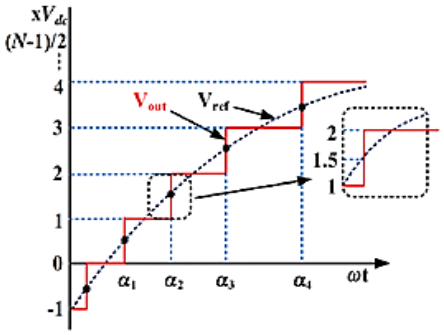

Figure 2. NLC technique

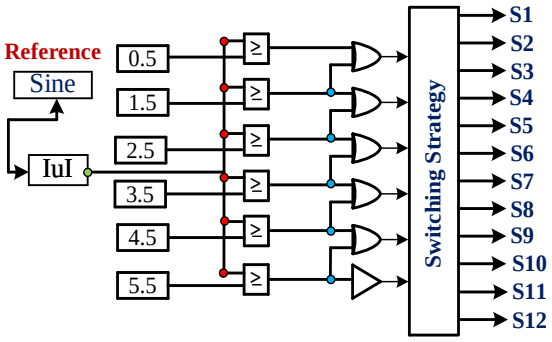

Figure 3. Switching logic of the NLC technique in the positive half cycle

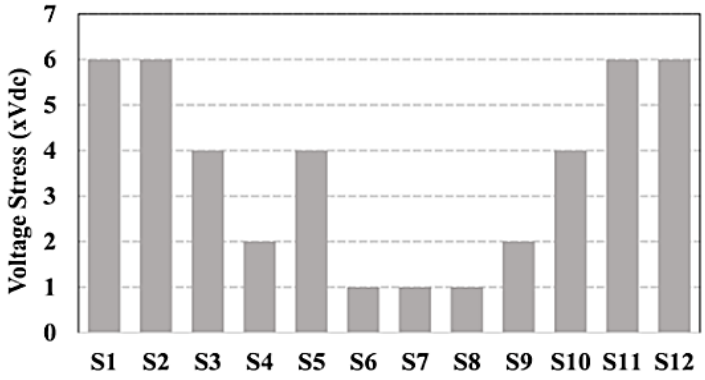

Figure 4. Maximum standing voltage across switches

2.4. Capacitor sizing and voltage balancing

The capacitor sizes of the power converter should be within allowed limits to perform efficiently. Large-size capacitors are more expensive, producing less ripple in output voltage. While smaller-size capacitors are less expensive, they produce more ripples in the output voltage, lowering the converter's performance. For the converter to function effectively, the capacitor voltage must be self-balanced, meaning that the energy dissipated and the energy assimilated must be equal while the capacitor is discharged or charged. The capacitors' maximum discharge value can be determined using (1) and (2) [19].

$$\Delta Q1 = \frac{1}{2\pi fo}\int_{\theta 2}^{\pi} Io\ dwt \quad (1)$$

$$\Delta Q2 = \Delta Q3 = \frac{1}{2\pi fo}\int_{\theta 3}^{\pi} Io\ dwt \quad (2)$$

The (3) and (4) can be used to determine the optimal capacitance of switched capacitors by considering a maximum allowable voltage ripple of V of the capacitors.

$$C1 = \frac{\Delta Q1}{\Delta V} = \Delta V.\frac{1}{2\pi f}\int_{\theta 2}^{\pi} Io\ dwt \quad (3)$$

$$C2 = C3 = \frac{\Delta Q2}{\Delta V} = \Delta V.\frac{1}{2\pi f}\int_{\theta 3}^{\pi} Io\ dwt \quad (4)$$

3. RESULTS AND DISCUSSION

The performance of the proposed SC-MLI topology was tested for static load and dynamic load conditions using MATLAB/Simulink. The changes in power factor and modulation index are also verified to check the reliability of the circuit. The nearest level control technique was applied to evaluate the circuit's viability. Table 2 shows the performance parameters that were chosen. In static loading, the circuit is tested for fixed R and RL load conditions, and various performance parameters, such as output voltage and output current, along with the THD analysis, are examined. Meanwhile, the circuit's performance is evaluated in dynamic load by varying the R and RL load. Additionally, variable modulation index (M.I.) and varying power factors are calibrated to test the circuit's fluctuation and reliability.

Table 2. Parameters for simulation analysis

Parameters	Specifications
Switches	IGBT
DC voltage sources (V_{dc})	50 V
Power frequency	50 Hz
Capacitor C_1,	50 V, 2250 µF
Capacitors C_2 and C_3	100 V, 4700 µF
Resistive load (R)	50 Ω, 100 Ω
Inductive load (RL)	50 Ω + 50 mH, 100 Ω + 90 mH

The fixed R load of 50 Ω and RL load of 50 Ω + 50 mH are used for static load analysis. The voltage source V_{dc} is set to 50 V, and voltage waveforms, current waveforms, and Capacitors voltage, along with FFT analysis, are traced as shown in Figure 5. The proposed inverter generates 13 levels at output voltage with a peak of 300 V and output current with a peak of 6 A under fixed R load as shown in Figure 5(a). For a fixed RL load the output voltage remains the same but the output current is sinusoidal with a peak of 6 A as shown in Figure 5(b). The proposed inverter exhibits a 6.51 % THD with a resistive load and 1.21 % THD with an inductive load in the output current, as shown in Figure 5(c). From the simulation results, it can be said that the proposed topology operated efficiently under fixed loading conditions. It was also observed that the voltage remained constant and was not affected by the change of load type, and the unity power factor was achieved with the resistive load. The capacitor's voltages are self-balanced; therefore, no need for auxiliary circuitry is required, which brings down the complexity of the circuit as shown in Figure 5(d).

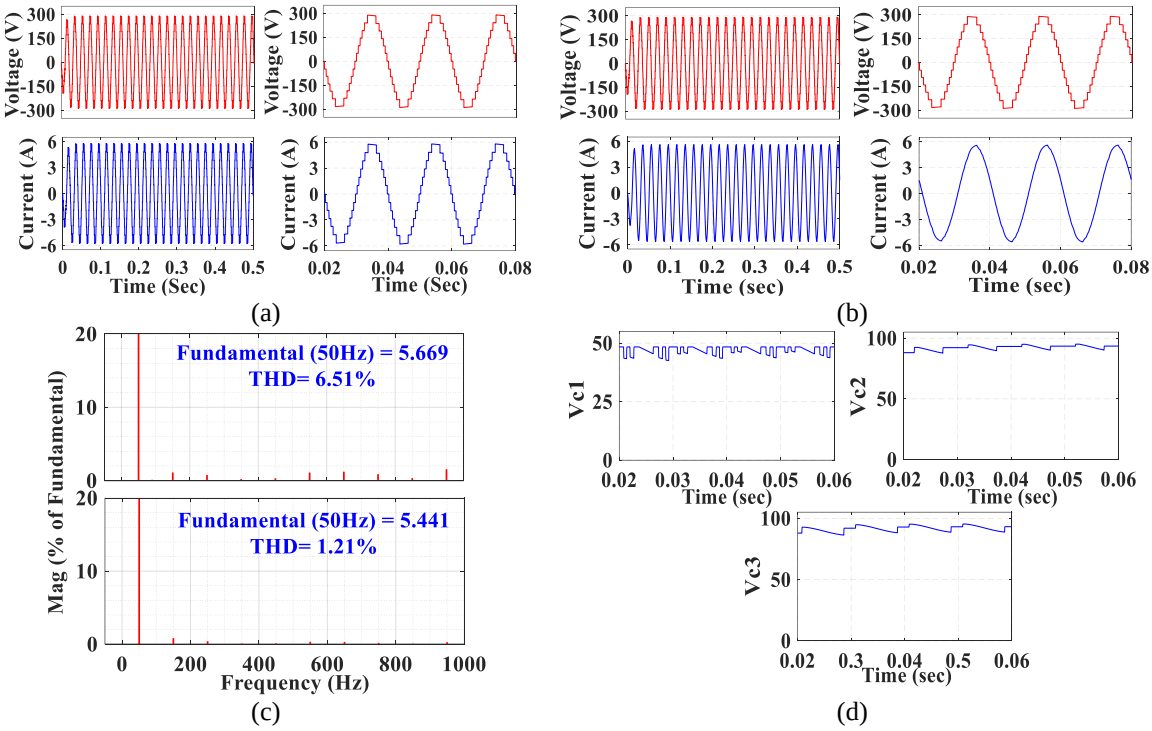

Figure 5. Obtained results with fixed loading conditions: (a) voltage and current waveforms for R load (50 Ω), (b) voltage and current waveforms for RL load (50 Ω + 50 mH), (c) FFT analysis, and (d) voltage across the capacitors

In real applications, the inverter is required to feed dynamic loads such as variations in the R-type and RL-type of loads. The dynamic R-type and RL-type loads represent the heating furnace and motor drives. The change in power factor and variation in modulation index were also performed to verify the feasibility under a sudden change in load and variation of control strategy, respectively. In varying R-type of load, the circuit's performance is tested by varying the resistive load from no load to 100 Ω then to 50 Ω. It can be noticed that the output voltage remains the same with a peak of 300 V, but the output current waveform increases from 0A to 6 A and then to 12 A as the load changes, as depicted in Figure6(a). The same procedure was followed for changing the RL load from no load to 100 Ω + 90 mH and then to 50 Ω + 45 mH in varying RL load. The output voltage remained the same but the output current increased from 0 A to 6 A and then to 12 A without any disturbance or spikes as the load decreased, as shown in Figure 6(b). The voltage and current waveforms under varying p.f are shown in Figure 6(c). Changing the modulation index plays an important role in assessing the dynamic stability of the circuit. The output voltage is reduced by lowering the modulation index (M.I). The output voltage dropped to 11 levels from 13 levels once the M.I. shifted from 1.0 to 0.8. As the M.I. reduced to 0.6, the output voltage dropped to 9 levels. Figure 6(d) shows the changes in output voltage as a function of the modulation index.

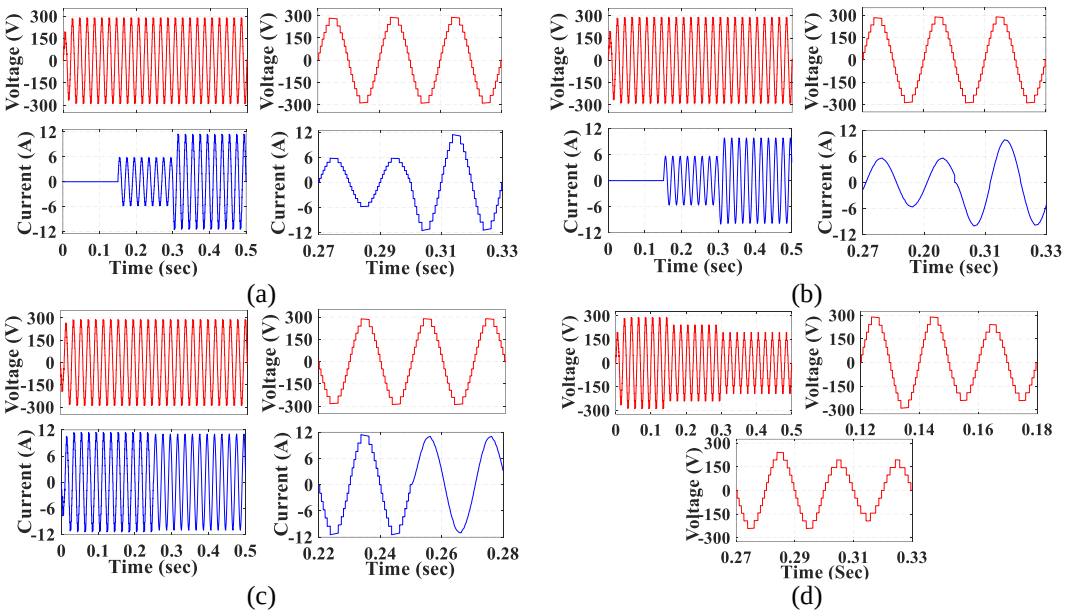

Figure 6. Obtained results with dynamic loading conditions: (a) voltage and current waveforms under varying R load, (b) voltage and current waveforms under varying RL load, (c) voltage and current waveforms under varying p.f, and (d) voltage and current waveforms under varying M.I.

4. THERMAL ANALYSIS

The thermal analysis of the SC-MLI topology was performed using PLECS to calculate total losses across the switches. Since the power loss analysis has a significant role in determining the performance and efficiency of the power converter. Two main types of power losses are conduction losses and switching losses associated with the semiconductor switches. The conduction losses occur due to the conduction of current. Therefore, conduction losses are associated with the internal resistance of the semiconductor device. On the other hand, switching losses are determined based on the energy losses during turning on and off the switch. Since the voltage and current within the switches are non-zero when the switches are turned on and off. Hence, the switching losses occur due to energy dissipation during the transition of the switch from the on to the off position.

The study investigates the conduction and switching losses of the proposed converter at different load conditions, as illustrated in Figure 7. Switching losses occur when voltage and current take a longer time to drop to zero during turns on and off, and higher switching frequency leads to increased losses. The proposed converter's low switching losses are attributed to its use of the low-frequency NLC PWM technique [20], [21]. Figure 8 depicts the relationship between efficiency and total power losses, where higher power results in increased conduction current and conduction losses, leading to a decline in the converter's efficiency. The total losses can be determined as the sum of the total conduction (P_c) and switching losses (P_{sw}) of the switch, as shown in (5).

$$Ptotal = Pc + Psw \quad (5)$$

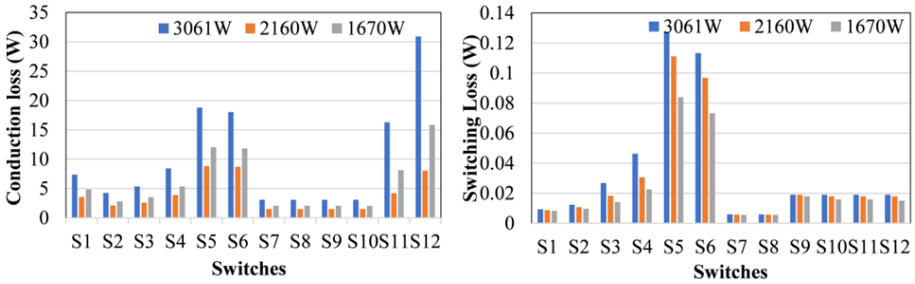

Figure 7. Conduction losses and switching losses in the proposed inverter topology

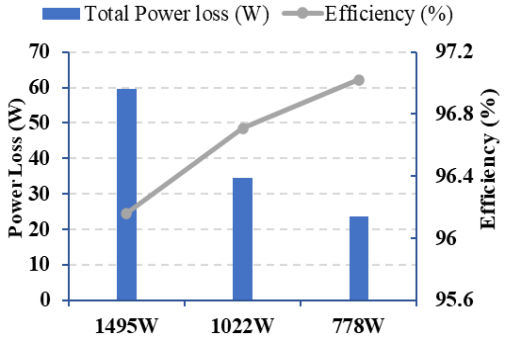

Figure 8. Variation in power losses and inverter efficiency with output power

5. COMPARATIVE ANALYSIS

The comparative analysis of the proposed topology with various recently existing 13 levels of MLIs is discussed in Table 3. This analysis was figured out based on the number of switches (N_{sw}), the number of DC voltage sources (N_{dc}), voltage gain (G), and total standing voltage (TSV) across the switches. Moreover, to validate the viability and improved performance of the proposed topology, the derived parameters cost analysis, N_L/N_{sw}, and $C.F/N_L$ were considered for a fair comparison. The graphical comparison is presented in Figure 9 From the analysis, it is observed that the proposed topology has fewer switches and a smaller number of components. Furthermore, this improved topology outraced similar topologies regarding (N_L/N_{sw}) and boosting factors, except those with more DC sources and component counts. Although the proposed topology has a higher TSV it requires the lowest cost factor. As depicted from Table 3, the proposed topology achieves a lower CF value than the other topology. The cost function (C.F) values calculated based on these three weighting coefficients (α=0.5, α=1, and α=1.5) show the feasibility of the topology's implementation, as shown in (6).

$$CF = N_{sw} + N_d + N_c + \alpha TSV \quad (6)$$

Table 3. Comparison of proposed SC-MLI topology with similar topology

Ref.	N_{sw}	N_{dc}	N_L/N_{sw}	N_d	N_c	N_T	G	TSV	C.F			$C.F/N_L$		
									α= 0.5	α= 1.0	α= 1.5	α= 0.5	α= 1.0	α= 1.5
[9]	20	2	0.65	0	6	26	1.5	5.30	28.65	31.30	33.95	2.20	2.40	2.61
[22]	14	2	0.928	2	4	20	3	6.00	25.00	28	31	1.92	2.15	2.38
[23]	16	2	0.813	2	4	22	3	5.60	26.80	29.6	32.40	2.06	2.28	2.49
[24]	18	3	0.722	3	3	24	2	5.00	28.5	31	33.50	2.19	2.38	2.60
[25]	16	2	0.813	4	4	24	3	5.33	28.76	31.33	34.00	2.21	2.41	2.61
[26]	12	1	1.083	4	4	20	3	4.33	23.16	25.33	27.50	1.78	1.94	2.11
Proposed	12	1	1.083	3	3	18	6	7.16	22.75	26.16	29.74	1.75	2.01	2.28

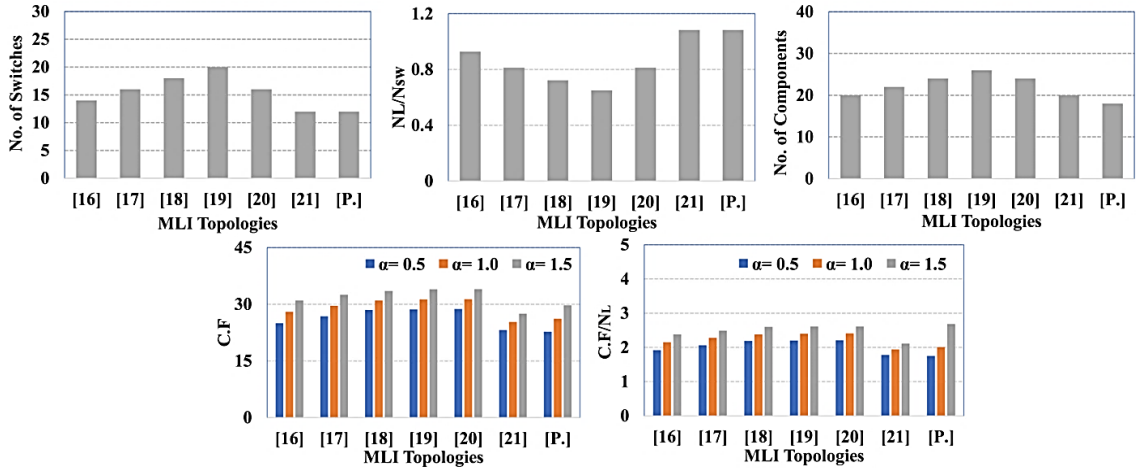

Figure 9. Graphical comparison of the proposed SC-MLI with similar topologies

6. SOLAR PV APPLICATION

Due to increasing energy demands in domestic and industrial applications, global attention for energy generation has shifted towards renewable energy sources from fossil fuels. Since fossil fuels have limited availability and have adverse effects on the environment in terms of emissions of greenhouse gases (GHGs) and temperature rise. Among different renewable sources, solar energy has significant contributions due to its environmentally friendly nature, ease of accessibility, low maintenance, and current advancements in PV technology. Power electronic converters are primarily combined with (RESs) for output regulation due to their higher efficiency power conversion ability. A solar PV system with a DC-DC converter is linked with this circuit topology to assess the feasibility of the proposed SC-MLI. The DC-DC boost converter was used to regulate the output of solar PV and deliver the desired source voltage to SC-MLI [27], [28].

This system consists of a solar PV array, conventional DC-DC boost converter, PSO-MPPT controller, and proposed SC-MLI topology as shown in Figure 10. The DC-DC converter was interfaced between the PV array and the DC link to regulate the solar PV output to 50V from 29V. The particle swarm optimization (PSO) based MPPT controller provided the appropriate switching signal to the dc-dc boost converter for obtaining the maximum power [29], [30]. The MATLAB model of the proposed topology for solar PV application is shown in Figure 11 The results showed that voltage across the capacitors is self-balanced; therefore, no auxiliary circuitry is required, as shown in Figure 12. The output voltage and current waveform of the proposed SC-MLI topology are shown in Figure 13. Hence, it is verified that the proposed topology was performed efficiently with solar PV application, which confirms its feasibility. The application of the proposed improved circuit for solar PV grid integration is presented in Figure 14. The proposed SC-MLI provides a 13-level output voltage, resulting in a smoother sine wave, minimizes the need for large filters, making the system more compact.

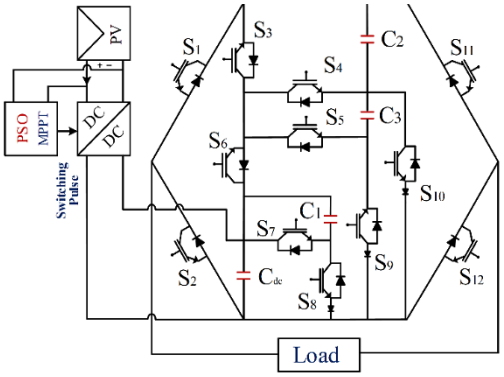

Figure 10. Application of proposed circuit for solar PV

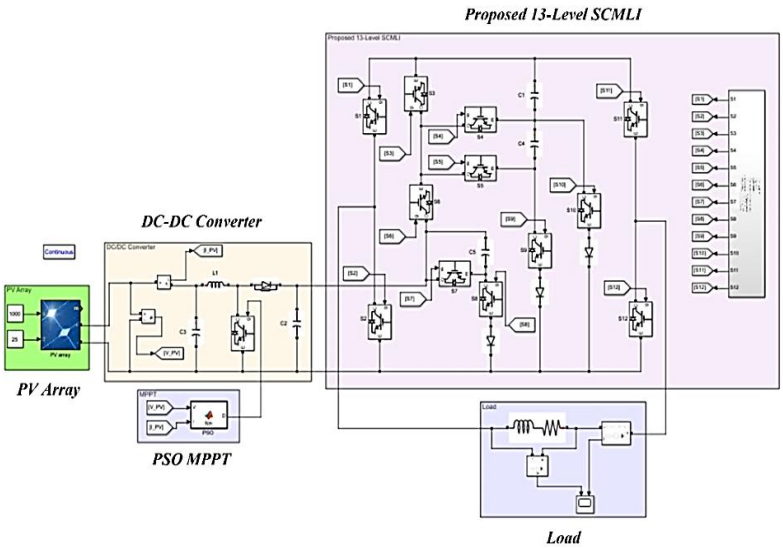

Figure 11. MATLAB/Simulink model of the proposed topology for solar PV application

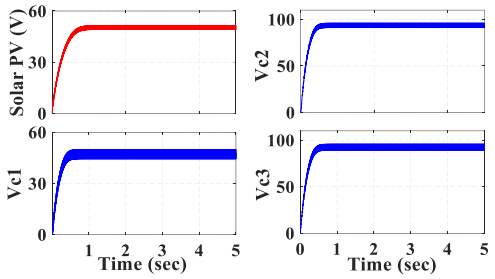

Figure 12. Output responses of solar PV system and inverter capacitor voltages

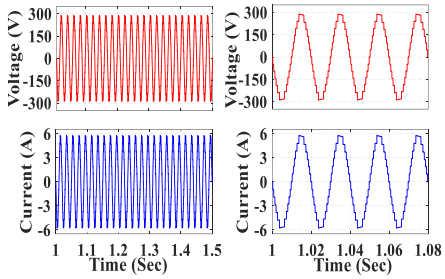

Figure 13. Steady state voltage and current waveforms of SC-MLI integrated with PV system

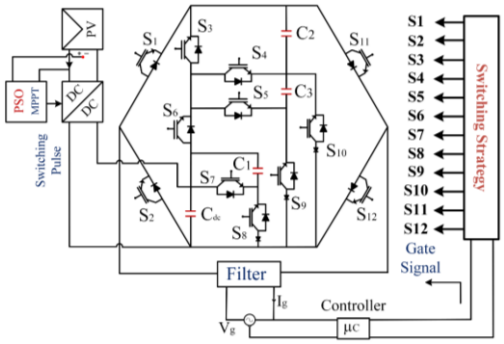

Figure 14. Application of proposed circuit for grid integration

7. CONCLUSION

This work presents an improved SC-MLI topology that generates 13-level output voltage with sextuple boosting gain. It consists of a single DC source, 12 unidirectional switches, 3 capacitors, and 3 diodes. The proposed topology generates high voltage gain with less component count and does not require an additional circuit or sensors for capacitor voltage balance which reduces the cost of the inverter. The nearest level control technique is used for the switching operation of the proposed circuit. The performance of the circuit was verified using MATLAB/Simulink under different loading conditions. The proposed SC-MLI achieved a THD of 6.51%, making it suitable for renewable energy grid integration due to its higher boosting feature and reduced THD. Thermal analysis is done using PLECS software to determine power losses. The results show that the proposed topology worked properly under different conditions and has an efficiency of above 96%. The feasibility of the proposed circuit was also verified for solar PV application using a PSO-MPPT controller.

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