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Enhancing power quality through DVR systems with advanced PLL-based ANFIS-optimized PI controller

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ABSTRACT

This paper presents a novel approach that integrates an advanced PLL with an ANFIS-optimized PI DVR controller, effectively mitigating voltage sags, swells, and harmonics in accordance with the IEEE 519 (2014b) guidelines for power quality in specialized application systems. The designed hybrid DVR controllers are tested using the hardware-in-the-loop OPAL-RT 4200 real-time simulator powered by an FPGA Kintex unit using the RT-LAB platform. The testing encompasses various loading conditions, including both nominal (100%) and increased (110%) loads. Under nominal loading conditions, the PLL-ANFIS optimized PI DVR controller is able to maintain power quality within acceptable limits. However, when the loading is increased to 110%, controllers based on the PLL-ANFIS optimized PI DVR method fail to meet the required standards. In contrast, the CDSC PLL-ANFIS optimized PI and MDSC PLL-ANFIS-optimized PI controllers perform better, successfully meeting the required limits. However, this achievement comes with a higher computational load and increased costs compared to alternative methods. Given the higher accuracy required to meet the IEEE 519 (2014a) guidelines for specialized applications, these trade-offs are considered acceptable, especially for critical and sensitive applications like healthcare facilities, semiconductor manufacturing plants, and pharmaceutical industries, where maintaining high power quality is crucial.

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1. INTRODUCTION

Power quality is a fundamental concern in modern electrical systems, where voltage sags, swells, and harmonics can severely impact industrial processes and sensitive equipment [1], [2]. Dynamic voltage restorers (DVRs) have emerged as an effective solution to mitigate these power quality disturbances. A DVR is a custom power device that injects compensating voltages into the system to maintain the desired load voltage during disturbances [3]. By dynamically adjusting the voltage waveform, DVRs can protect critical loads from the adverse effects of power quality issues, ensuring the smooth operation of sensitive electronic equipment.

The performance of a DVR largely depends on its control strategy. Traditional DVR controllers, such as proportional-integral (PI) controllers, are favored for their simplicity and ease of implementation [4]. However, these controllers often face challenges in adapting to varying system conditions and tuning their parameters for optimal performance. Advanced control strategies have been explored to overcome these limitations, including the use of artificial intelligence techniques like adaptive neuro-fuzzy inference systems (ANFIS). ANFIS combines the learning capabilities of neural networks with the reasoning capabilities of fuzzy logic to create a robust adaptive control system [5]-[8]. When optimized by ANFIS, PI controllers can

dynamically adjust their parameters in response to system changes, enhancing the DVR's ability to maintain power quality.

An essential component of an effective DVR control system is the phase-locked loop (PLL), which ensures precise synchronization with the grid voltage. Advanced PLL techniques, such as the cascaded delayed signal cancellation (CDSC) and multiple delayed signal cancellation (MDSC), have been developed to enhance the performance of PLLs under distorted conditions [9]-[11]. The CDSC and MDSC techniques improve the PLL's ability to track the phase and frequency of the grid voltage accurately, even in the presence of harmonics and noise. By integrating these advanced PLL methods with an ANFIS optimized PI controller, the overall performance and robustness of the DVR can be significantly enhanced. This paper presents a novel approach to power quality enhancement by combining an advanced PLL with an ANFIS optimized PI controller for DVR applications, demonstrating its effectiveness through detailed simulations and analysis.

2. EXISTING LITERATURE

Various topologies of DVRs have been used in literature to improve voltage stability, compensate for reactive power, function as series active filters to mitigate harmonics, and compensate for load voltage changes caused by voltage drifts, as suggested [12], [13] suggested the use of DVRs that are particularly designed to compensate for power sags of various kinds. In addition, [14] suggested a DVR that incorporates a transformer grid to minimize fault currents. The [15], [16] introduced a self-supported DVR that mitigates both symmetrical and asymmetrical grid failures. Hasan *et al.* [17] proposed using a DVR equipped with an intelligent hybrid control technique to enhance the fault ride-through (FRT) capacity of wind turbines. In their study, [18] introduced a multilevel converter using a three-level neutral point clamped (3L-NPC) architecture. The purpose of this design is to mitigate harmonics and manage unbalanced capacitor voltage in order to compensate for power quality issues. The effectiveness of a system with a stable output and rapid reaction time is greatly influenced by the choice of controller. The [19], [20] examined the constraints associated with existing current source inverters and voltage source inverters. Traditional PI and PID controllers for DVRs are calibrated using linearized models to achieve optimum performance. However, as highlighted by [21], their performance deteriorates when there are dynamic changes in operating circumstances. The [22], [23] have shown that PID controllers are unsuitable for rapid converter switching with nonlinear control operations because of their persistent non-linearity and demanding specifications. On the other hand, adaptive nonlinear controllers provide sufficient performance in the face of dynamic changes, but their implementation is more intricate and challenging compared to linear controllers. In order to tackle optimization problems in the presence of nonlinearity, scientists have devised innovative artificial intelligence (AI) methods such as artificial neural networks (ANN), fuzzy logic, genetic algorithms, expert systems, and ANFIS. The [24], [25] examined ANFIS as a cutting-edge method using optimized fuzzy rules to achieve rapid reaction control of power conditioning devices. Several non-linear intelligent control systems have been suggested in the literature. Shukla *et al.* [26] introduced a fuzzy logic controller that uses carrier-modulated pulse width modulation (PWM). In their study, they examined the limitations of traditional PI controllers and proposed the use of a dynamic PI controller that incorporates fuzzy logic. In their study, [27] introduced a three-phase PWM rectifier that relies on direct power control and utilizes neural networks.

3. IEEE GUIDELINES

3.1. IEEE 3002.8 guidelines for conducting harmonic studies

The IEEE 3002.8 guidelines and recommended practices provide a framework for harmonics analysis in commercial and industrial systems. These guidelines facilitate the collection of necessary data, recognition of potential issues, and the benefits of using computer tools for analysis. The main objective of the analysis is to assess the impacts of local and neighboring loads before attributing equipment failures to power quality issues. This helps in identifying the actual cause of failures. Power quality (PQ) investigations include activities such as calibrating a benchmark model with well-defined plans, identifying the magnitude, type, and location of harmonic sources, studying the penetration of harmonics into neighboring loads, and calculating harmonic indices to compare with relevant code limitations. For example, PQ assessments in hospital facilities involve on-site inspections of electrical systems and PQ monitoring at all bus bars, particularly those feeding the most critical and sensitive loads.

3.2. IEEE 519 limits for PQ in special applications

Previously, the IEEE 519 (2014a) established PQ compliance limits primarily for general systems. These have been updated to include different compliance requirements for special applications, general systems, and dedicated systems, as shown in Table 1. According to the IEEE 519 (2014a) guidelines, for a

system with sensitive and critical loads, the notch depth should be less than 10%, and the notch area should be less than 13.66 V/s. In past studies, compensation for voltage notches received less attention. Additionally, the voltage total harmonic distortion (THD) compliance for special applications has been updated to less than 3%, compared to the earlier limit of less than 5% for general systems.

Table 1. IEEE519 recommended limits on voltage notches and harmonics.

Parameters	Special applications[x]	General systems	Dedicated systems[y]
Notch depth (%)	10	20	50
Notch area (A_N)(V/s)	16.4	22.8	36.5
VTHD (%)	3	5	10

Special applications[x] - example critical and sensitive loads in airports.
Dedicated systems[y] - specific user supply or micro grid condition.

4. DYNAMIC VOLTAGE RESTORER

Figure 1 illustrates a schematic diagram of a series-connected DVR in a distribution system, with a detailed description available in [28]. The utilization of DVRs for mitigating voltage disturbances and their financial evaluation is discussed in [29]. The effectiveness of DVR compensation is influenced by its flexibility, the accuracy of switching using PWM, and the type of controller employed, which can include PI, fuzzy logic controller (FLC), artificial neural network (ANN), and ANFIS controllers.

Figure 2 presents the phasor diagram during a voltage sag condition, illustrating a single-phase scenario for simplicity. In this condition, the phasor representation includes the injected DVR voltage (VDVR), the source side voltage (V1), and the load side voltage (V2). The DVR injects voltage (VDVR) in such a manner that V2 remains constant at its pre-sag value, regardless of any disturbances or distortions in the supply voltage V1. The angles α, δ, and ϕ represent the advanced phase angle of the voltage, the phase angle of the source voltage, and the power factor angle of the load, respectively, with I denoting the load current. Besides in-phase voltage injection, an advanced phase angle voltage injection method, as proposed by [5], is also utilized. It has been demonstrated that by selecting an appropriate phase angle α, the energy supplied by the DVR for voltage restoration can be minimized. Theoretical analysis and derivation for generalized sag situations requiring voltage injection compensation have been conducted. The expressions for the optimal phase angle, αopt, are summarized as (1)-(4). The condition that must be satisfied involves the supply voltage, injected voltage, and pre-sag voltage.

$$|V_{ivlj}| = |V_{prev-sag}| - |V_{sag}| \quad (1)$$

$$\varphi_{inlj} = \tan^{-1}\left(\frac{V_{prev-sag}\sin(\varphi_{prev-sag})}{V_{presag}\cos(\varphi_{presag}) - V_{sag}\cos(\varphi_{sag})}\right) \quad (2)$$

$$\left[\left(\sum_{\forall j} V_{1j}\cos(\delta_j)\right)^2 + \left(\sum_{\forall j} V_{1j}\sin(\delta_j)\right)^2\right]^{1/2} \geq 3V_2\cos(\varphi) \quad (3)$$

$$\left\{\alpha_{Optm} = \varphi + B - Arc\cos\left(\frac{\left(\left(\sum_{\forall j} V_{1j}\cos(\delta_j)\right)\right)^2 + \left(\sum_{\forall j} V_{1j}\sin(\delta_j)\right)^2}{3V_2\cos(\varphi)}\right)\right\} \text{ else } \alpha_{opt} = \varphi + \beta \quad (4)$$

This optimal phase angle ensures that the DVR operates efficiently by minimizing the energy required to restore the voltage to its pre-sag condition.

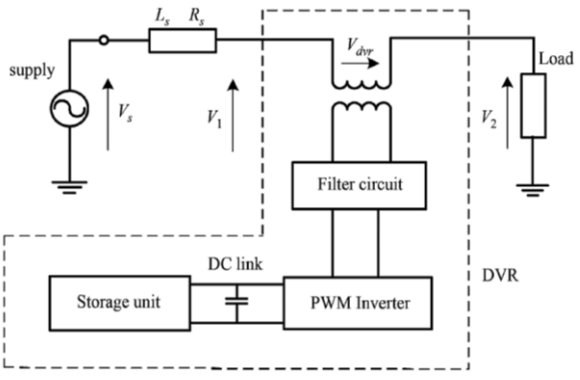

Figure 1. Schematic diagram of DVR

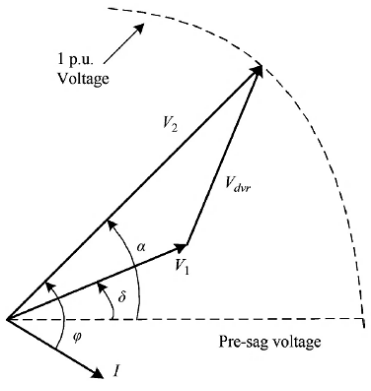

Figure 2. Phasor diagram of voltage sag condition

5. ESTIMATION OF VOLTAGE PARAMETER, NOTCH, AND INDEX FLUCTUATIONS

From (4), it is evident that the calculation of the optimal phase angle, αopt, requires parameters such as the phase change δj and the disturbance voltage magnitude V1j. Due to the difficulty of quickly estimating these variations upon the occurrence of a disturbance, the operation of the DVR with energy optimization is delayed. Therefore, it is proposed that the DVR should operate in in-phase compensation mode during a voltage disturbance until the supply parameters can be provided by the estimator for the phase-advanced compensation method. The fast fourier transformation (FFT) is utilized to estimate the supply voltage parameters. This technique allows for the tracking of supply voltage parameters and the estimation of optimal parameters regardless of the nature of the input signal. Consider a sinusoidal supply voltage with an angular frequency ω.

$$V_t = V_m \,.\sin(\omega t + \delta) \tag{5}$$

$$V_t = V_m \,.\cos\delta \,.\sin(\omega t) + V_m \sin\delta \,.\cos(\omega t) \tag{6}$$

The matrix form is written as (7).

$$x_k = j_{k-1} \,.\, x_{k-1} + w_{k-1} \tag{7}$$

Estimating voltage notches. The depth and size of the notch are computed using (8)-(11). The depth of noise, as in (8).

$$V_N = \frac{L_{Le}}{L_L + L_t + L_s} \tag{8}$$

The depth of notch, as in (9)-(11).

$$t_N = \frac{2(L_L + L_t + L_s)}{e} \tag{9}$$

$$e = \sqrt{2} \; {}^{*}E_L \tag{10}$$

$$A_N = V_N t_N \tag{11}$$

Here V_N is the depth of notch of group, t_N is the width of notch, A_N is the area of notch, L_L is the inductance of load, L_t is inductance of converter, L_s is the source inductance, and E_L is phase voltage.

6. DETERMINATION OF VOLTAGE SAG PARAMETERS FOLLOWING IEEE GUIDELINES

According to the IEEE 1564 guidelines, voltage sag indices are calculated for accurate assessment of system voltage quality and performance. These indices measure the DVR's compensation capability.

6.1. Voltage sag lost energy index (VSLEI)

The energy that is given to the load decreases as a result of voltage sag. This index, which is generated by (12), is a representation of the energy that is wasted when a sag condition is present.

$$W = T \left[1 - \frac{V}{V_{noml}}\right]^{a} \tag{12}$$

Here, T represents the duration of the voltage sag in seconds, V is the measured phase-to-phase voltage in per unit (pu), V_{noml} is the nominal voltage in per unit (pu), and α is set to 3.14 according to the Computer Business Equipment Manufacturers Association (CBEMA) curve.

6.2. Detroit edison sag score (SS)

It defines the system voltage quality after sag compensation. An SS value close to 0 indicates the effectiveness of the voltage sag compensation and the overall quality of the system, as described by (6).

$$SS = 1 = \frac{V_A + V_B + V_C}{3} \tag{13}$$

In this context, V_A, V_B, and V_C represent the RMS values of the phase voltages in per unit (pu).

7. PROPOSED HYBRID ADVANCED PLL BASED - ANFIS OPTIMISED PI DVR CONTROLLER

7.1. Advanced PLL methods CDSC and MDSC

7.1.1. CDSC-based PLL

The general structure of frequency adaptive CDSC PLL is shown in Figure 3. In the case of grid voltage distortion, a grid-synchronization PLL monitors the positive-sequence fundamental voltage component. The grid-synchronized dq-frame displays the existence of this component as a direct current (DC) signal. When harmonics are present, the previously existent ABC- and αβ-frame harmonics become dq-frame harmonics. This change happens with harmonics. The half-wave symmetry of sinusoidal harmonics moves them one order in the dq-frame from the original waveform.

For each randomized dq-frame voltage signal v(t), the proposed DSC operator may be stated generally as (14).

$$DSC_n = \frac{1}{2}\left[v_h(t) + v_h(t - \frac{T}{n})\right] \quad (14)$$

Where, n-delay factor and T-grid fundamental period. By manipulating the delay times (T/n), an out-of-phase signal may be generated. The minimal delay required by the DSC operator is the time period beginning at t = 0 and ending when the signal crosses zero in a negative direction. An example of a possible delay period for eliminating a 4th-order harmonic frequency signal is T/8, which may be further expressed as (T/8 + T/4), (T/8 + 2T/4), or (T/8 + 3T/4). In most cases, the potential delay periods T/n for removing the h^{th} harmonic signal are (15).

$$\frac{T}{n} = \frac{T}{2h} + k\frac{T}{h}, \forall\, k < h - 0.5 \;\&\; k \epsilon N_0 \quad (15)$$

DSC2, DSC4, DSC8, DSC16, and DSC32 remove harmonics of the forms 2k+1, 4k+2, 8k+4, 16k+8, and 32k+16. These operators eliminate harmonics. Multiple operators are often used to eliminate multiple harmonics. This is because each operator seeks a separate harmonic order. Harmonics of 2k, 4k, 8k, 16k, and 32k pass through these DSC operators without attenuation. Cascaded operators delete all lower-order harmonics, ensuring complete harmonic elimination. According to sources [14]-[16], this cascading creates the cascaded delayed signal cancellation (CDSC 2, 4, 8, 16, 32) operator. This operator was created to serve dq reference frame applications. When utilized in the ABC frame, it removes the fundamental frequency component, which is needed for SRF-PLL grid synchronization.

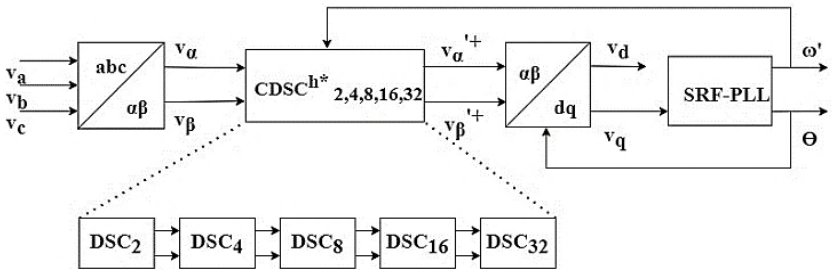

Figure 3. The general structure of frequency adaptive CDSC PLL

7.1.2. MDSC-based PLL

MDSC is a modified form of the DSC operator that addresses digital control system total delay time and storage issues. The general structure of the frequency adaptive MDSC PLL is shown in Figure 4. This invention improves performance and simplifies computing. MDSC, an improvement on CDSC, delays a test signal many times until the total of the signal and its delays approaches zero. This iterative method eliminates noise and interference to improve signal clarity. MDSC uses CDSC's phase manipulation and delay adjustment in digital control systems to increase signal quality by iteratively refining delay settings until signal augmentation or cancellation is achieved. The MDSC technique purposefully selects delay durations as integer multiples of T/15, where T is the fundamental time period. Our design limits delay times to the basic period T. This variation is MDSC15. MDSC15's maximum delay time is 14T/15, much less than CDSC versions.

$$\begin{bmatrix} MDSC_{15}[v_{\alpha h}] \\ MDSC_{15}[v_{\beta h}] \end{bmatrix} = \begin{bmatrix} cosh^*\theta & -sinh^*\theta \\ sinh^*\theta & cosh^*\theta \end{bmatrix} * \begin{bmatrix} MDSC_{15}[v_{dh}] \\ MDSC_{15}[v_{qh}] \end{bmatrix} \quad (16)$$

Where $MDSC_{15}[v_{dqh}] = \frac{1}{15}\sum_{l=0}^{14}[v_{dq}h(\omega t - Tl/15)]$.

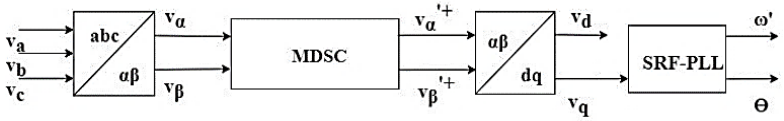

Figure 4. The general structure of the frequency adaptive MDSC PLL

7.2. PI controller

The PI controller is the most commonly used DVR controller. The DVR-PI controller receives an error signal by comparing the RMS value of the load terminal voltage with the reference voltage. However, under conditions of parameter variations, transient faults, and dynamically changing loads, achieving satisfactory performance is challenging due to its inability to quickly respond to sudden changes in error. The main issue is selecting the optimal gain for the PI controller, as it remains fixed under all conditions. Additionally, determining the appropriate controller gain requires a precise mathematical model. In this context, the conventional PI controller gain is tuned using the Ziegler-Nichols method. To overcome the drawbacks of conventional gain tuning for complex systems, advanced techniques such as rule-based FLC and ANN controllers are employed. Despite their benefits, both ANN and FLC have inherent disadvantages. To address these issues, the ANFIS configuration was developed, combining the strengths of both ANN and FLC. For DC-link control in DVR systems, typically, a PI controller is employed due to its simplicity and effectiveness in maintaining a stable DC bus voltage. In the context of this research work, where an ANFIS optimized PI controller is used, the DC-link control can benefit from this enhanced approach.

The control method for DC-link regulation generally involves the following steps:

- Voltage sensing: The actual DC-link voltage is continuously measured and compared to a predefined reference value. This reference is often based on the expected compensation voltage or the energy requirements of the DVR during disturbances.
- Error calculation: The difference (error) between the measured DC-link voltage and the reference voltage is fed into the PI controller.
- PI controller action: The PI controller adjusts the output to minimize the error over time. In this case, the ANFIS optimization can improve the PI controller's tuning by adapting to different conditions, making the controller more robust to system changes and external disturbances.
  Proportional action: Addresses the immediate error by adjusting the control output based on the current difference between the reference and the actual voltage.
  Integral action: Eliminates steady-state error by considering the cumulative error over time, ensuring that the DC-link voltage stabilizes around the reference.
- PWM control: The output of the PI controller is typically used to adjust the duty cycle of the DC-DC converter (such as a buck-boost converter), which directly controls the energy flow to or from the DC-link capacitor, thereby regulating the voltage.

This control method ensures that the DC-link voltage remains stable even during fluctuations in load or input voltage. The enhanced ANFIS-optimized PI controller improves this process by optimizing the controller parameters in real-time, leading to better dynamic performance and faster response during voltage sags or swells.

7.3. Adaptive neuro-fuzzy inference system

In fuzzy logic systems, the parameters of membership functions - such as their type, size, input, and output - are often selected through trial and error. Fuzzy inference systems do not have any established procedures for converting human knowledge into their rule base. Consequently, efficient techniques are required to refine membership functions and minimize the rule base. The creation of ANFIS, which integrates fuzzy logic's qualitative approach with neural networks' adaptive learning capabilities, allowed us to overcome these obstacles. This makes it possible to train the system without requiring a great deal of specialized expertise. The inverter operating conditions of the DVR are highly variable, making the selection of optimal gain values for conventional PI regulators difficult, potentially leading to incorrect operation if the wrong gain values are chosen. To address this issue, an ANFIS-optimized PI controller was developed, which is highly effective in controlling complex, non-linear systems.

7.4. ANFIS optimized PI controller

The ANFIS-optimized PI controller for DVR control features a 1:3:3:3:3:1 architecture, generated using MATLAB/ANFIS editor based on initial data from the PI controller, as illustrated in Figure 5. This ANFIS architecture, employing a Sugeno fuzzy model, has one input and one output. It is further tuned online using the error propagation method. The error between the d-axis voltage reference and the actual d-axis voltage component is fed into the input of the ANFIS controller, which adjusts the consequent and premise parameters for the d-axis component. Similarly, another ANFIS controller manages the q-axis component.

Fixed parameters are represented in circle nodes, while adaptive parameters, which change during training, are represented in square nodes. The functions of each layer node in the ANFIS-optimized PI structure are described as shown in Figure 5.

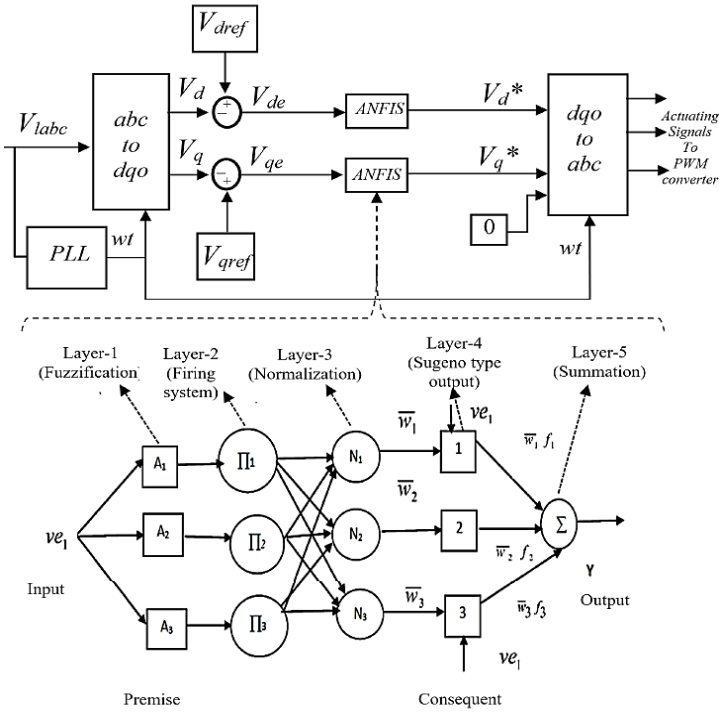

Figure 5. ANFIS optimized PI controller for DVR

7.4.1. Layer-1

In the fuzzification layer, each node is represented by a square. The parameters in this layer are known as precondition or premise parameters. Each node function is associated with linguistic labels A_i (such as A_1, A_2, and A_3). The input to node iii is ve1, and the corresponding node equations are given as follows:

- A_1: Represents a specific linguistic label for the node function.
- A_2: Represents another linguistic label for a different node function.
- A_3: Represents a third linguistic label for yet another node function.

These linguistic labels help define the fuzzy sets for the input variables, allowing the system to process and interpret the input ve1 according to the predefined fuzzy logic rules.

$$O_I = \mu A_I(Ve_1) \tag{17}$$

$$\mu A_I(Ve_1) = \begin{cases} 0 \; Ve_1 \le a_I \\ \frac{Ve_I - a_I}{b_I = a_I} \; a_I \le Ve_I \le b_I \\ \frac{c_I - Ve_I}{c_I = b_I} \; b_I \le Ve_I \le c_I \\ 0 \;\; c_I \le Ve_I \end{cases} \tag{18}$$

Here, i ranges from 1 to 3, representing the nodes in the layer. The output of the i^{th} node in layer 1 is denoted as O_I. The parameters a_I, b_I, and c_I are associated with the triangular membership function. The triangular membership function is used to map the input values to a degree of membership, which helps in the fuzzification process by transforming crisp inputs into fuzzy values that can be processed by the fuzzy inference system.

7.4.2. Layer-2

In this layer, each node is labeled as Φ. The incoming signals are multiplied within this layer and then transmitted to the subsequent layer. Here, i, J ϵ [1,2,3].

$$\overline{W_J} = \mu A_i(Ve_1) \quad (19)$$

7.4.3. Layer-3

In this layer, each node is labeled as N. The normalized strength of firing is calculated here, using a specific equation provided. Here Jϵ [1,2,3].

$$\overline{W_J} = \frac{W_J}{\sum_{k=1}^{3} W_k} \quad (20)$$

7.4.4. Layer-4

In this layer, the parameters are referred to as consequent parameters. Each node in this layer is represented by a square shape.

$$O_J = \overline{W_J} f_i = \overline{W_J}\ (p_J Ve_1 + t_J) \quad (21)$$

In this context, W_J represents the output from the third layer, while O_J denotes the output of the j-th node in the fourth layer. The variables p_J and t_J are sets of consequent parameters that are determined during the training process.

7.4.5. Layer-5

In this layer, the output (y) is calculated by summing all the incoming signals. This aggregation of inputs results in the final output value for the layer.

$$y = \sum_{j=1}^{3} \overline{W_J}\, f_i = \sum_{j=1}^{3} \left[(\overline{W_J}\, Ve_1)\, r_J + (\overline{W_J}) t_J\right] \quad (22)$$

In a similar manner, the node functions for each layer of the ANFIS structure are also derived for the q-component.

Figure 6 represents the flowchart of the optimized ANFIS-PI. To create the ANFIS controller, which is represented by a Sugeno fuzzy inference system (SFIS), the ANFIS editor GUI from the MATLAB/Simulink fuzzy logic toolbox is utilized. The ANFIS structure considered here incorporates a three-rule Sugeno model. A FLC scheme using the Mamdani type is proposed for a self-adaptive mechanism, optimizing the controller's functionality. Two FLCs are employed: one for controlling the direct axis component voltage error (d-axis) and another for the quadrature axis component voltage error (q-axis). Each controller uses two inputs: the voltage error (Vde or Vqe) and the rate of error change (ΔVde or ΔVqe). The FLC for the d-axis considers the error signal (Vde) as the difference between the actual and reference voltages of the d-axis, while the FLC for the q-axis considers the error signal (Vqe) similarly for the q-axis.

In decision-making, the link between input and output signals is established through a rule base, as shown in Table 2. The network phasor voltage of each phase is tracked by a PLL, generating a reference signal aligned to the supply frequency. The error, defined as the difference between the actual and reference voltages, serves as input to the FLCs. The FLC outputs control a pulse width modulation (PWM) generator to produce pulses for voltage source converter (VSC) switching. During voltage disturbances, the PLL quickly adjusts, ensuring the load voltage phase remains stable. The feedback control type is applied with a fast time response (approximately 1ms) to maximize performance and dynamic operation, providing quick compensation during voltage disturbances in the distribution system.

Here N-Negative, SP-Small Positive, P-Positive, MN1- Medium Negative 1, MN2- Medium Negative 2, MN3- Medium Negative 3, MP1- Medium Positive 1, MP2- Medium Positive 2, MP3- Medium Positive 3, LP1- Large Positive 1, LP2- Large Positive 2 & LP3- Large Positive 3. These are represented by triangular membership functions. Direct axis component voltage error (Vde) and rate of error change (ΔVde) are computed. Decision-making links input (voltage error and rate of error change) to output signals via a rule base, as shown in Table 2.

In the proposed method, the PLL tracks the network phasor voltage of each phase, generating a reference signal aligned to the supply frequency. The error, defined as the difference between actual load voltage and the PLL-generated reference signal, serves as input to the FLCs. The FLC outputs control a PWM generator to produce pulses for VSC switching. This setup ensures quick compensation during voltage disturbances, maintaining a stable load voltage. Data on the desired input/output is gathered from the simulation of the DVR PI controller and saved in the workspace in an array format. The saved workspace data is then used for training and validating the ANFIS. The first column vectors contain input data, while the last column vectors contain output data.

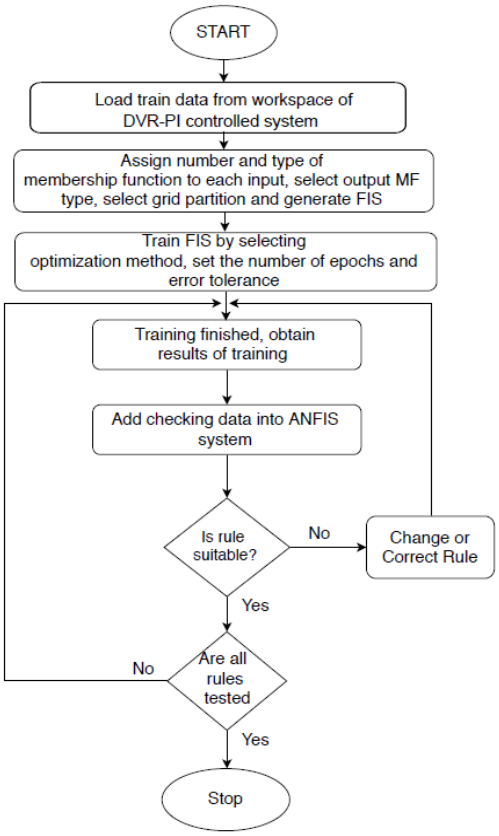

Figure 6. ANFIS optimizes the PI controller flowchart

Table 2. Rule-based representation

ΔVe/ Ve	N	SP	P
N	MN1	MP1	LP1
SP	MN2	MP2	LP2
P	MN3	MP3	LP3

8. PROPOSED DVR DESIGN

The design calculations provided outline the essential steps to determine the specifications of a DVR for a 3-phase 400 V, 50 Hz, 100 kVA critical load. The DVR is a device used to protect sensitive loads from power quality issues, such as voltage sags. The designed schematic diagram of the series-connected DVR system is shown in Figure 7.

First, the DVR's current rating is determined based on the load's power rating. For a 100 kVA load on a 400 V system, the DVR must handle a current of approximately 144.3 A. This current is essential as it indicates the DVR's capacity to manage the load's power needs during normal operation.

$$I_{DVR} = \frac{Load_{KVA}}{\sqrt{3}.V_s}$$

Next, the DVR's voltage rating is calculated by considering the maximum voltage sag the system must compensate for, which is 50% of the nominal voltage (0.5 per unit). After calculating the sag, the DVR must provide a compensating voltage of around 200 V to maintain stable operation during a sag event.

$$V_{sag} = V_s.(0.5) \qquad V_{DVR} = \sqrt{V_s^2 - V_{sag}^2} \qquad V_{DVR} = 199.9 \cong 200\ V$$

The kVA rating of the DVR, which represents the power it can deliver during a voltage compensation, is then computed to be 86.59 kVA. This rating is critical for sizing the injection transformer, which is the component that injects the compensating voltage into the system. The injection transformer is thus rated at 86.59 kVA, matching the DVR's kVA rating.

$$S_{DVR} = \frac{3.V_{DVR}.I_{DVR}}{1000} \quad (23)$$

$$S_{DVR} = 86.59\ kVA$$

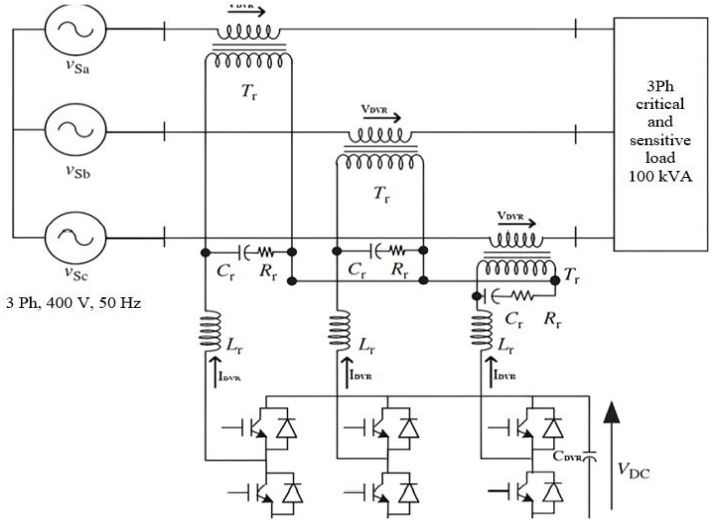

Figure 7. Designed a schematic diagram of a series-connected DVR system

The regulation of the DC bus is a critical aspect of DVR design, as it directly impacts the system's ability to respond effectively to voltage disturbances such as sags, swells, and harmonics. Here's a summary of the key points covered in our work on DC bus regulation:

- DC bus voltage control: Discuss the strategies employed to maintain a stable DC bus voltage, which is essential for DVR operation. This typically involves monitoring and regulating the DC link voltage to ensure it remains within specified limits, providing the necessary energy storage to inject or absorb power during disturbances.
- Energy storage system (ESS): Include details on the type of energy storage (e.g., batteries, supercapacitors) used in conjunction with the DC bus and how it interacts with the DVR to supply or absorb energy during transients. The efficiency of the DC bus voltage regulation directly impacts the DVR's ability to mitigate voltage sags and swells.
- Controller design for DC bus regulation: Elaborate on how the PLL-ANFIS optimized PI controller helps regulate the DC bus voltage, ensuring quick and precise voltage restoration. Highlight the feedback mechanisms and control algorithms designed to maintain a stable DC bus, especially during fluctuating grid conditions.
- Impact on power quality: Include analysis or simulation results showing how DC bus regulation affects the overall performance of the DVR in maintaining power quality. Poor DC bus regulation can lead to insufficient voltage correction or slower response times, so demonstrating effective regulation is vital.

To ensure the DVR can store enough energy to maintain voltage compensation, the DC capacitor voltage is calculated. The capacitor needs to maintain a voltage greater than 141.42 V, so a 150 V capacitor is chosen to provide a safety margin.

$$V_{DC} > 2\sqrt{2}.V_{V_{SC}} \quad (24)$$

$$V_{DC} > 2\sqrt{2}.(50) > 141.42\ V \quad (25)$$

The size of the capacitor bank, which is responsible for smoothing and filtering the DC voltage, is estimated to be around 1984 µF. A slightly larger capacitor, 2200 µF, is selected to ensure adequate energy storage and voltage regulation.

$$kVA/\ phase = 33.33\ kVA\ /\ phase, Charging\ Current = \frac{kVA\ /\ phase}{V_s} = 144.3\ A \quad (26)$$

$$C_{DVR} = \frac{Charging\ current}{X_c} = 1984\ \mu F \quad (27)$$

The interfacing inductor is sized to manage the current ripple, which is a small fluctuation in current due to switching operations. The calculated inductance is 6.05 mH, designed to limit the ripple current to 2%, ensuring smooth operation.

$$L_r = \frac{n.\left(\frac{\sqrt{3}}{2}\right)mV_{DC}}{6\alpha F_S \Delta I_S} = 6.05 \text{ mH} \quad (28)$$

Finally, a ripple filter, consisting of a series-connected capacitor and resistor, is designed to filter out high-frequency noise. The filter is tuned to half the switching frequency (15.5 kHz), with a capacitor value of 20.54 µF and a resistor of 1 ohm, ensuring that the DVR operates effectively without introducing unwanted electrical noise into the system. This implies the values to be substituted yielding the following values for C_r is $C_r = 20.54\ \mu F$.

$$F_r = {}^{1}/_{(2\pi R_r C_r)} \quad (29)$$

These calculations collectively ensure that the DVR is properly sized to protect the load from voltage sags, maintaining power quality and stability.

9. RESULTS

The study examines several scenarios involving the test system with and without DVR compensation. The designed DVR controllers are tested using hardware-in-the-loop (HIL) simulation powered by a field-programmable gate array (FPGA) Kintex unit and supported by the RT-LAB platform with the OPAL-RT 4200 real-time simulator. The developed model is structured into three distinct subsystems. The master subsystem (SM-Plant) houses the virtual plant model, simulating the operational environment. The slave subsystem (SS-Control) contains the DVR controller, which is designed for real-time control, ensuring optimal system performance. Lastly, the console subsystem (SC-Display) manages the operational-monitoring functions, facilitating real-time monitoring and user interaction with the system. The schematic of the simulator and experimental setup is shown in Figures 8 and 9, respectively. Initially, the test system is evaluated without any DVR compensation. Following this, the system is tested with DVR compensation to address voltage sag & swell issues and harmonics under both 100% and 110% loading conditions. Additionally, the system's performance is analyzed with DVR compensation for three-phase voltage sags of approximately 0.5 pu (magnitude) at both 100% and 110% loading. Furthermore, the compensation for three-phase voltage swells of about 0.5 pu (magnitude) is also assessed with DVR at 100% and 110% loading. The effectiveness of different advanced PLL-based controllers, such as the PLL-PI, CDSC PLL-PI, MDSC PLL-PI, PLL-ANFIS optimized PI, CDSC PLL-ANFIS optimized PI, and MDSC PLL-ANFIS optimized PI controller is evaluated for compensating harmonics, voltage sags, and swells in each scenario. The results of this comparative study are detailed in Tables 3, 4, and 5, with Table 5 specifically highlighting the comparative analysis of various DVR controllers for voltage sag indices as per IEEE 1564 guidelines.

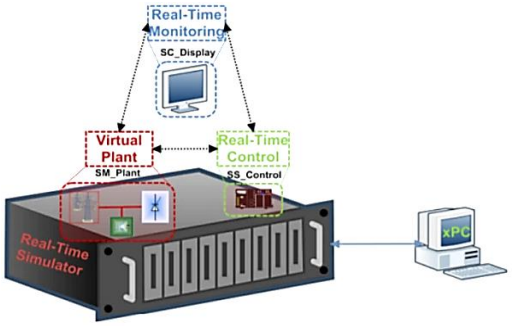

Figure 8. Schematic diagram of the OPAL-RT simulator

Figure 9. Experimental setup

The simulation results encompass four distinct cases evaluating the performance of DVR compensation systems:

- Test system without DVR compensation: This baseline scenario assesses the performance of the test system without any DVR compensation, providing a reference point for evaluating the effectiveness of subsequent compensations.

- Test system with DVR compensation for voltage harmonics: This scenario evaluates how well DVR compensation manages voltage harmonics under both 100% and 110% loading conditions. It helps in understanding how DVR can improve voltage quality and reduce harmonic distortions.
- Test system with DVR compensation for three-phase voltage sag: This scenario tests the DVR's effectiveness in compensating for three-phase voltage sags of around 0.5 pu (magnitude) under 100% and 110% loading conditions. Effective three-phase sag compensation is essential for ensuring balanced voltage levels across all phases.
- Test system with DVR compensation for three-phase voltage swell: This scenario evaluates the DVR's capability to address three-phase voltage swells of about 0.5 pu (magnitude) for 100% and 110% loading conditions. Proper compensation for three-phase swells ensures system reliability and equipment protection.

9.1. Comparative study of advanced PLL-based DVR controllers for harmonic mitigation

Table 3 provides a comparative analysis of different DVR controllers for harmonic mitigation. It includes various controllers like PLL-PI, CDSC PLL-PI, MDSC PLL-PI, PLL-ANFIS optimized PI, CDSC PLL-ANFIS optimized PI, and MDSC PLL-ANFIS optimized PI controller. The performance is evaluated in terms of the THD percentage under different loading conditions.

Table 3 presents a comparative analysis of various DVR controllers in terms of voltage quality compensation, specifically focusing on voltage harmonics. For critical and sensitive applications, such as those in hospital facilities, it is essential to keep voltage harmonics below 3%, as outlined in the guidelines by the IEEE 519 (2014b). In the test system without any DVR compensation, the voltage harmonics measured under 100% and 110% loading conditions were 25.24% and 30.02%, respectively. These values significantly exceed the recommended limits, indicating that the voltage quality is insufficient for such sensitive applications without proper compensation. The DVR compensation capabilities with various DVR controllers are assessed using a real-time simulator to evaluate their effectiveness in improving voltage quality with respect to voltage harmonics under both 100% and 110% loading conditions. The results of these evaluations are summarized in Table 3.

Figure 10 illustrates a radar chart depicting the performance of DVR voltage harmonic compensation. The chart features a hexagon representing the acceptable limits for voltage harmonics. Values plotted outside this hexagon are highlighted to show violations of the specified limits for each type of DVR controller. Under nominal loading conditions (100%), the designed DVR controller effectively keeps voltage quality within the acceptable limits. However, under increased loading conditions (110%), the DVR controllers with PI, fuzzy, and ANN control strategies fail to meet the required standards. In contrast, the DVR controllers with CDSC PLL-ANFIS optimized PI and MDSC PLL-ANFIS optimized PI perform better, successfully maintaining voltage quality within the specified limits even under higher loading conditions.

9.2. Comparative study of advanced PLL-based DVR controllers for voltage compensation

Table 4 compares different advanced PLL-based DVR controllers' effectiveness in voltage compensation, analyzing their ability to handle various voltage quality issues. Table 4 presents a comparative analysis of the performance of various DVR controllers, are PLL-PI, CDSC PLL-PI, MDSC PLL-PI, PLL-ANFIS optimized PI, CDSC PLL-ANFIS optimized PI, and MDSC PLL-ANFIS optimized PI controller regarding the mitigation of voltage sag and swell of approximately 0.5 pu (magnitude). The evaluation covers both three-phase (balanced conditions) and single-phase (unbalanced conditions) scenarios for durations ranging from 0.12 to 0.16 seconds, under both 100% and 110% loading conditions. The results, detailed in Table 4, show that the CDSC PLL- ANFIS optimized PI and MDSC PLL- ANFIS optimized PI controllers outperform the others in compensating the load voltage, as indicated by their superior performance in maintaining voltage within acceptable limits. This analysis highlights the advantages of advanced controllers like CDSC PLL- ANFIS optimized PI and MDSC PLL- ANFIS optimized PI in managing voltage quality issues more effectively than traditional methods.

9.3. Comparative study of advanced PLL-based DVR controllers for voltage sag indices as per IEEE 1564 guidelines

Table 5 evaluates the performance of advanced PLL-based DVR controllers in compensating for voltage sag indices, adhering to the IEEE 1564 guidelines. It provides insights into how well different controllers manage voltage sags according to industry standards. Table 5 presents a comparative analysis of the performance of various DVR controllers, are PLL-PI, CDSC PLL-PI, MDSC PLL-PI, PLL-ANFIS optimized PI, CDSC PLL-ANFIS optimized PI, and MDSC PLL-ANFIS optimized PI, specifically focusing on the calculated voltage sag indices during voltage sag compensation for both 100% and 110% loading conditions, as per the guidelines set by the IEEE 519 (2014a). According to these guidelines, VSLEI should be minimized because it represents the energy lost to the load, while the SS should be close to zero, reflecting the difference in the rated per-unit load voltage after compensation.

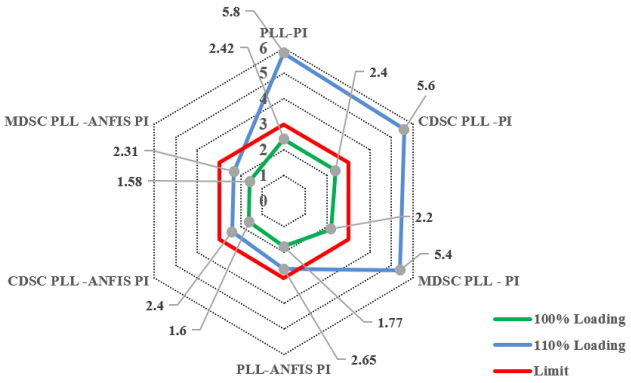

Figure 10. DVR voltage harmonics compensation (VTHD%)

Table 3. Comparative study of DVR controllers for harmonic mitigation

Harmonic mitigation	Loading (%)	Uncompensated	PLL-PI	CDSC PLL -PI	MDSC PLL - PI	PLL-ANFIS PI	CDSC PLL-ANFIS PI	MDSC PLL-ANFIS PI
VTHD %	100	25.24	2.42	2.40	2.2	1.77	1.6	1.58
	110	30.02	5.8	5.6	5.4	2.65	2.4	2.31

Table 4. Comparative study of DVR controllers for voltage compensation

Voltage Compensation	Loading (%)	Uncompensated	PLL-PI	CDSC PLL -PI	MDSC PLL-PI	PLL-ANFIS PI	CDSC PLL-ANFIS PI	MDSC PLL -ANFIS PI
0.5-pu of 3-ph	100	0.9753	0.9813	0.9823	0.9833	0.9953	0.9969	0.9979
Vsag	110	0.9414	0.9583	0.9594	0.9610	0.9892	0.9910	0.9920
0.-5pu of 3-ph	100	0.9582	0.9814	0.9824	0.9844	0.9962	0.9972	0.9983
Vswell	110	0.9432	0.9524	0.9534	0.9554	0.9883	0.9893	0.9912

Table 5. Comparative study of DVR controllers for voltage sag indices as per IEEE1564 guidelines

Voltage compensation	Loading (%)	Uncompensated		PLL-PI		CDSC PLL - PI		MDSC PLL - PI		PLL-ANFIS PI		CDSC PLL - ANFIS PI		MDSC PLL - ANFIS PI	
		VSLEI	SS	VSLEI	SS	VSLEI	SS	VSLEI	SS	VSLEI	SS	VSLEI	SS	VSLEI	SS
0.5 pu of 3 ph Vsag	100	12.65	0.5	1.06e-6	0.0248	4.02e-6	0.0032	2.82e-6	0.001 1	4.42e-6	0.0046	3.82e-6	0.0024	1.93e-6	0.0003
	110	17.34	0.6	18e-3	0.0588	1.21e-4	0.0112	1.02e-4	0.010 1	1.26e-4	0.0126	1.01e-4	0.0102	1.003e-4	0.0098

10. CONCLUSION

This test system places significant emphasis on the assessment of power quality through harmonic studies, following the IEEE 3002.8 guidelines, and the design of DVR controllers for real-world implementation aimed at improving power quality. These efforts align with the IEEE 519 (2014b) guidelines for PQ in specialized application systems. Additionally, the performance of each DVR controller is evaluated against voltage sag indices as per IEEE 519 (2014a) guidelines. The designed DVR controllers are tested in real time using HIL simulation powered by an FPGA Kintex unit and supported by the RT-LAB platform with the OPAL-RT 4200 real-time simulator. The testing encompasses various loading conditions, including both nominal (100%) and increased (110%) loads. Under nominal loading conditions, the DVR controller is expected to maintain voltage quality within acceptable limits. However, when the loading is increased to 110%, controllers based on PI-PLL methods fail to meet the required standards. In contrast, the CDSC PLL-ANFIS optimized PI and MDSC PLL-ANFIS optimized PI controllers perform better, successfully meeting the required limits. Despite their superior performance, these advanced controllers involve higher computational loads and increased costs compared to other methods. Given the higher accuracy required to meet the IEEE 519 (2014b) guidelines for specialized applications, these trade-offs are considered acceptable, especially for critical and sensitive applications like healthcare facilities, where maintaining high power quality is crucial. Future research is suggested to explore the use of other custom power devices for power quality improvement, employing optimization techniques and multilevel converter applications, and implementing them in suitable real-world environments.

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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare that they have no competing interests. All authors approved the final manuscript.

DATA AVAILABILITY

Data availability is not applicable to this paper as no new data were created or analyzed in this study.

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