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Single-stage transformer less multilevel boost inverter with zero leakage current for PV system

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ABSTRACT

Transformer less inverters (TIs) are highly efficient and have a high power density, making them a popular choice for grid-connected solar PV applications. However, certain topologies can lead to high-frequency common-mode voltage (CMV), which can cause issues such as high leakage current, electromagnetic interference, and an absence of safety. Our newly developed inverter is designed to be more efficient, cost-effective, and compact than traditional types while also addressing the issue of leakage current. This architecture eliminates leakage current by directly connecting the grid's neutral terminal to the PV's negative polarity, resulting in a low leakage current. Moreover, the inverter increases output voltage using only one voltage source and a few power devices, making it a cost-effective solution. Its modular form allows for an increase in output levels, further enhancing its cost-effectiveness. We conducted a comprehensive mathematical examination, and the MATLAB/Simulink results demonstrate its ability to increase the output voltage, eliminate leakage current, and maintain acceptable output voltage THD and current waveforms. These results and the inverter's safety features showcase significant improvements over traditional inverters and provide a secure and reliable solution for grid-connected solar PV applications.

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1. INTRODUCTION

In photovoltaic (PV) applications, transformers are commonly used for galvanic isolation and voltage ratio conversions. However, traditional transformers add weight, bulk, and expense to the inverter while reducing efficiency and power density. To address these issues and prevent safety concerns like ground fault and leakage currents, we aim to design an inverter that does not require transformers and can operate safely without additional precautions [1]–[4].

Various topological topologies, including circuit designs based on AC and DC dissociating, have been suggested in the literature to statement leakage current problems [5], [6]. The most often used and effective topology of this kind is the (HERIC) topology, built on the AC decoupling technique offered in this study. Other DC topologies contain H5 and various forms of H6. But still have the leakage current issue. Furthermore, conduction losses and the inverter's incapacity to the main disadvantages of such inverter topologies are increased [7]–[14].

Voltage using neutral-point-clamped (NPC) inverters is an additional option that reduces leakage current to a manageable range by keeping the common-mode voltage (CMV) constant. Increasing the output voltage levels also improves the quality of electricity. The most advanced and effective topologies in this category of inverter structures are the flying capacitor (FC)-based t-type and active neutral-point-clamped (ANPC). Recently, a five-level inverter built on an impedance source was described in [15]–[19].

This inverter's poor voltage gain, large component count, and leakage current are its key shortcomings. Consequently, EMI filters are included to reduce high-frequency volatility in CMV, which raises the inverter's cost. Conversely, in these topologies, the maximum AC voltage is just half the DC-link voltage; therefore, a two-stage power managing design with a further boost converter is required for low-voltage solar energy systems [20], [21]. As an alternative, a unique way for satisfying the demands of grid-connected renewable energy sources, particularly PV sources, is to use (CG) TI that may eliminate the issue of high-frequency (CMV), which causes leakage current. Based on the common-ground method, SCMLIs for reducing leakage current have lately acquired acceptance in the literature. They are described as a unique 5-L common-ground CG-type inverter using dual SCs, six switches, and a diode designed for PV systems. Additional sensors are required to balance the SC voltages [22]–[26]. Compact MLIs with boosting capabilities and minimal THD voltage generation are required for PV systems. MLIs based on switched capacitors (SC) have recently become popular as DC/AC voltage converters with boosting capabilities [27]. The SC unit's output voltage range is changeable.

It is dependent on the arrangement and spans a wide range. A traditional active neutral point clamp (ANPC) architecture utilizing capacitors was created [28]. Five output voltage levels beyond the load may be produced with a single DC voltage source, eight IGBTs, and three capacitors. However, there is no way to boost production levels in the load terminal.

Nevertheless, this arrangement does not have a way to raise the output voltage. Two new kinds of ANPC topologies were presented in [29]. These topologies are unable to enhance voltage, and this paper describes a new 5-level boost inverter with continuous gain controller capabilities. The inverter needs an inductor to supply continuous input current in both DC and AC modes, essential for photovoltaic and other renewable energy applications. Because the negative end of the DC source is linked to the neutral terminal of the grid, the design has minimal LC and few components.

The paper's structure follows: section 2 explains the construction of the suggested 5-level multilevel boost inverter. Section 3 explains the switch mechanism and pulse-generating method. Section 4 shows MATLAB Simulink findings for the inverter, which ends in section 5.

2. PROPOSED TOPOLOGY

Figure 1 shows the inverter's circuit architecture, which includes a boost inductor to sustain continuous input current and give adjustable gain voltage, seven switches, and two capacitors. The inverter uses a single DC source designed specifically for photovoltaic (PV) systems. Additionally, this provides a large boost gain, with the peak output voltage set at 2M/(1-D) for a 5-level output.

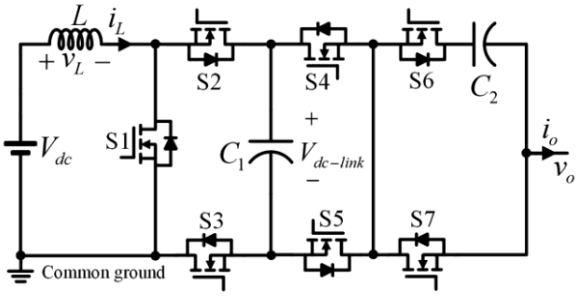


Figure 1. The basic block of the proposed 5-level inverter topology

2.1. Operating modes

In this section, Figure 2(a) illustrates the primary operational modes of the proposed 5-level converter. These establish distinct operating settings for each voltage stage, guaranteeing a consistent output voltage even during faults. Moreover, the system incorporates multiple charging and discharging modes to suit varying levels of inverter power. This design maintains the equilibrium of the capacitors' voltage and simplifies the

control of the boost duty cycle, resulting in additional benefits, for instance, capacitor voltage balancing. Furthermore, the input inductance within this inverter undergoes charging during the conduction phase of the IGBT S1, while it experiences discharge when the power switch S1 transitions to the off state. Consequently, the key waveforms pertinent to the proposed inverter are illustrated in Figure 2(b). As illustrated in Figure 2(a), the state (+1) consists of two operational conditions: the state of inductor charging and the state of inductor discharging; during the charging phase, the inductor is energized by the direct current (DC) source when switch S1 is activated, in this state the switches S1, S3, S4, S6are activated to reach the +1 level. During the discharging phase, switch S2 is activated, while switches S3, S4, and S6 remain conducting to reach the -1 level, and the same operation principle is used for the rest states.

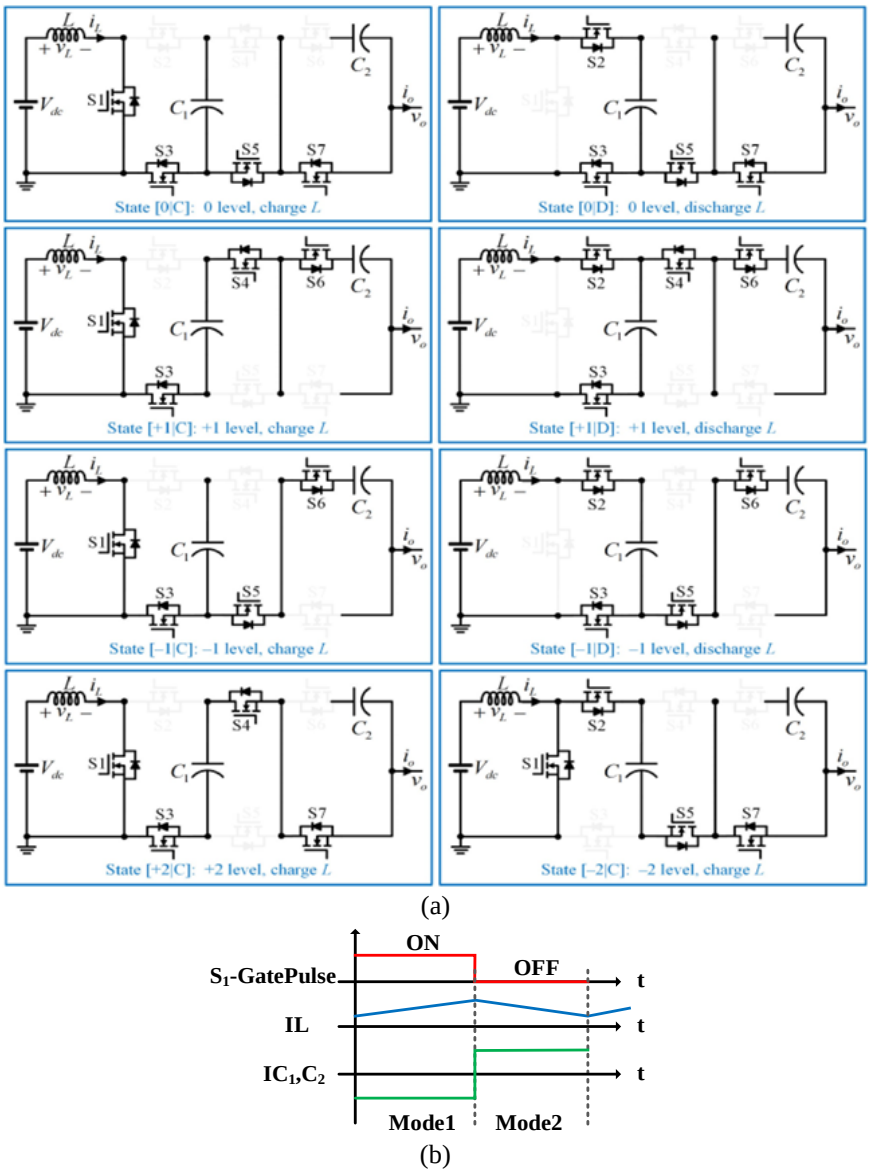


Figure 2. Operational modes of the (a) charging and discharging stages of the input boost inductor and (b) key waveforms associated with the inverter during both charge and discharge functions

2.2. Voltage gain analysis

The gain of the suggested inverter can be determined as follows, considering the DC source voltage and the AC output voltage.

$$Gi = \frac{2M}{1-D} \quad (1)$$

Since every capacitor in the proposed inverter has the same amount of charge, the voltage of every capacitor may be determined as follows:

$$V_{C1} = V_{C2} = \frac{V_{DC}}{1-D} \quad (2)$$

As a result, the highest maximum voltage is equal to the total voltages across the previously stated capacitors. Thus, the following methods can be used to obtain it:

$$V_{O,Max} = \frac{2V_{DC}}{1-D} \quad (3)$$

Table 1 shows equations demonstrating the relationship between the output voltage and the modulation index. Variations in the duty cycle (D) may affect the peak value of the waveform. Table 2 shows the disparities in maximum output voltage. When the modulation index surpasses 0.5, the level shift PWM (LS-PWM) approach creates a 5-level waveform for the inverter output from a sinusoidal reference voltage signal. When the modulation index falls below 0.5, the converter output switches to a three-level waveform.

Table 1. The association between a modulation index and the output waveform

Output voltage	Rang of modulation index	Range of output voltage waveform
$V_O = \frac{2MV_{DC}}{1-D}$	0 to 1	V_O => 0 *to* $\frac{2V_{DC}}{1-D}$

Table 2. illustrates various modulation index ranges

Modulation index	Output levels	Gain voltage
M > 0.5	5	$\frac{V_{O,peak}}{V_{DC}} = \frac{2}{1-D}$
M < 0.5	3	$\frac{V_{O,peak}}{V_{DC}} = \frac{1}{1-D}$

2.3. Design factors

This section covers the suggested inverter model concerns for switches, input boost inductors, and capacitors. As demonstrated by the preceding formulations, equations indicating the voltage stress of the switches are constructed.

$$V_{4,6} = \frac{1}{1-D}V_{DC}, V_{1,2,3,5,7} = \frac{2}{1-D}V_{DC} \quad (4)$$

Additionally, the input boost inductor may be developed by the subsequent equation:

$$L_{in} \geq \frac{DV_{DC}}{f_s \Delta i_L} \quad (5)$$

Furthermore, the following definition may be applied to the values of the inverter capacitors:

$$C_{1,2,\ldots n} \geq \frac{D(1-D)I_o G}{f_s \Delta V_C} \quad (6)$$

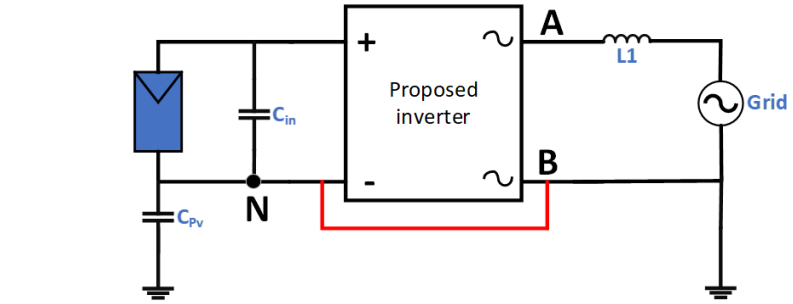
3. METHODOLOGY

Due to the input and output terminals sharing common ground, the suggested inverter has zero CMV. Figure 3(a) shows that the sinusoidal waveform value from point B to neutral point N is zero (VBN). The PV array's parasitic capacitor (C_{PV}) is short-circuit due to the inverter's common ground capabilities. Consequently, the leakage current through C_{PV} is also zero. As a result, the inverter's CMV value can be calculated as (7).

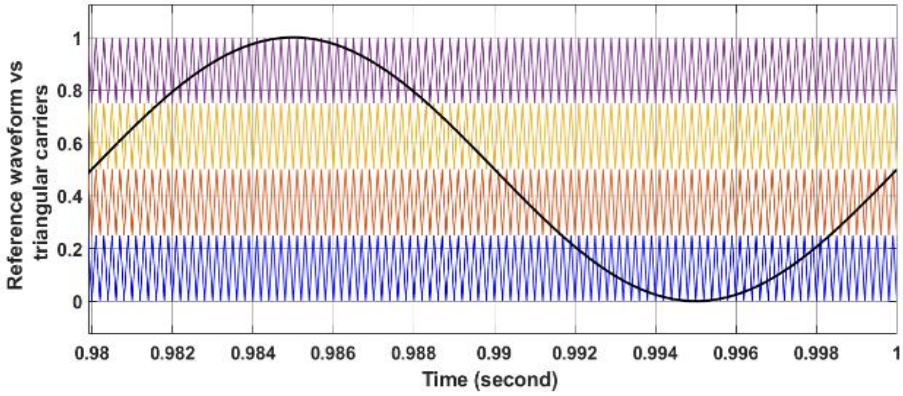
$$V_{CM.Total} = \frac{V_{AN}}{2} + (V_{AN})\left(\frac{-L_1}{2(L_1)}\right) = 0 \quad (7)$$

3.1. Modulation and switching rules

The proposed topology produces a sinusoidal waveform at the output by controlling the IGBTs with level shift modulation. Figure 3(b) shows the carrier signal waveforms concerning the reference sinusoidal waveform. Four triangular carrier waveforms are included in a 5-level inverter. Every voltage state of the inverter corresponds to one or more switching situations. Table 3 shows the switching table with five levels from -2 V to +2 V3.



(a)



(b)

Figure 3. The inverter structure common ground and the level shift PWM, (a) the planned inverter association to the AC grid's general schematic and (b) triangle carrier signals compared to the suggested inverter's reference sinusoidal waveform

Table 3. Switching states for 5-level MLI

Level / Switches	Power switches							Inductor
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	
0	1	0	1	0	1	0	1	Charge
	0	1	1	0	1	0	1	Discharge
+1	1	0	1	0	0	1	0	Charge
	0	1	1	1	0	1	0	Discharge
-1	1	0	1	0	1	1	0	Charge
	0	1	1	0	1	1	0	Discharge
-2	1	1	0	0	1	0	1	Charge
+2	1	0	1	0	0	0	1	Charge

4. RESULTS AND DISCUSSION

As previously explained, the proposed inverter operates in continuous boost mode with a constant input current and 0% leakage current. Furthermore, the loss value findings using the PLECS software illustrate the proportion of losses for each inverter component. The critical parameter values used through the simulation are detailed in Table 4. Table 5 contrasts the proposed inverter to a variety of topologies.

Figure 4(a) illustrates the five-level output voltage characterized by a peak value of 240 V, utilizing the parameter specifications provided in Table 4. Figure 4(b) illustrates the variations in output voltage as the duty cycle is adjusted in increments of 10%, ranging from D = 80% to D = 20%. A notable attribute of the proposed inverter is its ability to regulate the peak output voltage across a broad operational spectrum.

Figure 4(c) illustrates the modulation index value altered from 0 to its maximum (M = 1). The converter produces a three-level voltage when M < 0.5 and a five-level waveform when M > 0.5, as detailed in Table 2. Figures 5(a) and 5(b) present the voltage measurements of the topology capacitors (C1 and C2).

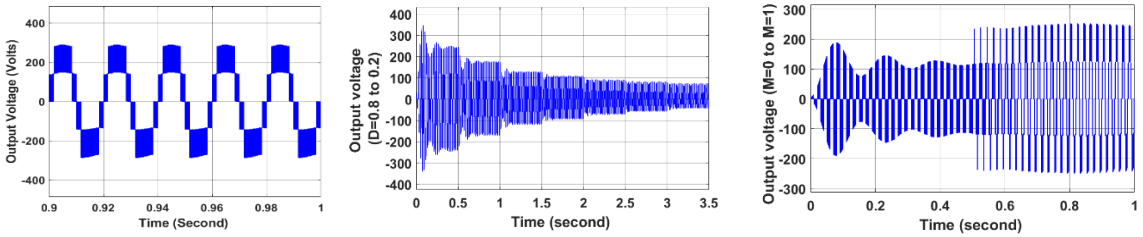
Table 4. Simulation parameter estimates of the proposed inverter

Value	Parameter	Value	Parameter
3 mH	Input inductor (L_b)	24 V	Source (V_{dc})
100 Ω + 10 mH	Inductive load	1200µF	Capacitor (C_1 and C_2)
Level shift PWM	PWM	10 kHz	$F_{(SW)}$
80%	D	1	M

Table 5. Comparison of 5-level boost inverters with other inverter topologies

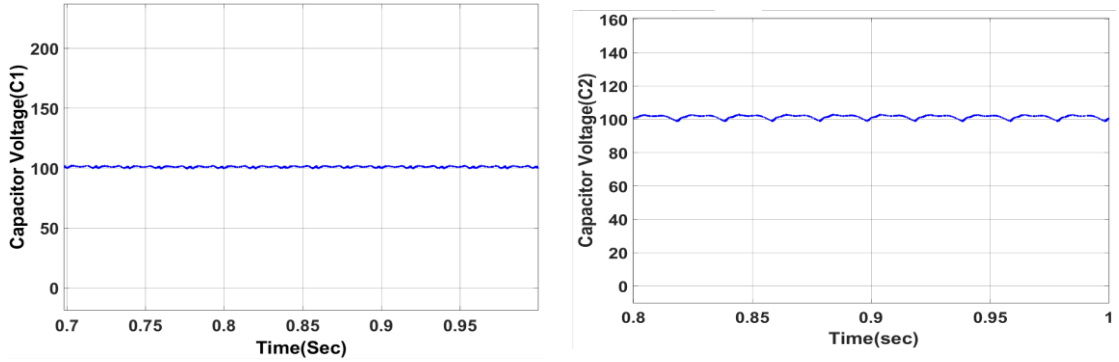
Structure	S	D	C	L	N_{Level}	Gain	CC	CG
[27]	3	6	2	2	3	$\frac{DV_{dc}}{(1-D)}$	×	✓
[28]	7	0	2	1	5	$2V_{dc}$	×	×
[29]	6	3	2	1	3	$\frac{DV_{dc}}{(1-D)}$	×	✓
Proposed 5-level	7	0	2	1	5	$\frac{2MV_{dc}}{(1-D)}$	✓	✓

*S: Switching number, D: Diodes number, C: Capacitors number, L: Inductors number, N_{Level}: Number of voltage levels, Gain: Boost gain, CC: Continuous input current, CG: Common ground, and M: Modulation index



(a) (b) (c)

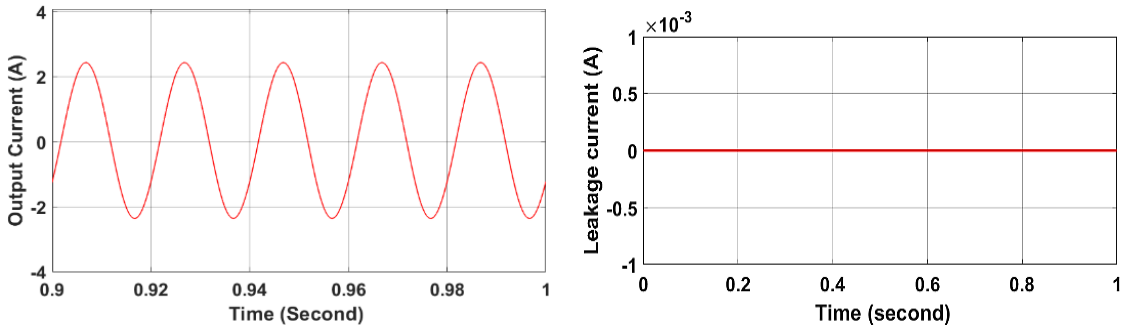
Figure 4. The output voltage waveforms are as follows: (a) D = 80%, M = 1 output voltage waveform, (b) duty-cycle charging from D = 80% to D = 20, and (c) modulation index changing from M = 0 to M = 1



(a) (b)

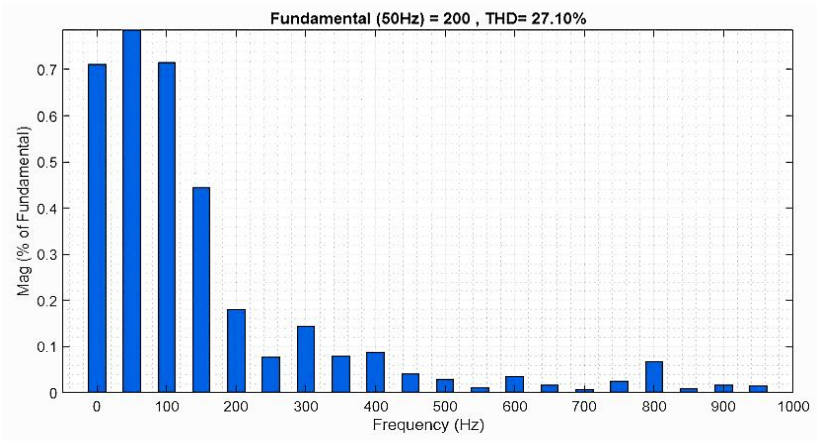
Figure 5. Voltage waveforms of the virtual DC source capacitors: (a) VC1 and (b) VC2

Figure 6(a) illustrates the absence of leakage current across the parasitic capacitance of the input source. Furthermore, Figure 6(b) depicts the waveform of the inverter's output current, characterized by the attributes previously delineated in Table 4. Additionally, Figures 7(a) and 7(b) disclose that the output voltage and current of the inverter exhibit total harmonic distortion (THD) values of 27.10% and 0.65%, respectively.

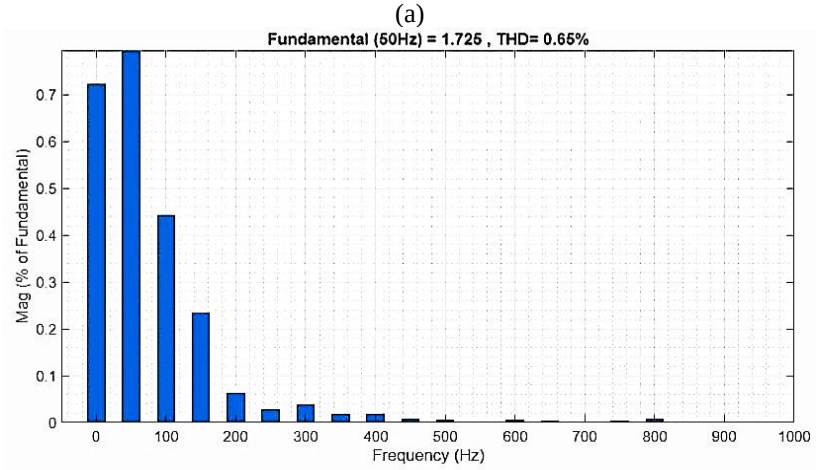


(a) (b)

Figure 6. The output current waveform, (a) zoomed output current waveform and (b) leakage current waveform



(a)



(b)

Figure 7. Frequency spectrum and THD of the inverter, (a) output sinusoidal waveform and (b) output current

4.1. Comparative and losses analysis

The next sections provide a comparative comparison of the suggested five-level inverter and other innovative topologies. Table 5 indicates the suggested inverter has a high voltage gain and a constant input current, which makes it especially appropriate for photovoltaics. Figures 8(a) and 8(b) also show the simulated converter. Additionally, Figure 9(a) shows the comparative study of voltage gain. Additionally, the efficiency curve of the converter and the percentage distribution of losses among the inverter's components are shown, while variable the output power from 0 to 1500 Watts with real conditions conferring to the values in Table 6 that are shown in Figures 9(b) and 9(c), correspondingly.

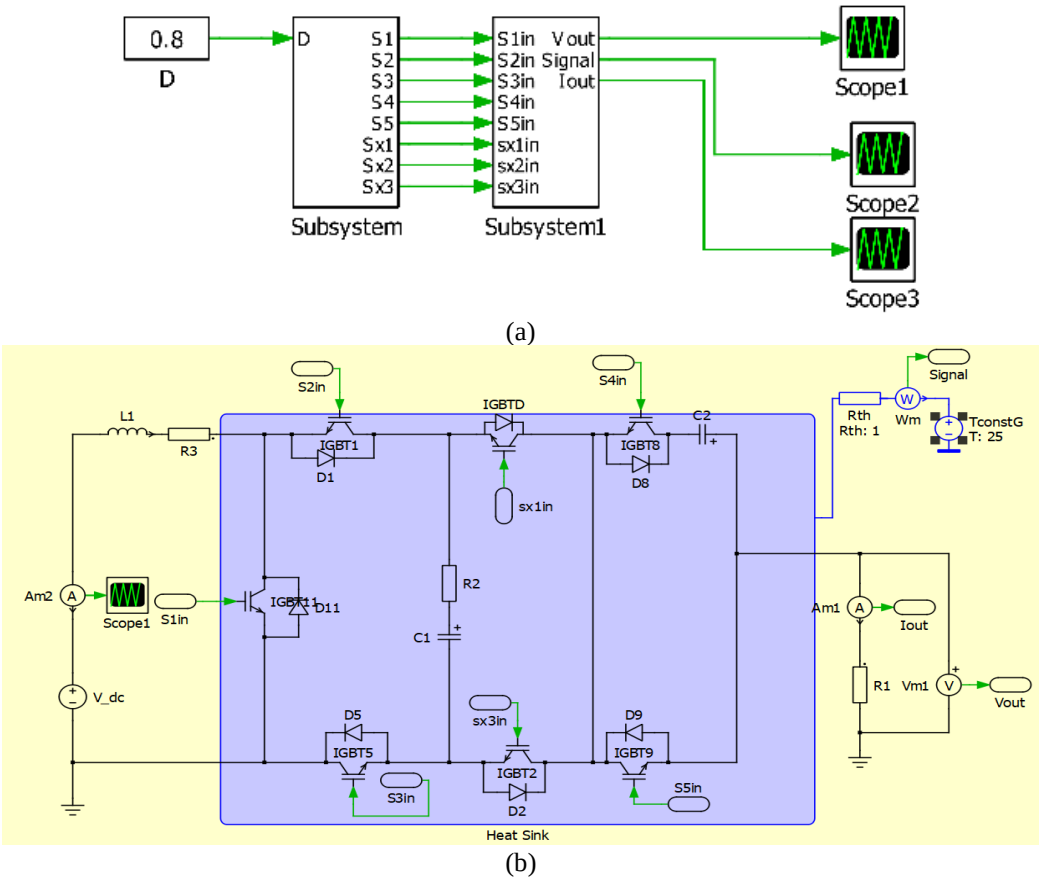


Figure 8. The modeled converter with PLECS software: (a) control system and (b) proposed converter

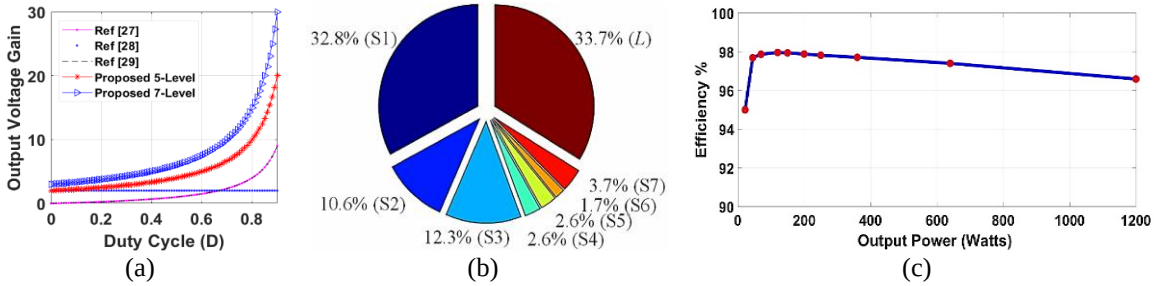


Figure 9. Comparison of an assessment of the proposed inverter's voltage gain and loss: (a) output voltage gains about the D, (b) loss of each component, and (c) efficiency curve

Table 6. Components and factors applied to calculate losses and efficiency

Parameter	Value	Parameter	Value
Power switches	IGBT-FGH60N60SMD	$V_{(dc)}$	24 V
$L_{(in)}$	3mH (10mΩ internal resistor)	D	80%

5. CONCLUSION

This paper proposes a new five-level step-up common ground inverter with a reduced number of power switches specifically developed for photovoltaic and other renewable energy systems. The proposed inverter demonstrates the capability to attain elevated output voltages utilizing a single-source inverter configuration. Owing to the shared ground connection between the direct current (DC) input and the alternating current (AC) output, this inverter has effectively mitigated the issue of leakage current. The various switching methodologies corresponding to every output voltage level have been elucidated, yielding benefits such as

enhanced voltage balance out among capacitors and straightforward duty-cycle regulation. The architectural design of the inverter achieves a doubling of the boost gain (2D/1−D) within a five-level configuration. A comprehensive analysis of the inverter and a comparative evaluation of its performance relative to other contemporary topologies are provided. Ultimately, simulation outcomes obtained through the MATLAB/Simulink environment are presented to validate the inverter's efficiency.

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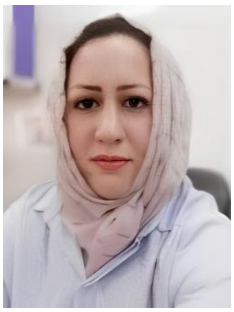

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