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Design and analysis of seven-level hybrid modified H-bridge multilevel inverter

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ABSTRACT

This paper introduces a novel boosting multilevel inverter that utilizes switched capacitors. Current multilevel inverters (MLIs) face several issues, such as complex structures, intricate switching controls, and challenges in generating gate pulses, numerous components, and high voltage stress on semiconductors. The increase in the number of levels adds to the complexity and cost of the circuit and can reduce reliability in some cases. The proposed topology creates a 7-level voltage waveform using 9 switches, 1 diode, and 2 capacitors, and it triples the voltage gain. The capacitors maintain self-balanced operation without the need for additional circuits. A simple logic gate-based pulse-width modulation (PWM) technique is presented to ensure power balancing of the capacitors. The proposed 7-level switched capacitor boosting multilevel inverter features a reduced switch count, lower voltage stress, and built-in fault tolerance. The paper includes a comprehensive comparison of various related topologies. The proposed topology is simulated in PSIM, with simulation results presented for different parameters.

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1. INTRODUCTION

In industrial applications, DC-AC power converter systems are favored for their nearly sinusoidal output voltage and high-power handling capacity. Traditional three-level inverters, however, necessitate a large output filter and a high DC link voltage [1], [2]. To enhance power quality and efficiency, there is a need for inverters with a greater number of output voltage levels [3], [4]. In smart grids or microgrids, multilevel inverters can be seamlessly integrated with renewable energy sources like photovoltaic (PV) cells. Leading electric vehicle manufacturers have recently adopted higher-voltage batteries to achieve faster charging times, increased power density, and reduced current consumption [5], [6]. As the trend in electric vehicles shifts toward higher DC-link voltages, certain multilevel inverter architectures are being considered as practical and effective alternatives to two-level inverters [7]. Multilevel inverters offer several advantages, including higher efficiency, greater power density, improved waveform quality, and inherent fault-tolerance [8], [9].

Multilevel inverters (MLIs) have emerged as the most advanced power conversion technology for various applications, such as electric motor drives, flexible AC transmission systems (FACTS), and renewable energy resources (RERs) [10], [11]. The popularity of MLIs in medium- to high-power operations is due to their numerous benefits, including low harmonic content, reduced power consumption through power electronic switches, and significantly decreased electromagnetic interference (EMI) at the receiving end.

Through the above discussion, it is clear that the main limitations of the recently proposed 7-level SCMLIs include a higher component count, increased total standing voltage, higher maximum blocking voltage, and a lower boosting factor. The novel 7-level SCMLI presented in this brief has the following key features:

- The proposed 7-level MLI uses only one DC source;
- The switch and capacitor counts are significantly reduced in this 7-level MLI;
- In the absence of a closed loop, the capacitors self-balance;
- Four switches operate at the fundamental frequency, and about 50% of the switches conduct for each voltage level production, resulting in minimal net power loss;
- Compared to previous MLIs, the output voltage of the proposed MLI is boosted to three times the input voltage; and
- The designed MLI can handle both high and low power factor (PF) loads.

2. PROPOSED METHODOLOGY

2.1. Switching topology seven-level mli topology

Figure 1 illustrates the simplified structure of the planned seven-level architecture. It consists of nine switches (S1, S2, S3, S4, S5, S6, H1, H2, H3, H4), two capacitors (C1, C2), one diode (D1), and one voltage source (Vdc) to create a 7-level output voltage (V_0). The SPWM (switch pulse width modulation) technique is used to generate the switching pulses and the required output voltage.

The final voltage is generated during both the positive and negative half cycles using an H-bridge. Vdc can directly charge each of the capacitors connected to the proposed inverter. Table I describes the different scenarios for each level and their effects on the capacitor's state. It shows that to create an output voltage of 3 Vdc, switches S1, S4, H1, and H4 are turned "on," while switches S2, S3, S5, H2, and H3 are turned "off." In the table, "on" is represented by 1, "off" by 0, "discharging" by "D," "charging" by "C," and "not connected" by "NC." The switch statuses listed in Table 1 determine all the voltage levels.

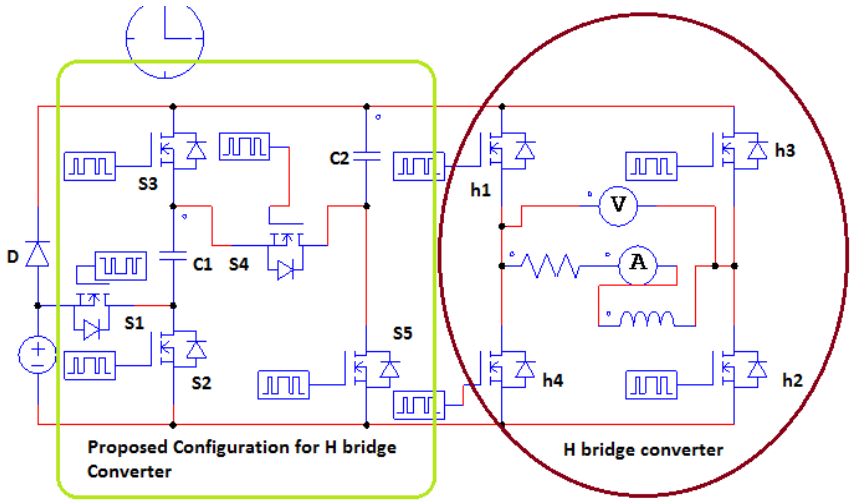

Figure 1. PSIM simulation of a seven-level hybrid modified H-bridge multilevel inverter

Table 1. The planned 7-level MLI topology's switching state

Switching states									Diodes and capacitors			Output
S_1	S_2	S_3	S_4	S_5	H_1	H_2	H_3	H_4	D_1	C_1	C_2	V_o
1	0	0	1	0	1	0	0	1	0	D	D	3 V_{dc}
1	0	1	0	0	1	0	0	1	0	D	NC	2 V_{dc}
0	1	1	0	1	1	0	0	1	1	C	C	V_{dc}
0	1	1	0	1	1	0	1	0	1	C	C	0
0	1	1	0	1	0	1	0	1	1	C	C	0
0	1	1	0	1	0	1	1	0	1	C	C	-V_{dc}
0	0	0	1	0	0	1	1	0	1	NC	D	-2 V_{dc}
1	0	0	1	0	0	1	1	0	0	D	D	-3 V_{dc}

2.2. Operational modes

This subsection presents the governing principle of the proposed SCMLI. Figures 2(a)-2(d) (see in appendix) illustrate the circuits for the voltage levels +0Vdc, +1Vdc, +2Vdc, and +3Vdc with positive charging current pathways and a load current i0 > 0. Table 1 shows the switching parameters for achieving various positive and negative voltage levels. Here, "1" and "0" denote the "on" and "off" states of a switch and a diode, respectively, while "D," "C," and "NC" denote the "discharging," "charging," and "not-connected" states of the capacitor. The following is a description of how different voltage levels are generated:

i) State 3 Vdc

The load voltage is realized at 3Vdc by combining the voltage of C1 and C2 with Vdc. In this mode, both capacitors C1 and C2 are discharging, and switches S1 and S2 are on. If switches H1 and H3 are on, the voltage across the load is +3 Vdc presented in Figure 2(a). When switches H2 and H4 are on, the voltage across the load is -3 Vdc, as shown in Figure 2(e).

ii) State 2 Vdc

Vdc and C1 are connected in series. Switches S1, S3, H1, and H4 are turned on to provide a voltage level of +2Vdc across the load, as shown in Figure 2(b). In this mode, capacitor C1 is discharging, and capacitor C2 is not connected. To create -2Vdc, Vdc, and C2 are connected in series, and the appropriate switches are activated. Switches S4, H2, and H3 are turned on, and diode D1 becomes forward biased to provide a voltage level of -2Vdc across the load, as shown in Figure 2 (f). At this voltage level, capacitor C2 is discharging, and capacitor C1 is not connected.

iii) State Vdc

This voltage can be achieved by directly placing Vdc across the load or by using the capacitor voltages across C1 or C2. For creating +Vdc across the load, switches S2, S3, S5, H1, and H4 are turned on, and diode D1 becomes forward biased, with capacitors C1 and C2 charging, as shown in Figure 2(C). To create -Vdc, switches S2, S3, S5, H2, and H3 are turned on, and diode D1 becomes forward biased, with capacitors C1 and C2 also charging, as shown in Figure 2(g).

iv) State 0 Vdc

When either H1 and H3 or H2 and H4 are switched on, the 0Vdc voltage level is observed across the load terminals, as described in Figures 2(d) and 2(h). To charge capacitors C1 and C2, switches S2, S3, and S5 are turned on, and diode D1 becomes forward-biased.

3. METHODS

3.1. Mathematical calculations

In this section, the voltage across the switches S1, S2, S3, S4, S5, H1, H2, H3, and H4 is calculated as described below, leading to the calculation of TSV. The voltage stress across various switches is illustrated in Figure 3. The (1) determines the MBV of switches S1, S2, S3, and S4, while (2) provides the MBV of switch S5, and in (3) gives the MBV of switches H1, H2, H3, and H4. Thus, TSV is determined using (3), and the diode's PIV is provided by (4).

MBV for switches S1, S2, S3, and S4 is calculated as Vdc, as shown in (1). For switch S5, the MBV is 2 Vdc, according to (2), while for switches H1, H2, H3, and H4, the MBV is 3 Vdc, as per (3). Consequently, TSV is set at 18 Vdc, as per (4), and the diode's PIV is represented by Vdc in (5).

$$MBV(S_1,S_2,S_3,S_4)=V_{dc} \quad (1)$$

$$MBV(S_5)=2V_{dc} \quad (2)$$

$$MBV(H_1,H_2,H_3,H_4)=3V_{dc} \quad (3)$$

$$TSV=18\ V_{dc} \quad (4)$$

$$PIV_{diode}=V_{dc} \quad (5)$$

TSV plays a crucial role in high-voltage conditions. The per-unit (pu) values of TSV and MBV for the intended topology are defined as shown in (6) and (7), respectively:

$$\text{Per unit TSV (pu)} = \text{TSV/peak output voltage} \quad (6)$$

$$\text{Per unit MBV (pu)} = \text{MBV/peak output voltage} \quad (7)$$

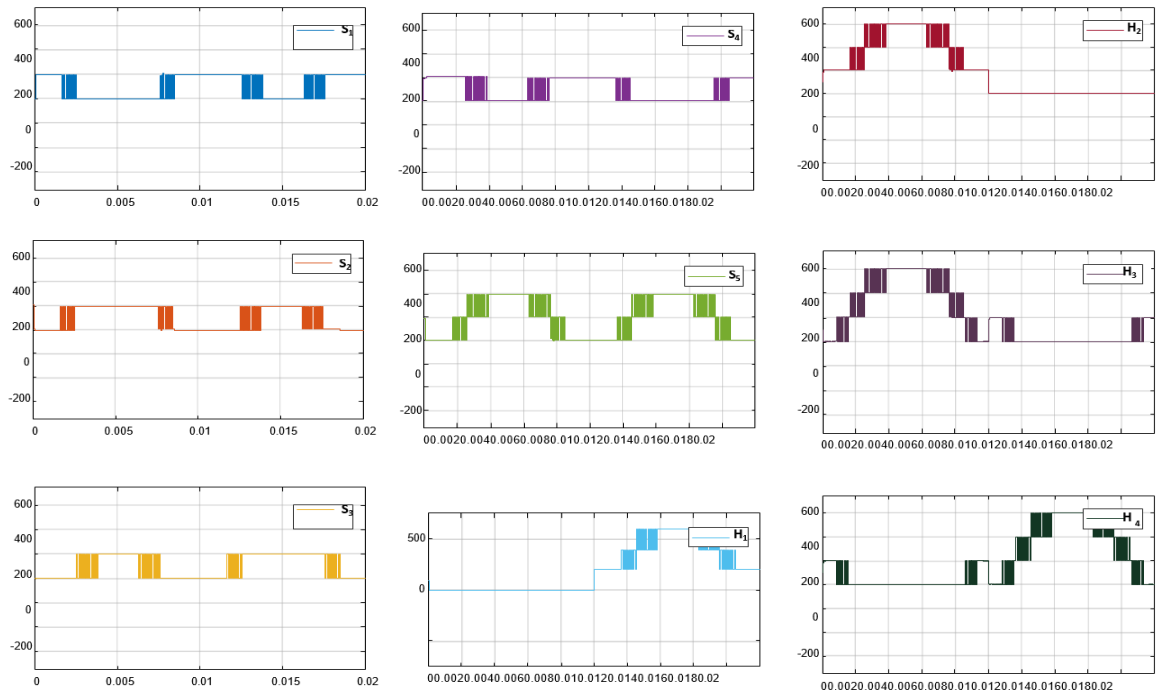

Figure 3. Voltage stress across the switches (S_1 to H_4)

3.2. Logic gate-based PWM

Various types of continuous pulse width modulation (CPWM) techniques employed in this context encompass SPWM and SVPWM [12], [13]. In CPWM methods, continuous switching occurs due to the consistent intersection of carrier and reference signals within the carrier band boundaries, where the reference signal is maintained. Conversely, in discontinuous pulse width modulation (DPWM), switching ceases during this period as the reference signal is clamped at the maximum positive or negative value within the carrier band [14]-[16]. In carrier-based space vector pulse width modulation (SVPWM) and DPWM systems, it's essential to obtain a zero-sequence signal and integrate it with the reference signal to generate a modulating signal [17]-[19]. One of the advantages of SPWM technology lies in its uniform switching frequency [20], [21]. Maintaining a constant switching frequency simplifies the thermal design of switching components since component losses can be accurately calculated [22], [23]. This rationale underscores the planned adoption of SPWM technology in the proposed topology [24], [25].

4. RESULT AND DISCUSSION

A comprehensive PSIM model is proposed for the suggested architecture to develop a 7-level inverter, aimed at verifying the conceptual viability of the intended inverter. This model employs four IGBTs arranged in an H-bridge configuration to emulate the functionality of the 7-level 9-switch inverter, generating both positive and negative voltages akin to a single-phase inverter. A resistive load is incorporated, with the source voltage set to 200 V.

In Figure 4, a simulation waveform is depicted for a supply voltage (Vdc) of 200 V and a resistive load (R) of 300 Ω. Additionally, an inductor with a value of L = 100 mH is introduced. In Figure 5, a simulation waveform is depicted for a supply voltage (Vdc) of 100 V and a resistive load (R) of 300 Ω. Additionally, an inductor with a value of L=200mH is introduced. The simulation waveform is presented, illustrating the output boosted to three times the input voltage without any closed-loop control. Furthermore, Figures 4 and 5 showcase a simulation waveform demonstrating the output voltage and load current with a modulation index of 0.51. Figure 6, the charging voltage across capacitors C1 and C2. It's observed that the final steady-state voltages across C1 and C2 are measured at 200 V. The FFT analysis shows that the THD across the load is 17.36 % of the fundamental frequency, and the voltage is observed as 296.4, as shown in Figure 7.

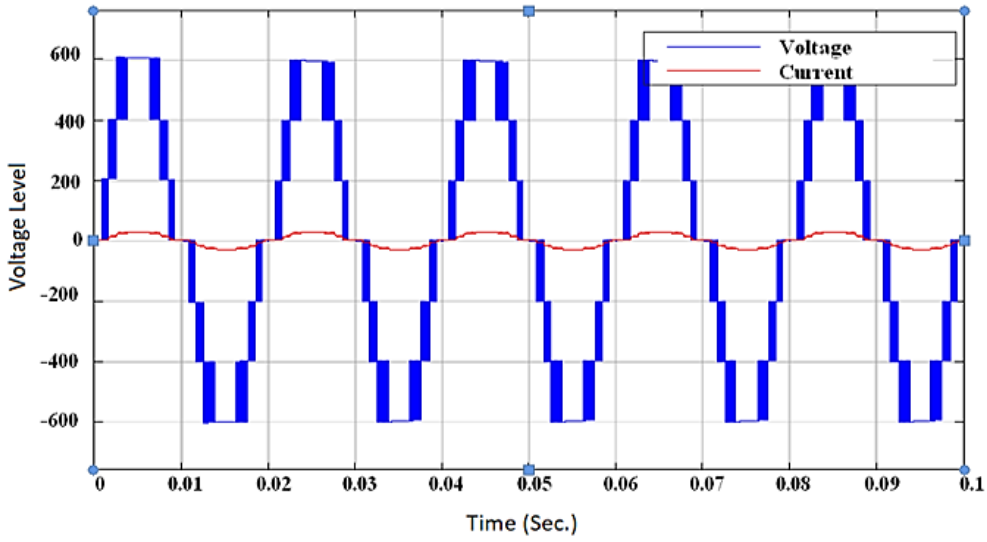

Figure 4. Voltage and current waveform of the proposed converter (Vdc = 200, R = 300, L = 100 mh)

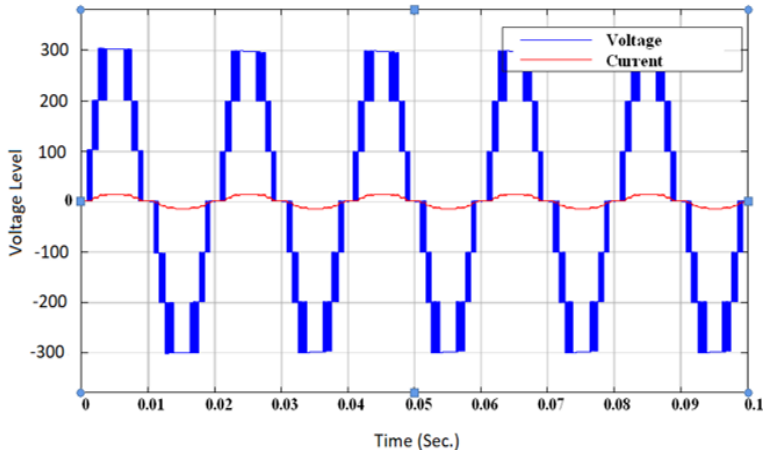

Figure 5. Voltage and current waveform of the proposed converter (Vdc = 100, R = 300, L = 200 mh)

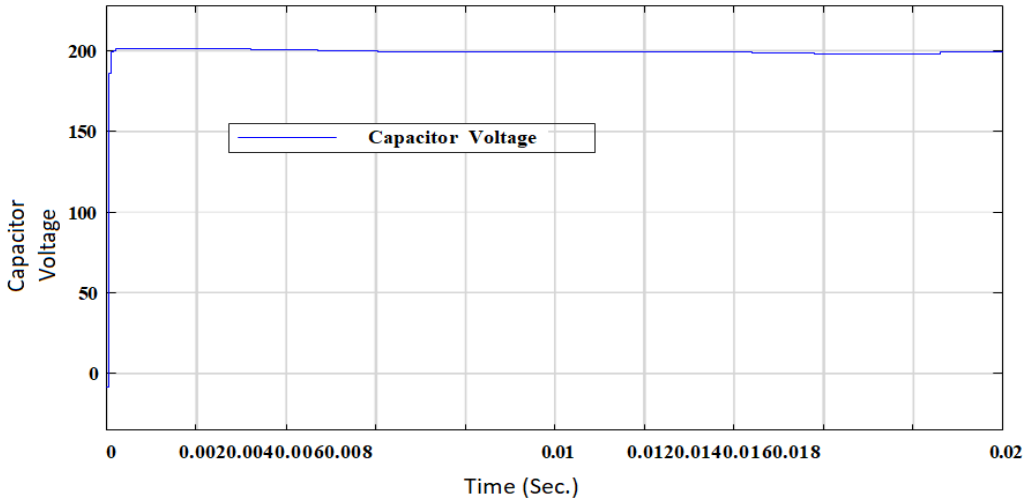

Figure 6. Voltage across the capacitor

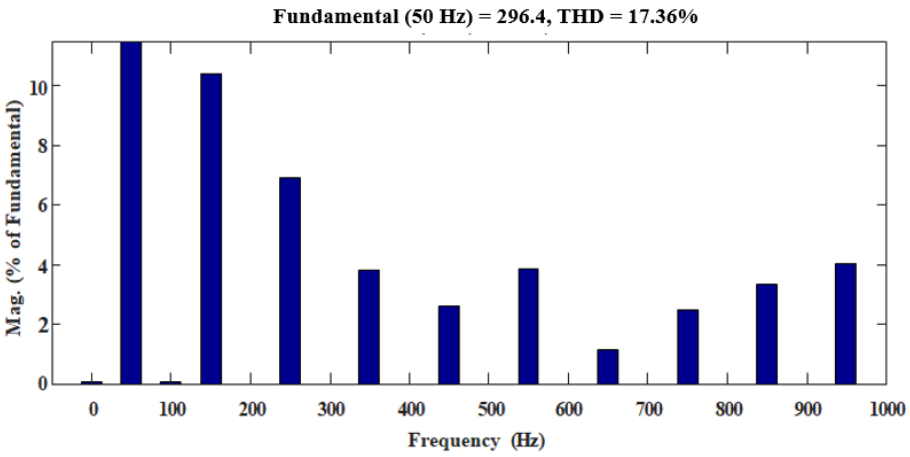

Figure 7. THD of the voltage across the load

4 CONCLUSION

This article introduces a proposed topology featuring seven levels in its Simulation model. The suggested converter boasts a boosting factor of 3 and is capable of generating seven distinct levels of output. Detailed discussions are provided on the suggested inverter's circuit configuration, operational concept, and voltage stress analysis, including a thorough examination of the capacitor selection process. An analysis comparing the performance of similar inverters reveals that the suggested inverter achieves the same range of output voltage values using fewer switches and drivers, rendering it a more cost-effective option. Voltage balancing is autonomously managed by capacitors C1 and C2. The feasibility and performance of the Simulation model are extensively evaluated. Switches are controlled via SPWM, with the switching sequence primarily focused on balancing capacitor charging/discharging and the capacitors themselves. Additionally, the total harmonic distortion (THD) of the recommended converter is scrutinized.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Arpan Dwivedi	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓			
Raman Kumar		✓				✓		✓	✓		✓	✓		
Sailesh Sourabh	✓		✓	✓			✓		✓		✓			
Vikash Rajak						✓				✓				
Vikash Kumar Singh					✓		✓			✓		✓		
Maruti Nandan Mishra		✓						✓	✓	✓				

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

Data availability is not applicable to this paper as no new data were created or analyzed in this study.

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APPENDIX

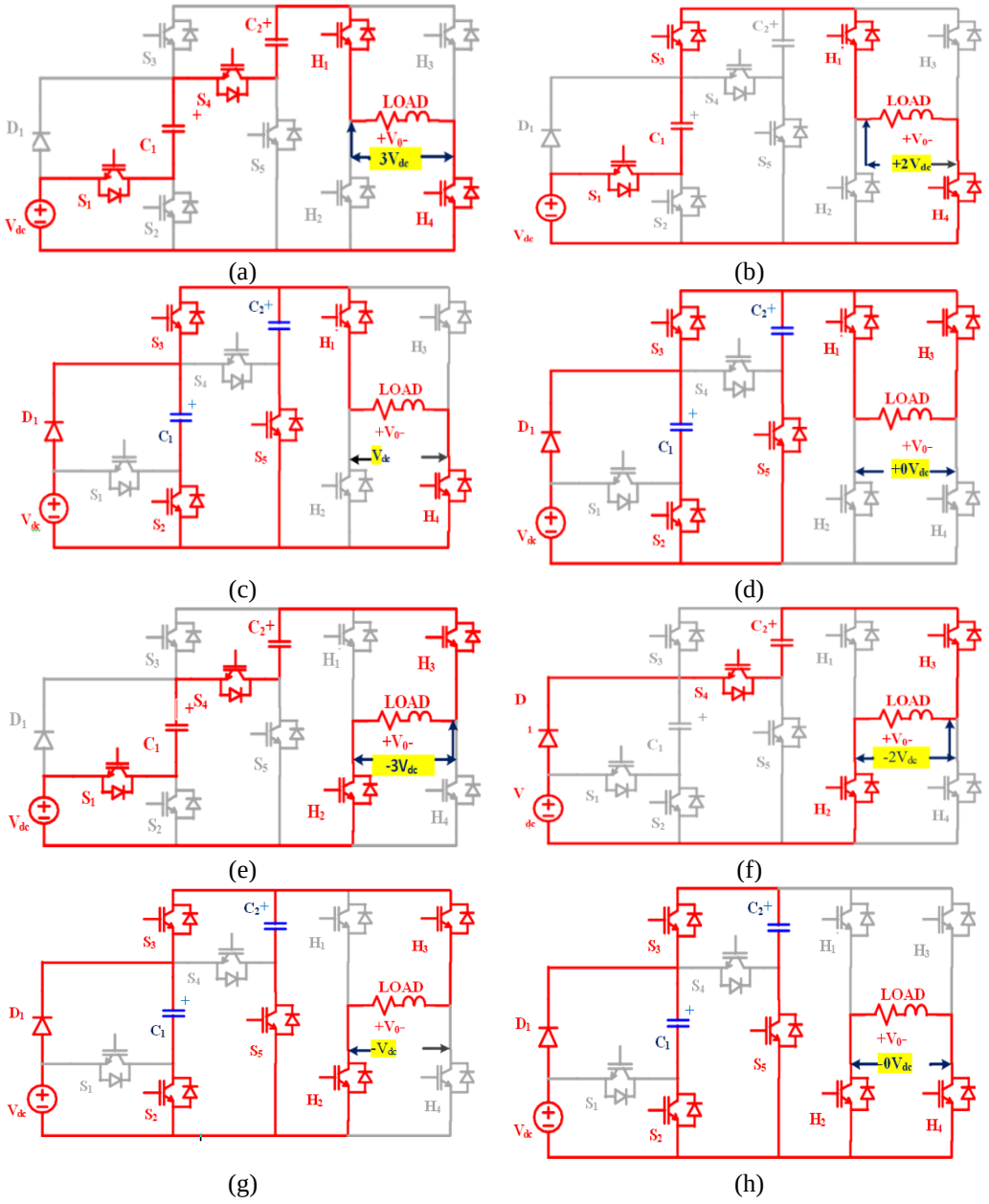

Figure 2. Eight operational modes of the proposed SCMLI during one full cycle: (a) +3 Vdc, (b) +2 Vdc, (c) +Vdc, (d) 0 Vdc, (e) -3 Vdc, (f) -2 Vdc, (g) -Vdc, and (h) 0 Vdc (negative half-cycle)

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