International Journal of Power Electronics and Drive System (IJPEDS)
Vol. 16, No. 3, September 2025, pp. 1740~1751
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v16.i3.pp1740-1751

Analysis of cascaded H-Bridge multilevel inverters using SPWM with multi-sinusoidal reference

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Article Info

Article history:

Received Sep 26, 2024
Revised May 15, 2025
Accepted May 25, 2025

Keywords:

5, 7, 9, 11, 13, and 15-level
CHMI
Multilevel inverter
Multi-sinusoidal reference
SPWM

ABSTRACT

Multilevel inverters have become the preferred choice for medium voltage and high-power applications due to their superior waveform quality, reduced stress on switching components, and overall enhanced performance. Among these, the cascaded H-bridge inverter stands out for its simpler control and modulation techniques, as well as its greater efficiency compared to other multilevel inverter topologies. This paper presents the design and performance evaluation of a cascaded H-bridge multilevel inverter (CHMI) for five, seven, nine, eleven, thirteen, and fifteen levels, utilizing sinusoidal pulse width modulation (SPWM) in MATLAB Simulink. The proposed technique, the multi-sinusoidal reference, is implemented by comparing multiple sinusoidal wave signals with a carrier triangular signal, with the resulting comparison pulses used to control the inverter's switching. The output results indicate that as the number of levels in multilevel inverters increases, the total harmonic distortion (THD) decreases, and the output voltage improves.

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1. INTRODUCTION

Multilevel inverters (MLIs) have been widely studied in recent years because of their potential to enhance power quality, suppress harmonics, and improve efficiency in high-power and medium-voltage applications [1]-[3]. The key benefits of multilevel inverters are the capability to synthesize a sinusoidal output voltage waveform with reduced harmonic content at high power switching frequency that enhances the efficiency and reduces the mechanical stresses on the output electrical equipment [4]-[7]. They have been largely employed in renewable energy systems, motor drives, and grid-connected power electronics [8]-[9]. They noted that among different existing MLI topologies, the H-bridge multilevel inverter (CHMI) could take the lead over the others due to the modularity, fewer components, and ability to produce high output voltage without the need for heavy transformers [10]-[11]. One of the main considerations in multilevel inverters is to attain low total harmonic distortion (THD) under effective switching control. IEEE 519-2014 establishes harmonic THD limits for voltage and current, providing a guideline for reliable high-quality power. Maintaining these levels is critical to increase system efficiency, reduce power losses, and improve general power quality. By minimizing the THD, not only is the inverter performance enhanced, but the system meets IEEE 519 with grid-connected applications, renewable energy systems, and industrial motor drives. Sinusoidal pulse width modulation (SPWM) is one of the most commonly used control strategies due

to its simplicity and effectiveness in generating smooth output waveforms [12], [13]. However, conventional SPWM techniques, particularly single-reference modulation, struggle to optimize THD when applied to high-level CHMIs. Previous studies have explored various methods, including multi-carrier SPWM, selective harmonic elimination (SHE), and space vector modulation (SVM), each with advantages and limitations [14]-[16]. For instance, SVM provides better harmonic reduction but involves complex computations [15], while SHE requires solving nonlinear equations, making real-time implementation challenging [16]-[17], and implementation of multi-carrier SPWM requires complex computational processing because it utilizes multiple carriers together with comparison logic [18]. Despite these advances, further improvements in THD reduction and voltage quality are needed for high-performance applications. Previous works indicate that increasing the number of levels in CHMIs improves voltage quality but also increases circuit complexity and computational demand for control techniques [10]-[11], [19]. Additionally, existing studies lack a comprehensive comparison of how a multi-sinusoidal reference in SPWM affects the performance of CHMIs across different levels.

This study presents a comparative analysis of CHMI with multi-reference sinusoidal SPWM, exploring its performance across five, seven, nine, eleven, thirteen, and fifteen levels. The key contributions of this work include: i) Proposing a modified SPWM technique that employs multiple reference sinusoidal signals instead of a single reference, enhancing voltage quality and reducing THD [20]-[23]; ii) Performing a detailed performance evaluation through MATLAB Simulink simulations to analyze how different inverter levels affect THD and waveform quality [24]; and iii) Comparing the results with conventional SPWM techniques, demonstrating that the proposed approach achieves lower THD and improved voltage profiles, making it suitable for high-power applications [11], [24], [25].

2. CIRCUIT CONFIGURATION OF CASCADED H-BRIDGE INVERTERS

The topology of the cascaded CHMI is formed by cascading H-bridge conventional inverters, as depicted in Figure 1. The switching states and output voltage VAB of the H-bridge inverter are depicted in Table 1. The level of the CHMI is determined using the formula n=2m+1, where n represents the number of levels in the inverter, m is the number of distinct DC sources, and s=2(n−1) is used to calculate the number of switches required for a given level of CHMI [25]. The comparison of component requirements for 5 to 15 levels of the cascaded H-bridge inverter is provided in Table 2. Figure 2 shows the configuration of the cascaded H-bridge inverter per phase for 5, 9, and 15 levels. The output voltage (V_{AB}) is the summation of each output from each H-bridge inverter. For a three-phase system, the output of three identical structures of single-phase CHMI can be connected in either a wye or delta configuration.

Figure 3 illustrates the schematic diagram of a wye-connected m-level CHMI with separate DC sources (vdc) for a 5-level CHMI. The line voltages are expressed in terms of two-phase voltages. For instance, the voltage between phase A and phase B, denoted as V_{AB}, is calculated using the (1):

$$V_{AB} = V_{AN} - V_{BN} \quad (1)$$

where, $V_{AB}$is the line voltage V_{AN} is the voltage of phase A with respect to the neutral point N, V_{BN} is the voltage of phase B with respect to the neutral point N.

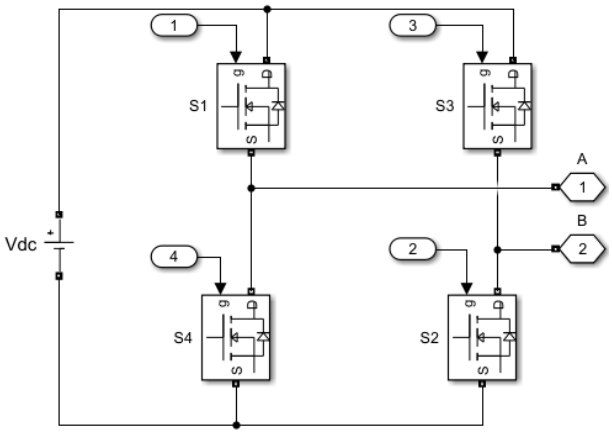

Figure 1. H-bridge conventional inverter topology and switching state (S3 and S4 are in complementary states to S1 and S2, respectively)

Table 1. Switching states and output voltage V_{AB} of the H-bridge inverter

S1	S2	S3	S4	V_{AB}
1	1	0	0	+Vdc
1	0	0	1	0
0	1	1	0	0
0	0	1	1	-Vdc

Table 2. The comparison of component requirements for 5 to 15 levels of the cascaded H-bridge inverter per phase

Levels	DC sources	No. of switches
5	2	8
7	3	12
9	4	16
11	5	20
13	6	24
15	7	28

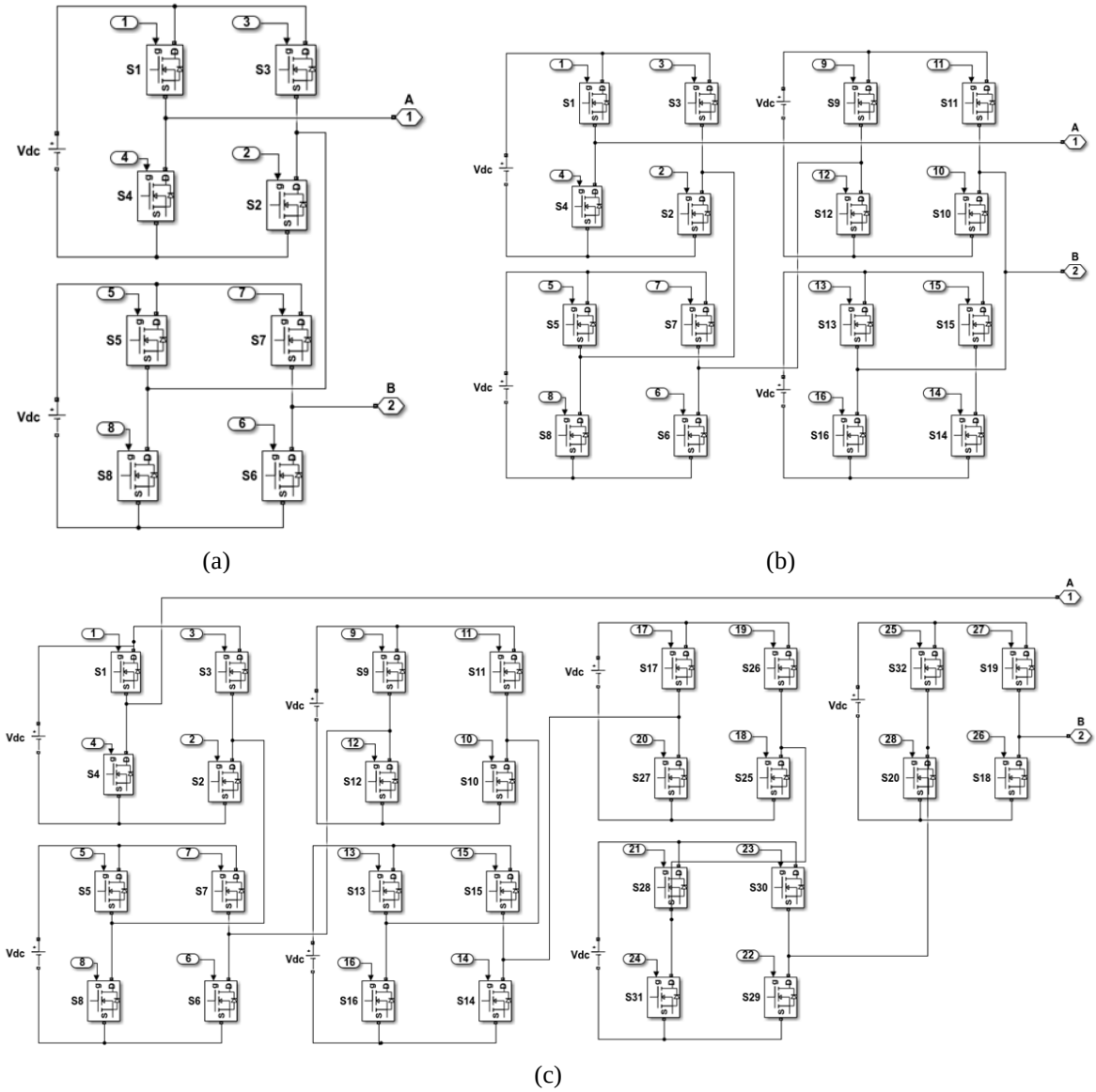

Figure 2. The configuration of the cascaded H-bridge inverter per phase for: (a) 5-level CHMI, (b) 9-level CHMI, and (c) 15-level CHMI

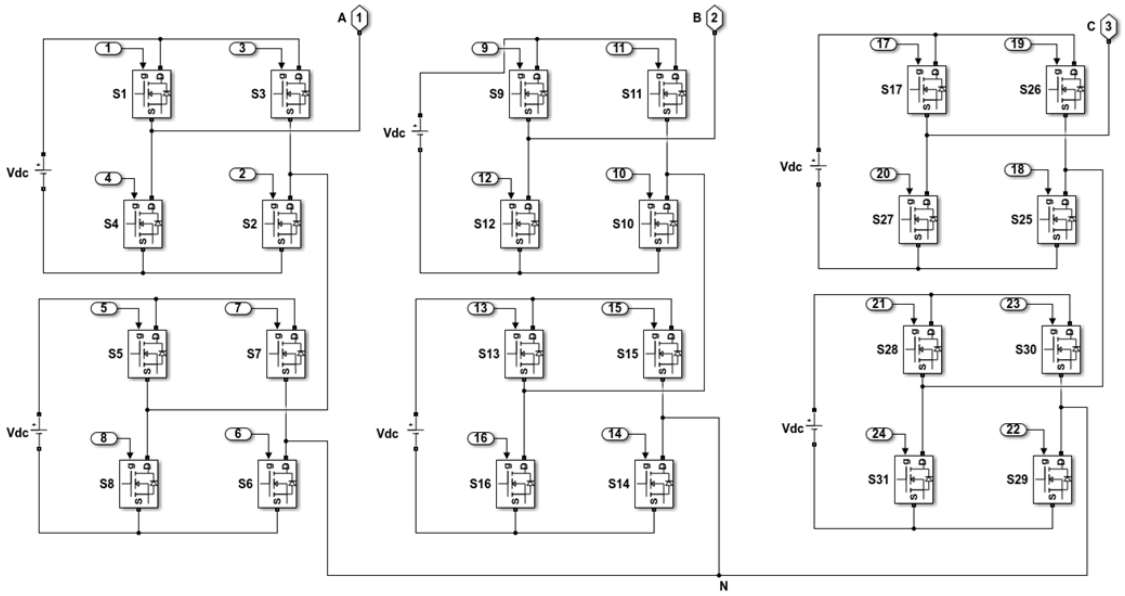

Figure 3. The configuration of the cascaded H-bridge inverter for 5-level phase A, B, and C

3. MODULATION TECHNIQUES OF CASCADED H-BRIDGE INVERTERS

Numerous researchers in the power converter technologies field have developed various modulation techniques for control strategies for multilevel inverters. The most well-known and straightforward technique is sinusoidal pulse width modulation (SPWM). The CHMI can be controlled using SPWM techniques. To obtain the multi-level output, multi-carrier wave signals are used and compared with a sinusoidal signal; the obtained compared pulses are used to switch off the inverter [22]. The technique can be categorized into level-shifted variations of Pulse Width Modulation (PWM), including phase disposition pulse width modulation (PDPWM), Phase opposite disposition pulse width modulation (PODPWM) and alternative phase opposite disposition pulse width modulation (APODPWM).

In this paper, the technique has been modified by employing multiple reference sinusoidal signals with varying amplitudes, compared with triangle/ramp waves, to generate the switching signals that control the semiconductor switches in a timed sequence. This technique employs 2(n-1)/2 reference sinusoidal to produce the n-level inverter output voltage per phase. The amplitude of the sinusoidal is obtained using the formula (n-1)/2. The summary of the comparison in terms of the number of H-bridge and sinusoidal reference signals, the amplitude, and the shift of the sinusoidal reference signals is shown in Table 3.

Table 3. The comparison of multiple reference sinusoidal signals for 5 to 15 levels for modulation

Levels	No. of H-bridge	No. of sinusoidal signals	Amplitude of a sinusoidal	Shifted amplitude
5	2	4	2	0, -1, 1, 2
7	3	6	3	0, -1, 1, -2, 2, 3
9	4	8	4	0, -1, 1, -2, 2, -3, 3, 4
11	5	10	5	0, -1, 1, -2, 2, -3, 3, -4, 4, 5
13	6	12	6	0, -1, 1, -2, 2, -3, 3, -4, 4, -5, 5, 6
15	7	14	7	0, -1, 1, -2, 2, -3, 3, -4, 4, -5, 5, -6, 6, 7

Four sinusoidal waveforms with a frequency of 50Hz and a triangular carrier waveform of 10 kHz for the 5-level CHMI are shown in Figure 4(a). The sinusoidal references, Ref 1 and Ref 2, are compared to generate PWM signals for controlling the semiconductor switches (S1 to S4) of the H-Bridge 1. Similarly, Ref 3 and Ref 4 are compared to produce the switching signals for the switches (S5 to S8) of the H-Bridge 2. Figure 4(b) presents 14 sinusoidal waveforms with a frequency of 50 Hz, having shifted amplitudes (refer to Table 3), along with a triangular carrier waveform of 10 kHz, used to generate PWM for the 15-level CHMI. Figure 5 illustrates the PWM signals for switches S1 through S8, where the PWM signals for S3, S4, S7, and S8 are complementary to those of S2, S1, S6, and S5, respectively.

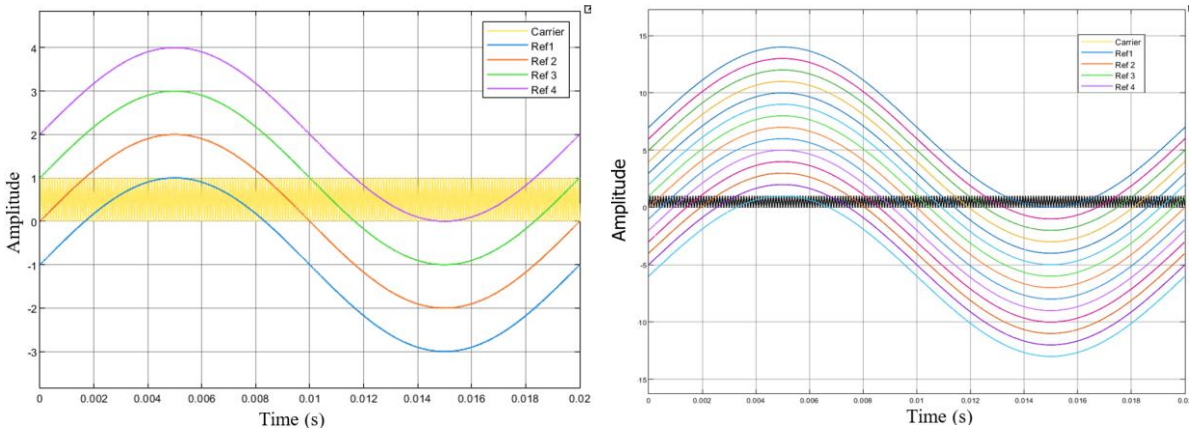

Figure 4. The sinusoidal waveforms with a frequency of 50 Hz and a carrier of 5 kHz for (a) 5-level and (b) 15-level CHMI

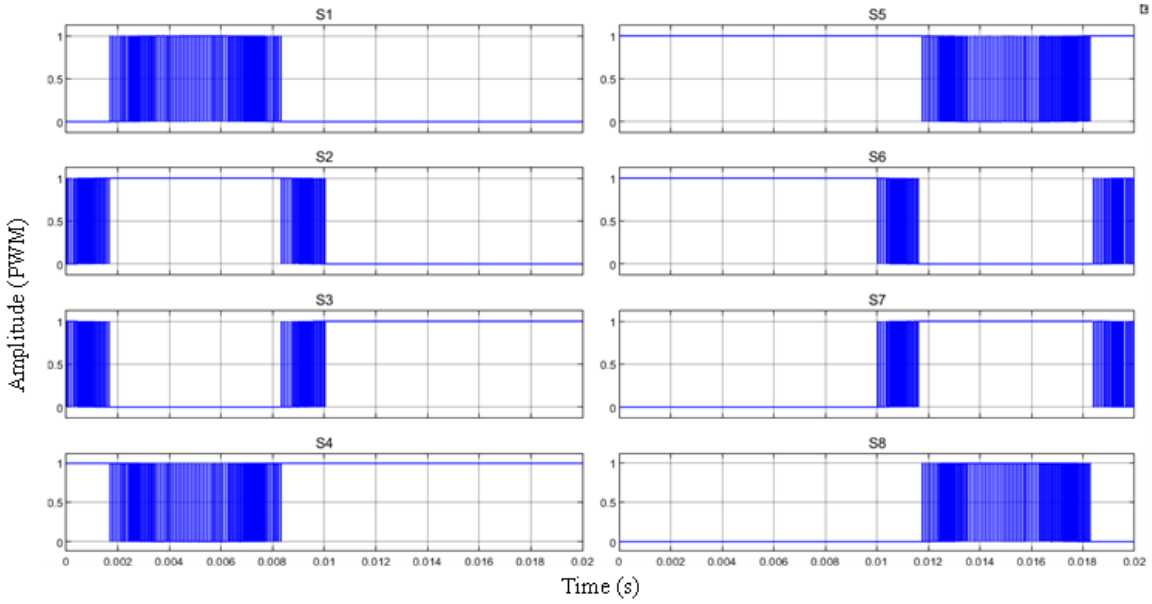

Figure 5. The PWM of S1 to S8 for 5-level CHMI

Table 4 shows the phase output levels for a 5-level CHMI across a full cycle. The switching states of S1 to S4 determine the output for H-Bridge 1, which can be -Vdc, 0, or +Vdc. Similarly, the states of S5 to S8 control the output for H-Bridge 2, which also varies between -Vdc, 0, and +Vdc. The overall phase output is the sum of the outputs from both H-Bridges, resulting in multiple voltage levels: ±2 Vdc, ±Vdc, and 0, in a specific sequence.

Table 4. The phase output level (V_{AN}) for 5-level CHMI (full cycle)

S1	S2	S3	S4	Output (H-Bridge 1)	S5	S6	S7	S8	Output (H-Bridge 2)	Total Phase Output ($\boldsymbol{V_{AN}}$) 5-level CHMI
0	0↔1	1↔0	1	-Vdc ↔ 0	1	1	0	0	+Vdc	0↔+Vdc
0↔1	1	0	1↔0	0↔+Vdc	1	1	0	0	+Vdc	+Vdc↔+2Vdc
0	0↔1	1↔0	1	0 ↔ -Vdc	1	1	0	0	+Vdc	+Vdc↔0
0	0	1	1	-Vdc	1	0↔1	0↔1	0	+Vdc↔0	0↔-Vdc
0	0	1	1	-Vdc	0↔1	0	1	0↔1	0 ↔ -Vdc	-Vdc ↔-2Vdc
0	0	1	1	-Vdc	1	0↔1	0↔1	0	+Vdc↔0	+Vdc↔0

This concept is extended to higher levels of CHMI, including 7, 9, 11, 13, and 15 levels. Table 5 presents the switching states of S1 to S28, determined by comparing a triangular carrier waveform with 14 sinusoidal waveforms. These states consist of 0, 1, and PWM (1↔0) over half a cycle. The outcome of this switching process is summarized in Table 6. The combined phase output from all seven cascaded H-Bridges produces multiple voltage levels: ±7 Vdc, ±6 Vdc, ±5 Vdc, ±4 Vdc, ±3 Vdc, ±2 Vdc, ±Vdc, and 0, following a specific sequence for a full cycle.

Table 5. The output level for the 15-level CHMI (half cycle)

State	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	T17	T18	T19	T20
S1	0	0↔1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0↔1	0
S2	0↔1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0↔1
S3	1↔0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1↔0
S4	1	1↔0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1↔0	1
S5	0	0	0↔1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0↔1	0	0
S6	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S8	1	1	1↔0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1↔0	1	1
S9	0	0	0	0↔1	1	1	1	1	1	1	1	1	1	1	1	1	0↔1	0	0	0
S10	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S11	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S12	1	1	1	1↔0	0	0	0	0	0	0	0	0	0	0	0	0	1↔0	1	1	1
S13	0	0	0	0	0↔1	1	1	1	1	1	1	1	1	1	1	0↔1	0	0	0	0
S14	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S15	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S16	1	1	1	1	1↔0	0	0	0	0	0	0	0	0	0	0	1↔0	1	1	1	1
S17	0	0	0	0	0	0↔1	0↔1	1	1	1	1	1	1	0↔1	0↔1	0	0	0	0	0
S18	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S19	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S20	1	1	1	1	1	1↔0	1↔0	0	0	0	0	0	0	1↔0	1↔0	1	1	1	1	1
S21	0	0	0	0	0	0	0	0↔1	0↔1	0↔1	0↔1	0↔1	0↔1	0	0	0	0	0	0	0
S22	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S23	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S24	1	1	1	1	1	1	1	1↔0	1↔0	1↔0	1↔0	1↔0	1↔0	1	1	1	1	1	1	1
S25	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S26	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
S27	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
S28	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6. The output level for the 15-level CHMI (half cycle)

Output H-Bridge 1 (S1-S4)	Output H-Bridge 2 (S5-S8)	Output H-Bridge 3 (S9-S12)	Output H-Bridge 4 (S13-S16)	Output H-Bridge 5 (S17-S20)	Output H-Bridge 6 (S21-S24)	Output H-Bridge 7 (S25-S28)	Total phase output 15-level CHMI
-Vdc ↔ 0	0	0	0	0	0	+Vdc	0↔ +Vdc
0↔ +Vdc	0	0	0	0	0	+Vdc	+Vdc↔ +2Vdc
+Vdc	0↔ +Vdc	0	0	0	0	+Vdc	+2Vdc↔ +3Vdc
+Vdc	+Vdc	0↔ +Vdc	0	0	0	+Vdc	+3Vdc↔ +4Vdc
+Vdc	+Vdc	+Vdc	0↔ +Vdc	0	0	+Vdc	+4Vdc↔ +5Vdc
+Vdc	+Vdc	+Vdc	+Vdc	0↔ +Vdc	0	+Vdc	+5Vdc↔ +6Vdc
+Vdc	+Vdc	+Vdc	+Vdc	0↔ +Vdc	0	+Vdc	+5Vdc↔ +6Vdc
+Vdc	+Vdc	+Vdc	+Vdc	+Vdc	0↔ +Vdc	+Vdc	+6Vdc↔ +7Vdc
+Vdc	+Vdc	+Vdc	+Vdc	+Vdc	0↔ +Vdc	+Vdc	+6Vdc↔ +7Vdc
+Vdc	+Vdc	+Vdc	+Vdc	+Vdc	0↔ +Vdc	+Vdc	+6Vdc↔ +7Vdc
+Vdc	+Vdc	+Vdc	+Vdc	+Vdc	0↔ +Vdc	+Vdc	+6Vdc↔ +7Vdc
+Vdc	+Vdc	+Vdc	+Vdc	+Vdc	0↔ +Vdc	+Vdc	+6Vdc↔ +7Vdc
+Vdc	+Vdc	+Vdc	+Vdc	+Vdc	0↔ +Vdc	+Vdc	+6Vdc↔ +7Vdc
+Vdc	+Vdc	+Vdc	+Vdc	0↔ +Vdc	0	+Vdc	+6Vdc↔ +5Vdc
+Vdc	+Vdc	+Vdc	+Vdc	0↔ +Vdc	0	+Vdc	+6Vdc↔ +5Vdc
+Vdc	+Vdc	+Vdc	0↔ +Vdc	0	0	+Vdc	+5Vdc↔ +4Vdc
+Vdc	+Vdc	0↔ +Vdc	0	0	0	+Vdc	+4Vdc↔ +3Vdc
+Vdc	0↔ +Vdc	0	0	0	0	+Vdc	+3Vdc↔ +2Vdc
0↔ +Vdc	0	0	0	0	0	+Vdc	+2Vdc↔ +Vdc
-Vdc ↔ 0	0	0	0	0	0	+Vdc	+Vdc↔ 0

4. RESULTS AND DISCUSSION

The three-phase cascaded H-bridge inverter (5, 7, 9, 11, 13, and 15 levels) is simulated in MATLAB/Simulink using the proposed SPWM. Each DC source is set to 1500 V, the load is 1 Ω per phase, and the modulation index is 1 for all cases. Figure 6 presents the phase-A outputs for the higher-level CHMIs; the maximum phase voltages are 4500 V, 6000 V, 7500 V, 9000 V, and 10 500 V for the 7-levels.

9-levels, 11-levels, 13-levels, and 15-levels cases, respectively, showing the progressive increase in output as the number of levels rises. Figure 7 shows the three-phase (A, B, C) output of the 5-level CHMI, confirming the discrete levels of ±3000 V, ±1500 V, and 0 V consistent with Table 3. These results follow the linear scaling Vphase max = N×1500 V for N cascaded cells with equal DC sources. As the level count increases, the step size decreases and the phase waveform becomes more sinusoidal, which helps reduce low-order harmonics and filter requirements.

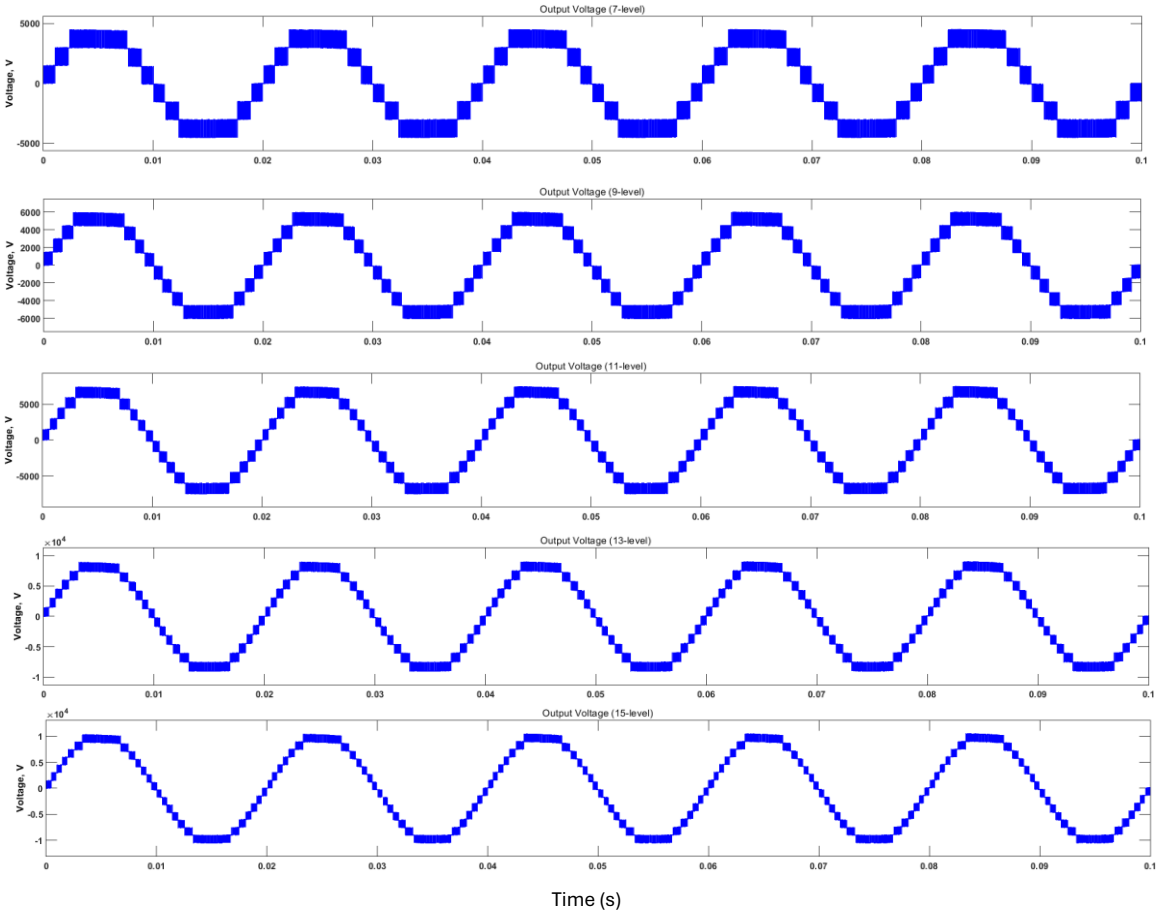

Figure 6. The phase output voltage for 7, 9, 11, 13, and 15-levels CHMI in Phase A

To validate the effectiveness of the proposed SPWM technique, the THD values obtained from the simulations are compared with the IEEE 519-2014 standard. According to IEEE 519, voltage THD should not exceed 5% for systems below 69 kV. Figure 8(a) shows the phase-voltage spectrum of the 5-level CHMI at a modulation index of 1, where prominent low-order odd harmonics (3rd, 5th, 7th) yield a THD of 26.98%. Figure 8(b) presents the corresponding spectrum for the 15-level CHMI, in which the low-order components are markedly suppressed and the THD reduces to 8.02%. These spectra illustrate the progressive reduction in distortion as the number of levels increases. The lower THD at a higher number of levels also means smaller filters, reduced losses, and improved voltage profiles in practice.

The Phase-A line voltage for the 5, 7, 9, 11, 13, and 15-levels cascaded H-bridge multilevel inverter (CHMI) configurations is shown in Figure 9. It highlights how increasing the number of levels improves waveform quality, voltage stability, and reduces total harmonic distortion (THD). As the number of levels increases, the output voltage becomes smoother and more sinusoidal, resulting in lower distortion and better power quality. The voltage profile also aligns with IEEE 519-2014 standards, which define acceptable THD limits for maintaining power quality. The results confirm that higher-level CHMIs are more effective in delivering clean and stable voltage output, making them a great choice for applications like renewable energy systems, industrial motor drives, and grid-connected power electronics. The 15-level CHMI, in particular, stands out for its minimal distortion, reducing the need for extensive filtering and improving overall system efficiency.

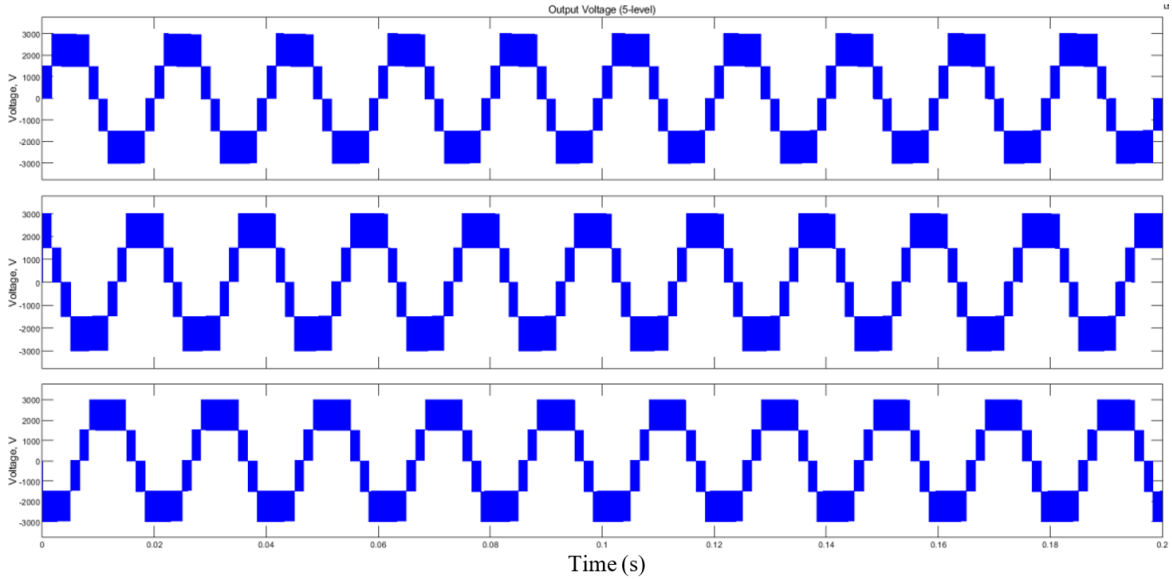

Figure 7. The phase output voltage for 5-level CHMI in Phase A (upper), B (middle), and C (lower)

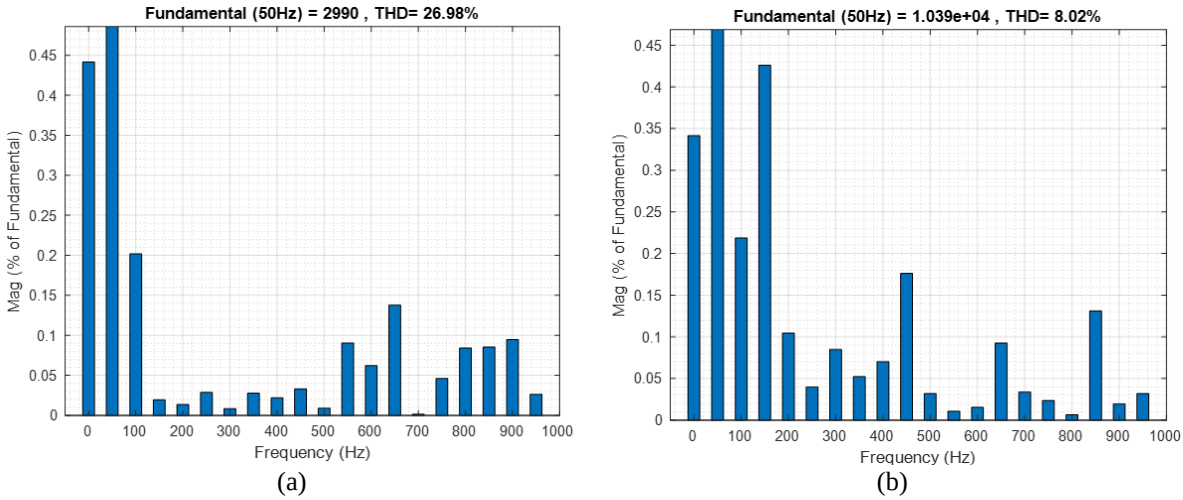

Figure 8. THD analysis (modulation index 1) of (a) 5-level CHMI and (b) 15-level CHMI

Table 7 presents the obtained results of levels of the maximum voltage, and the %THD for both line and phase voltages for the 5, 7, 9, 11, 13, and 15-levels CHMI with modulation index change in phase voltage. As the modulation index and the number of levels increase, phase-voltage %THD decreases, while the maximum phase voltage rises in 1,500 V steps. A similar trend appears for line voltages, where higher modulation index and more levels both reduce line-voltage %THD as presented in Table 8. Notably, line-voltage %THD is consistently lower than the corresponding phase-voltage THD at comparable conditions because the line-to-line subtraction cancels part of the harmonic content. From the simulation results discussed above, it follows that an increase in the number of levels of the considered CHMI leads to greater immunity of the output voltage quality to harmonic distortion deficiencies. The higher-level configuration is thus more appropriate for applications requiring good quality power and little interference. THD reduction is a testament to the closer sine waveforms attainable in the output voltages of higher-level inverters, thereby enhancing power quality and efficiency. In order to study the performance of these set-ups, the results must also be compared to the IEEE 519-2014 normative standards, which have set limits for acceptable THD values for power quality. For full IEEE 519-2014 compliance (THD $\leq$ 5%), it is possible to utilize small passive filters (LC or LCL) in small-sized (13-level and 15-level) CHMIs. CRHMI is the most compact of standards-compliant HMIs, and minimum filtering should render it a compliant design.

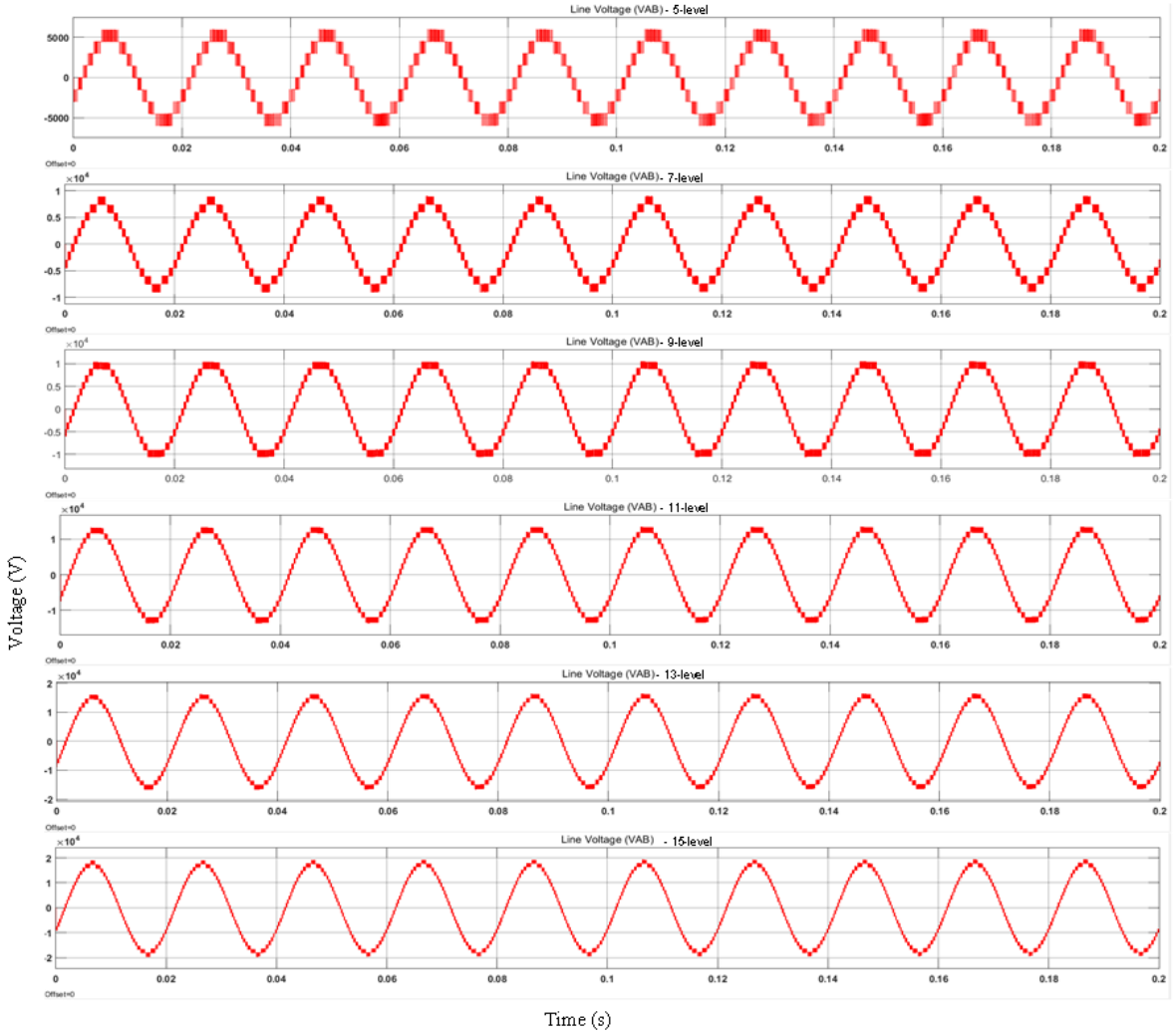

Figure 9. The line output voltage for 5, 7, 9, 11, 13, and 15-levels CHMI in phase A

Table 7. Variation modulation index, level, maximum voltage, and %THD of phase voltage for 5, 7, 9, 11, 13, and 15-levels CHMI

Modulation index	Levels CHMI	No. of level	Max. phase output voltage (V)	%THD	Levels CHMI	No. of level	Max. phase output voltage (V)	%THD	Levels CHMI	No. of level	Max. phase output voltage (V)	%THD
0.2	5-level	3	1500	148.22	7-level	3	1500	109.46	9-level	3	1500	79.19
0.3		3	1500	106.51		3	1500	66.31		5	3000	44.68
0.4		3	1500	77.07		5	3000	44.68		5	3000	38.79
0.5		3	1500	52.22		5	3000	40.69		5	3000	27.44
0.6		5	3000	44.45		7	3000	34.04		7	4500	24.47
0.7		5	3000	41.79		7	4500	25.35		7	4500	21.57
0.8		5	3000	38.4		7	4500	24.46		9	6000	17.25
0.9		5	3000	33.56		7	4500	22.65		9	6000	16.85
1.0		5	3000	26.98		7	4500	18.44		9	6000	13.89
0.2	11-level	3	1500	54.15	13-Level	5	3000	44.7	15-level	5	3000	42.23
0.3		5	3000	40.7		5	3000	34.06		5	3000	25.37
0.4		5	3000	27.44		7	4500	24.48		7	4500	21.58
0.5		7	4500	24.08		7	4500	18.46		9	6000	17.09
0.6		7	4500	18.46		9	6000	16.86		11	7500	13.2
0.7		9	6000	17.08		11	7500	13.2		11	7500	11.9
0.8		9	6000	13.9		11	7500	12.46		13	9000	10.72
0.9		11	7500	13.19		13	9000	10.78		15	10500	9.08
1.0		11	7500	11.17		13	9000	9.38		15	10500	8.02

Table 8. Variation modulation index, level, maximum voltage, and %THD of line voltage for 5, 7, 9, 11, 13, and 15-levels CHMI

Modulation index	Levels CHMI	No. of level	Max. phase output voltage (V)	%THD	Levels CHMI	No. of level	Max. phase output voltage (V)	%THD	Levels CHMI	No. of level	Max. phase output voltage (V)	%THD
0.2	5-level	3	1500	92.13	7-level	5	3000	52.88	9-level	5	3000	41.95
0.3		5	3000	49.76		5	3000	38.98		7	4500	26.4
0.4		5	3000	42.17		7	4500	26.39		7	4500	21.58
0.5		5	3000	35.29		7	4500	23.22		9	6000	17.18
0.6		7	4500	25.65		9	6000	17.77		11	7500	13.28
0.7		7	4500	24.18		9	6000	16.54		11	7500	12.12
0.8		7	4500	21.68		11	7500	13.28		13	9000	10.83
0.9		9	6000	17.4		11	7500	12.8		15	10500	9.04
1.0		9	6000	17.1		13	9000	10.69		15	10500	8.3
0.2	11-level	5	3000	36.01	13-level	7	4500	26.41	15-level	7	4500	24.23
0.3		7	4500	23.23		9	6000	17.78		9	6000	16.55
0.4		9	6000	17.18		11	7500	13.29		11	7500	12.13
0.5		11	7500	13.51		13	9000	10.69		15	10500	9.04
0.6		13	9000	10.69		15	10500	9.05		17	12000	7.78
0.7		15	10500	9.04		17	12000	7.78		19	13500	6.9
0.8		15	10500	8.3		19	13500	6.86		21	15000	6.11
0.9		17	12000	7.56		21	15000	6.19		23	16500	5.24
1.0		19	13500	6.87		23	16500	5.58		25	18000	4.59

5. CONCLUSION

This study examined cascaded CHMI using SPWM with multi-sinusoidal reference and found that increasing the number of levels helps improve waveform quality and significantly reduce THD. While the 15-levels CHMI performs much better than lower-level designs, with a THD of 8.02%, it still slightly exceeds the IEEE 519-2014 limit of 5%. To fully meet this standard, small passive filters (LC/LCL) can be added. Overall, higher-level CHMIs (13-levels and 15-levels) prove to be a better choice for applications requiring cleaner power, such as renewable energy, motor drives, and grid-connected systems. Future work can explore passive filtering, advanced modulation techniques, and real-world testing to further improve performance.

ACKNOWLEDGMENTS

The authors wish to express their gratitude to the Universiti Teknikal Malaysia Melaka (UTeM), Fakulti Teknologi dan Kejuruteraan Elektrik (FTKE), Centre of Robotic and Industrial Automation (CERIA), and Centre of Research and Innovation Management (CRIM).

FUNDING INFORMATION

This research was financially supported by the Centre of Research and Innovation Management (CRIM), Universiti Teknikal Malaysia Melaka (UTeM), which covered the article processing fee.

AUTHOR CONTRIBUTIONS STATEMENT

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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper. Authors state no conflict of interest.

DATA AVAILABILITY

Data availability is not applicable to this paper as no new data were created or analyzed in this study.

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