

# DC bus control strategy and implications for voltage source converter system

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## ABSTRACT

Significantly, the use of power electronic devices in residential and industrial settings has grown significantly in the last several years. Recent advancements in power semiconductors and microelectronics may be the main reason of their growing use in power systems for filtering, conditioning, and compensating. Additionally, the proliferation of semiconductor switches appropriate for high-power applications, and the enhancement of microelectronics enable mixed signal processing and control mechanisms. Furthermore, the concentration on renewable energy sources within the electric utility industry has emphasized the incorporation of power electronic converters into power systems. The operation and control of the regulated DC-voltage power port are examined in this work, a key part in different applications, such as STATCOM, dual mode HVDC converter systems, and aerodynamic wind energy converters with adaptive-speed optimization, emphasizing its significance in upholding a stable voltage level throughout the DC bus. The research also highlights the importance of power electronic converters within contemporary power systems, emphasizing their crucial role in facilitating effective and reliable power distribution. The obtained simulation results confirmed the efficacy of feed-forward compensation in stabilizing the voltage responses of the DC bus.

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## NOMENCLATURE

HVDC	: High voltage direct current	PLL	: Phase-locked loop
STATCOM	: Static synchronous compensator	$\tau_i$	: Time constant of closed loop system
VSC	: Voltage source converter	Gp(s)	: Transfer function
PCC	: Point of common coupling	Ky(s)	: Compensator in a control system
VDC	: Voltage of the DC bus	Vsabc	: Three-phase AC voltage
VDC2	: Squared value of DC voltage	Ps	: Real power component
Vta, Vtb, Vtc	: AC voltages at the inverter terminal	Vsa, Vsb, Vsc	: AC-side voltage source
Qs	: Reactive power component	Pt	: Power at the inverter AC side
Ps-ref	: Real power reference value	Ppc	: Instantaneous DC power
Id	: Direct current component in the dq-frame	Pext0	: Steady-state external power exchange
Pext	: External power exchange	Qs-ref	: Reactive power reference value
PLOSS	: Power loss	mabe	: Modulating signal in PWM

$\tau$	: Time constant related to the overall dynamics of the system	maug-a, maug- b, maug-c	: PWM signals in the dq-abc frame
VCO	: Voltage-controlled oscillator		

## 1. INTRODUCTION

Throughout the course of their history, power electronic converters have been used most often in applications that are either household, industrial, or related to information technology. Despite this, the use of power semiconductors and microelectronics in power systems has received a great deal of attention in the last two decades as a result of technological improvements in power semiconductors and microelectronics. Therefore, converters for power electronics are becoming a gradually common component in applications involving conditioning systems, remuneration, and filtering of power [1]-[4].

An electronic power converter comprises a control and protection system in addition to a power circuit. The power circuit can be achieved by any one of a number of different configurations of power switches and passive components. Signals for gating and switching as well as feedback control signals, provide the connection between the two [5]-[7].

For an extended period, the utilization of high-power converters in electrical power grids was primarily restricted to high-voltage direct current (HVDC) transmission systems, with only marginal implementation in typical static VAR compensators (SVC) and the synchronous machine electronic excitation systems. This situation lasted for a considerable amount of time [4]. Despite this, since the end of the 1980s, there has been an upward trend in interest in the applications in electrical power systems for the production, distribution, transmission, and transport of electric power [1]-[6]. The primary explanations are:

- Recent and ongoing advances in technology for electrical systems, as well as the accessibility of a wide variety of switches created from semiconductors suited for use in applications of high power.
- The moving forward development of technology for microelectronics has made it possible to implement complex signal processing and control techniques, as well as the algorithms necessary for such strategies, in a variety of contexts and context-specific applications.
- The electric utility sector is undergoing restructuring, which necessitates the use of power electronics-based technology to solve issues like power line congestion.
- The ongoing expansion of energy demand has led to the use of the electric power utility infrastructure that is very near to reaching its maximum capacity, which necessitates the use of electronic power equipment in order to improve the system's stability.
- The trend toward increased usage of green energy is a response to the phenomena of global warming as well as environmental problems linked with centralized power generation. Because of recent developments in technology, this movement has gained traction, which has led to the commercial and technological feasibility of alternative sources of energy, especially those that are renewable. Specifically, this viability has resulted in the viability of renewable energy resources. Power electronic converters are frequently used to establish a connection between these types of energy resources and the electric power system [8]-[10].

The direct current side of the voltage source converter (VSC) is linked to an ideal direct current voltage source, which is responsible for dictating the voltage of the direct current bus. As a result, the system of VSC serves as a channel for the flow of power in both directions, connecting the AC system and the DC voltage source. But in a lot of situations, such as fuel-cell and photovoltaic (PV) systems, this is not the case. The DC side of the VSC is not interfaced with a voltage source; rather, it is coupled to a DC power source. Before the AC system can utilize this power, a controlled energy exchange and precise regulation must be implemented to ensure seamless integration and operational stability [11]-[16].

The purpose of this study is to enhance the stability of the regulated DC-voltage power port using an optimized feed-forward compensation approach. The introduction of this work outlines the significance of power electronic converters and the challenges in DC bus voltage regulation. The paper is structured systematically: i) Section 1 provides an introduction; ii) Section 2 presents the system structure; iii) Section 3 details the mathematical modelling; iv) Section 4 discusses the control strategy; v) Section 5 introduces third harmonic injection for improved PWM performance; and vi) Section 6 validates the approach through simulation results.

## 2. SYSTEM STRUCTURE

Figure 1 illustrates the VSC system, and the source of DC voltage is represented as a (varying) DC power source in this instance. Typically, the source of power is represented by a unit of power electronics that has the main energy source that powers it. In particular, this may be a fuel cell unit, a gas turbine-

generator system, a variable-speed wind turbine-generator system, or an array of solar panels. We tackle this as a black box and make the assumption that it trades a power supply with the DC side of the VSC that varies over time. Because of this, the VSC system shown in Figure 1 permits a power exchange in both directions between the power supply and the alternating current AC system. For the rest of this discussion, we are going to talk about the VSC system shown in Figure 1 as the DC-voltage power port which regulates. The regulated DC-voltage power port is crucial in the STATCOM, the components of variable-speed wind power, and the back-to-back HVDC converter system [17]-[19].

As seen in Figure 1, the VSC is approximated by a CPU with lossless power that contains an analogous DC-bus capacitor, a current source that represents the loss of VSC switching power, and the AC side's series on-state resistance that represents the VSC conduction power loss. The VSC's DC side can be connected to either a DC voltage or a DC power source. A series RL branch connects each VSC phase to the AC system.

In this paper, we will be approximating an endlessly stiff AC system in order to better understand it. As a result, the AC system may be conceptualized as a representation of the optimal three-phase power supply, denoted by  $V_{sabc}$ . In addition to this, it is presumed that  $V_{sabc}$  is symmetrical, sinusoidal, and has a frequency that is generally stable. At the point of common connection, the real and reactive power components  $P_s(t)$  and  $Q_s(t)$  are traded between the AC system and the VSC system. Figure 1 shows this process point of common coupling (PCC) [16].

Where  $V_{ta}$ ,  $V_{tb}$ , and  $V_{tc}$  are the AC voltages at the inverter terminal.  $V_{sa}$ ,  $V_{sb}$ , and  $V_{sc}$  are the AC-side voltages source.  $P_{DC}$  is the instantaneous power at the DC side,  $P_t$  is the electrical power at the AC side of the inverter, and  $P_s$  is power supplied to the voltage source on the AC side.  $P_{ext}$  is the varying-time power exchange between the power source and DC side VSC, and  $P_{loss} = V_{DC} \times i_{loss}$ .

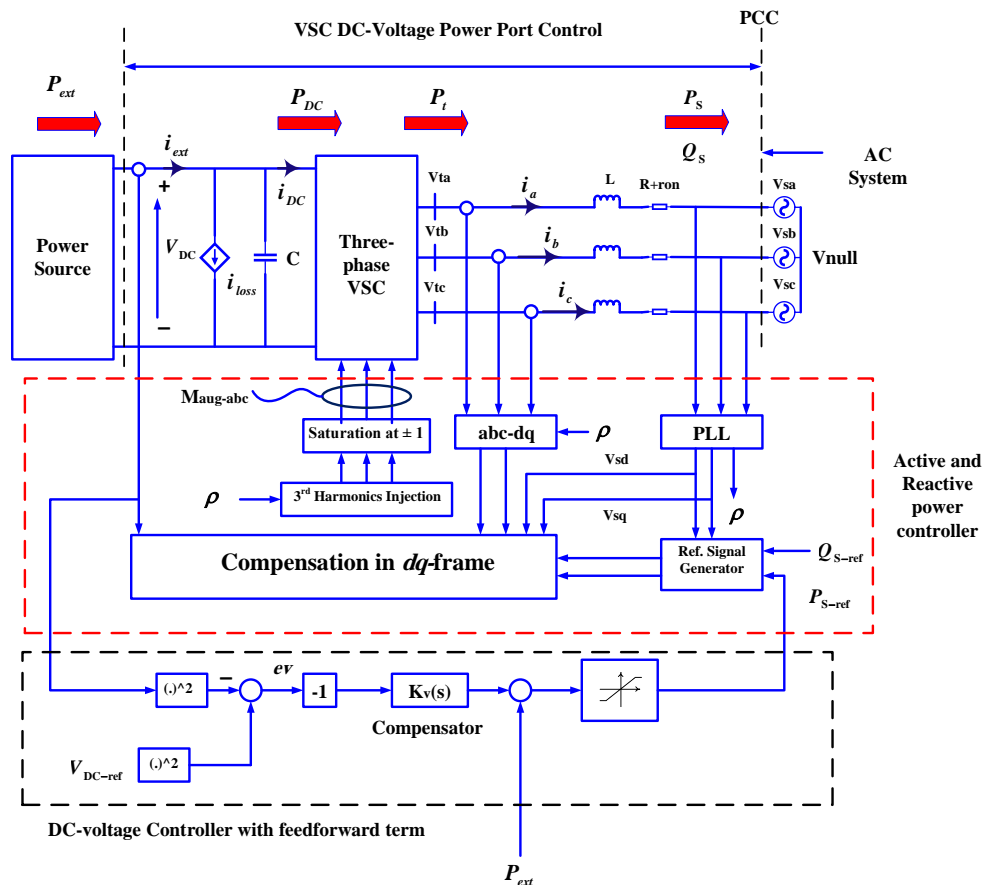


Figure 1. A diagrammatic representation of the regulated DC-voltage power port

The primary control goal of the regulated DC-voltage power outlet is to maintain a consistent voltage across the DC bus (denoted by  $V_{DC}$ ). The power port with controlled DC voltage is depicted in Figure 1, as can be seen. A feedback mechanism, therefore, compares the voltage of the DC bus  $V_{DC}$  with its reference

command in order to control the voltage of the DC bus. According to the results of this comparison,  $P_s$  is adjusted in such a way that the net power that is exchanged with the DC-bus capacitor is maintained at zero. On the other hand, the reactive power  $Q_s$  can be modified on an individual basis. In a great number of applications,  $Q_s$  is controlled to remain at zero; in these cases, the VSC system maintains a power factor of unity. It is possible to control PCC voltage by  $Q_s$  being adjusted in a closed-loop manner [14]-[18].

### 3. MODELLING OF CONTROLLED POWER PORT WITH REGULATED DC-VOLTAGE

The main control needs for the regulated DC-voltage power port shown in Figure 1 is to regulate the voltage of the DC bus, which is denoted by  $VDC$ . To put it another way, it is preferred to regulate  $VDC^2$  as opposed to  $VDC$ . Using (1) as a starting point, the dynamics of  $VDC^2$  are characterized as (1).

$$\frac{dVDC^2}{dt} = \frac{2}{c}P_{ext} - \frac{2}{c}P_{loss} - \frac{2}{c}\left[P_s + \left(\frac{2LP_s}{3\bar{V}_s^2}\right)\frac{dP_s}{dt}\right] + \frac{2}{c}\left[\left(\frac{2LQ_s}{3\bar{V}_s^2}\right)\frac{dQ_s}{dt}\right] \quad (1)$$

According to the combined dynamic model of the two-level VSC in (1),  $VDC^2$  is the output;  $P_s$  is the control input;  $P_{ext}$ ,  $P_{loss}$ , and  $Q_s$  are the disturbance inputs; and  $P_{ext}$  is the input that controls the gain. In accordance with what is depicted in Figure 1,  $VDC^2$  is compared to  $VDC_{ref}^2$ . The signal of error is dealt with by the compensator  $Kv(s)$ , and the order  $P_{s-ref}$  is sent to the controller of the real power. In its turn, the real-power controller is responsible for regulating  $P_s$  at  $P_{s-ref}$ , whereas  $Q_s$  is open to independent regulation. If there is a requirement for a controlled bidirectional regulation of reactive power interaction with the AC system,  $Q_{s-ref}$  can be adjusted to a value that is not zero. In an alternating current (AC) system with a high impedance, the PCC voltage is prone to fluctuations due to the time-dependent shifts in  $P_s$  (i.e., due to the changes of  $P_{ext}$ ). In a closed-loop system that supplies the PCC voltage back,  $Q_s$  is controlled and commands  $Q_{s-ref}$  is one way in which the voltage of the PCC may be managed in this instance [17]-[25].

In order to obtain the transfer function  $Gp(s) = P_s(s)/P_{s-ref}(s)$ , we first need to make the observation that as (2).

$$Id(s) = G_i(s) Id_{ref}(s) \quad (2)$$

In which  $G_i(s)$  is provided by (3).

$$G_i(s) = \frac{1}{\tau_i s + 1} \quad (3)$$

Where  $\tau_i$  represents the final closed-loop system's time constant. When we assume that  $Vsd$  remains unchanged, and multiply both sides of (2) by  $(3/2)Vsd$ , we get the result as (4).

$$P_s(s) = G_i(s) P_{s-ref}(s) \quad (4)$$

As a result,  $Gp(s) = G_i(s)$ , and taking into account (3), it obtains (5).

$$\frac{P_s(s)}{P_{s-ref}(s)} = G_p(s) = \frac{1}{\tau_i s + 1} \quad (5)$$

Because in  $dq$ -frame, actual power is directly proportional to  $id$ , the form (5) is the one that one would intuitively expect to see. Because of the  $P_s dP_s/dt$  and  $Q_s dQ_s/dt$  factors, the control plant that is described by (1) is a nonlinear system. The plant that has been linearized is given by (6).

$$\frac{d\widetilde{Vdc}^2}{dt} = \frac{2}{c}\widetilde{P}_{ext} - \frac{2}{c}\left[\widetilde{P}_s + \left(\frac{2LP_{s0}}{3V_{sd}^2}\right)\frac{d\widetilde{P}_s}{dt}\right] + \frac{2}{c}\left[\left(\frac{2LQ_s}{3V_{sd}^2}\right)\frac{d\widetilde{Q}_s}{dt}\right] \quad (6)$$

Where the superscripts  $\sim$  and 0 refer, respectively, to the values of the variables during steady-state circumstances and small-signal disturbances. After applying the Laplace transform to (6), we were able to derive the transfer function  $Gv(s)$  as  $\widetilde{Vdc}^2/\widetilde{P}_s$  using (7).

$$G_v(s) = \frac{\widetilde{Vdc}^2}{\widetilde{P}_s} = -\left(\frac{2}{c}\right)\frac{\tau s + 1}{s} \quad (7)$$

Where the constant of the time  $\tau$  is as (8).

$$\tau = \frac{2LP_{s0}}{3V_{sd}^2} = \frac{2LP_{ext0}}{3V_{sd}^2} \quad (8)$$

According to the solution of (8), the value of the time constant  $\tau$  is proportional to the real power flow in a steady condition  $P_{ext0}$  (or  $P_{s0}$ ). Therefore, if  $P_{ext0}$  is low, then it will be negligible, and this will indicate that the plant is mostly an integrator. As the value of  $P_{ext}$  goes up, the value of the time constant goes up as well, which induces a phase change in  $Gv(s)$ . When the device is operating in its inverting mode,  $P_{ext0}$  has a positive value, thus also has a positive value and contributes to the phase of  $Gv(s)$ . In contrast, when the rectification operating mode is engaged—that is, when  $P_{ext0}$  is less than zero—the value of is also less than zero, which causes a decrement in the phase of  $Gv(s)$ . The phase decreases even further as the absolute value of  $P_{ext0}$  increases. The plant zero may be calculated using the formula  $z = -1/\tau$ , which can be found in (7). As a result, a negative value of is equivalent to the value zero on the right-half plane (RHP). As a direct consequence of this, the regulated DC-voltage power port is a non-minimum-phase system while it is operating in the rectifying mode [24]-[27].

#### 4. CONTROL OF A POWER PORT WITH A CONTROLLED DC VOLTAGE

Figure 2 shows a block layout of the DC-bus voltage controller used for the DC-voltage power port that is regulated in Figure 1. The compensator  $K_v(s)$ , controller pf the real power  $G_p(s)$ , and control plant  $G_v(s)$  comprise the closed-loop system, as defined by (7). Figures 1 and 2 show that in order to offset the negative sign of  $G_v(s)$ ,  $K_v(s)$  is multiplied by 1.  $K_v(s)$  should comprise a lead function of transfer with an integral term. The lead transfer function adjusts for plant phase lag and maintains an adequate phase margin at the frequency of the gain crossover.  $G_v(s)$  has the greatest phase lag when  $P_{ext}$  is at on rated negative value, according to (7) and (8). The closed-loop system remains stable at all other working points if a significant phase margin is supplied at this particular point [28]-[32].

In order to design  $K_v(s)$ , choosing the gain crossover of  $\omega_c$  to be sufficiently less than the amount of bandwidth of  $G_p(s)$ , such that  $G_p(j\omega_c) = 1 + 0j$ . Then,  $K_v(s)$  is calculated to have a sufficiently wide phase margin in the most severe operational conditions. The frequency response design approach was employed. The reason for this, according to the  $\alpha\beta$ -frame control,  $G_p(s)$  is often a high-order transfer function that is mostly determined by its bandwidth in contrast to its pole/zero map.  $G_p(s)$  (as provided by (5)) is a first-order transfer function in this case, and the root-locus design technique is also an alternative. The benefit of the root-locus technique is that performance metrics such as the settling time and maximum overshoot are more easily tied to the pole/zero loci and may be easily considered into account in the design process [25]-[33].

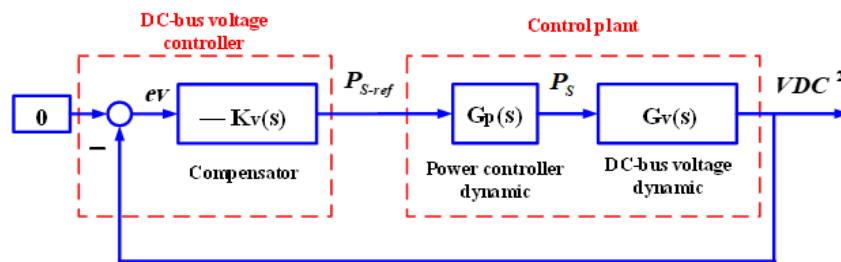


Figure 2. The DC voltage controller block diagram

#### 5. THIRD HARMONIC INJECTION FOR PWM

The third-harmonic injected PWM technique was utilized to increase the allowable voltage range of the VSC. The third-harmonic was developed and implemented in  $\alpha\beta$ -frame as depicted in the block diagram shown in Figure 3, that represents a block diagram for third-harmonic injected PWM in  $dq$ -frame, where  $m_{abc}$  generates the third-harmonic injected based on (9)-(11). The block diagram clearly illustrates how the  $dq$  to  $abc$  frame transformation of  $m_d$  and  $m_q$  results in  $m_{abc}$ . The third-harmonic injected PWM also demands  $m^2$ . Consequently, we write  $m^2$  in terms of  $m_d$  and  $m_q$  as  $m = \sqrt{m_d^2 + m_q^2}$  [34]-[36].

$$m_{aug-a}(t) = \frac{3}{2}m_a(t) - \frac{2}{3} \frac{m^3_a(t)}{m^2_\alpha + m^2_\beta} \quad (9)$$

$$m_{aug-b}(t) = \frac{3}{2}m_b(t) - \frac{2}{3} \frac{m^3_b(t)}{m^2_\alpha + m^2_\beta} \quad (10)$$

$$m_{aug-c}(t) = \frac{3}{2}m_c(t) - \frac{2}{3} \frac{m^3_c(t)}{m^2_\alpha + m^2_\beta} \quad (11)$$

PLL schematic diagram based on (12)-(14) is shown in Figure 4, which illustrates how the PLL transforms  $V_{sabc}$  to  $V_{sdq}$  and changes the  $dq$  frame speed of rotation ( $\omega$ ) to equate  $V_{sq}$  to zero as in the steady state, where  $\omega = d\rho/dt$ . Consequently,  $\rho = \omega_0 t + \theta_0$ , and  $V_{sd} = \widehat{V}_s$  [26]-[37].

The integrator, described in (13), can be recognized from Figure 4 how it is implemented using VCO (voltage-controlled oscillator). The VCO is functioning as a resetting integrator, resetting its output ( $\rho$ ) to zero as it approaches  $2\pi$ . The compensator  $H(s)$  influences the PLL dynamic performance significantly. Figure 5 explains clearly how the closed loop control of PLL is built. The reference signal,  $\omega_0 t + \theta_0$ , consists of a constant component,  $\theta_0$ , and a ramp function,  $\omega_0 t$ . With the inclusion of an integral term within the loop gain, the PLL can track the steady state zero error of the constant component of the reference signal. In order to achieve zero steady-state error for the ramp component, the loop gain must incorporate at least two integrators. Hence,  $H(s)$  must incorporate a minimum of one integral term, corresponding to  $s = 0$  pole. The other roots of  $H(s)$ , zeros and poles, are determined by closed-loop the of PLL bandwidth and stability criteria (gain and phase margins) [38]-[49].

$$V_{sq} = \widehat{V}_s \sin(\omega_0 t + \theta_0 - \rho) \quad (12)$$

$$\frac{d\rho}{dt} = \omega(t) \quad (13)$$

$$\omega(t) = H(p) V_{sq}(t) \quad (14)$$

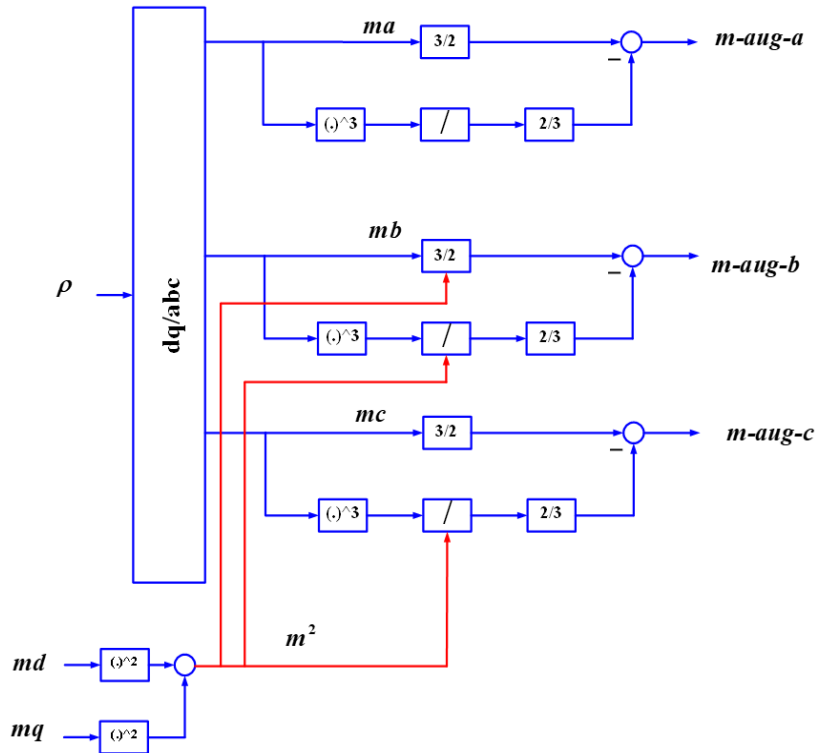


Figure 3. The block diagram of third harmonic injection for generating the modulating signal

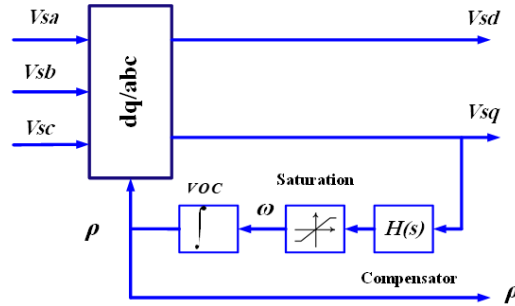


Figure 4. The phase-locked loop block diagram

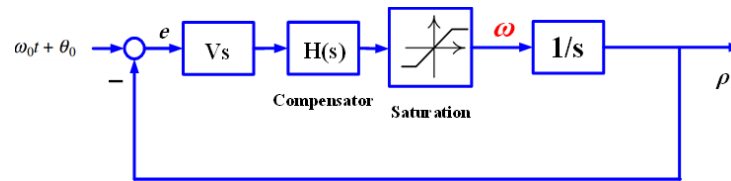


Figure 5. The closed-loop control of the phase-locked loop

## 6. SIMULATION RESULTS

The system is simulated based on the parameters shown in Table 1. The regulated DC-voltage power port, shown in Figure 1, is simulated in MATLAB Simulink. Its response to a start-up and progressive adjustments in  $P_{ext}$  is illustrated in Figure 6, which presents the obtained results when the DC-bus voltage control loop's feed-forward adjustment is turned off, the VSC system undergoes the subsequent sequence of occurrences. First, when  $P_{ext} = 0$ , The VSC's gating signals are suppressed, which makes the controllers idle; hence, the VSC's DC-side capacitors are charged via the antiparallel diodes in the switch cells, resulting in a voltage of approximately 700 V. Then, when  $t = 0.20$  s, the gating signals are unblocked, controllers are involved, and  $VDC_{ref}$  is gradually increased from 700 to 1450 V. Consequently, to raise the VDC,  $K_v(s)$  commands a negative  $P_{S-ref}$  to bring in a real power from the AC system to the VSC DC terminal;  $P_{S-ref}$  is momentarily capped to its negative threshold. When the simulation time  $t = 0.30$  s, VDC is controlled at  $VDC_{ref} = 1450$  V,  $P_s$  and  $P_{S-ref}$  remain at their modest values corresponds to the VSC power loss. Figure 6 explains a gradual increase in  $P_{ext}$ , from 0 to 1000 KW, when  $t = 0.35$  s, causing an overshoot in VDC. To retain VDC to 1450 V, the compensator has to increase  $P_{S-ref}$  as well as  $P_s$  in response to the disturbance. As  $t = 0.50$  s,  $P_{ext}$  steadily decreases from 1000 to  $-1000$  MW. Undershoots in VDC will appear until the compensator starts to reduce  $P_{S-ref}$ . The exceeded pattern at  $t = 0.50$  s is slightly different from the overshoot at  $t = 0.35$  s. After that, when  $t = 0.65$  s,  $Q_{sref}$  witnesses a transition from 0 to 500 KVAR. This disturbance does not significantly impact VDC since the contribution of  $Q_s$  to  $dV_{DC}^2/dt$  is pondered by the term  $2L/(3V_{sd}^2)$ , which is usually a small amount.

The response of the regulated DC-voltage power port, depicted in Figure 1, to disturbances is illustrated in Figure 6. When feed-forward adjustment is activated within the DC-bus voltage control loop (by incorporating a measure of  $P_{ext}$  into the output of  $K_v(s)$ ). Comparison of Figures 6 and 7 demonstrates that employing feed-forward correction clearly minimizes deviations of VDC from  $VDC_{ref}$ . Variations in  $P_{ext}$  are promptly communicated to  $P_{S-ref}$ , allowing swift power rebalancing.

The obtained simulation results explain the functionality of the DC-bus voltage controller in the  $dq$ -Frame. It is observed that significant oscillations occur when altering  $P_{ext}$  from 1000 kW to  $-1000$  kW utilizing uncompensated loop gain. Despite correcting the loop gain,  $Q_s$  remains somehow dependent on  $P_s$ ; however, VDC exhibits higher stability. When  $t = 0.20$  s, a gradual increase in  $VDC_{ref}$  from 700 to 1450 V as illustrated Figure 6. To achieve this increase,  $K_v(s)$  facilitates the transfer of actual power from the AC to the DC sides of VSC using a negative  $P_{S-ref}$ . At  $t = 0.35$  s,  $P_{ext}$  gradually increases from 0 to 1000 kW, causing an overshoot in VDC. The compensator adjusts  $P_{S-ref}$  to retain VDC to 1450 V. Afterward, at  $t = 0.50$  s,  $P_{S-ref}$  transitions sequentially from 1000 to  $-1000$  kW, resulting in undershooting in VDC until the compensator reduces  $P_{S-ref}$ . At  $t = 0.65$  s,  $Q_{S-ref}$  changes from 0 to 500 kVAR, which minimally impacts VDC, as explained in Figure 6. This phenomenon is elaborated in (6). Furthermore,

Figure 7 demonstrates how the power port controlled by the DC voltage responds to disturbances when feedforward compensation is activated for the voltage control loop of DC-bus. Utilizing feedforward correction substantially mitigates deviations of  $V_{DC}$  from  $V_{DC_{ref}}$ , as clarified in Figures 6 and 7.

Table 1. System parameters

Parameters	Value
$V_{sd}$	391 Volts
$V_{DC}$	1500 Volts
$f$	50 Hz
$f_s$	1700 Hz
$\omega_0$	314 rad/s
$C$	9625 $\mu F$
$L$	100 mH
$R$	0.75 m $\Omega$
$r_{on}$	0.85 m $\Omega$

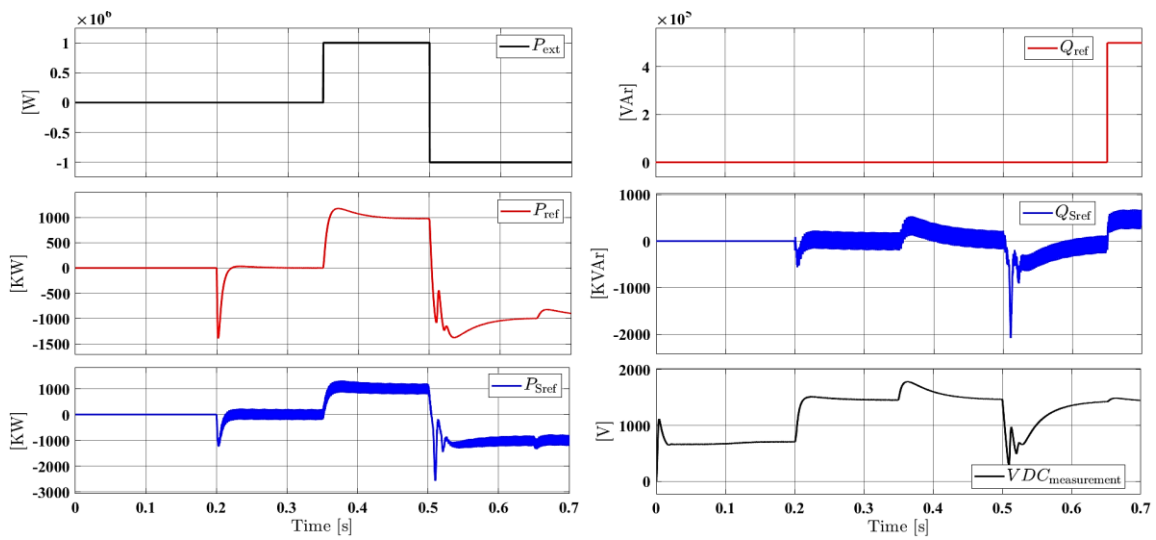


Figure 6. The dynamic behavior of a DC-voltage power port with control of no feed-forward compensation

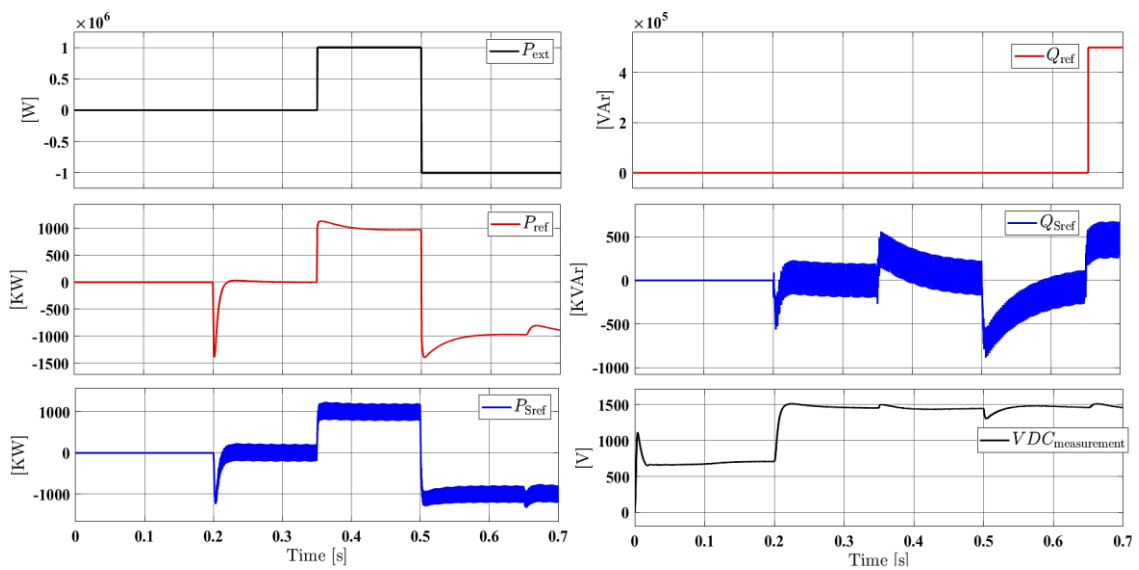


Figure 7. The dynamic behavior of DC-voltage power port with control of feed-forward compensation

## 7. CONCLUSION

The model that was simulated of the regulated DC-voltage power port implies that using a feed-forward compensation ( $P_{ext}$ ) enhances the stability of the VDC response. This enhancement is associated with the prompt transmission of any  $P_{ext}$  changes to  $P_{S-ref}$ , ensuring fast tracking of VDC to  $VDC_{ref}$  and swift recovery of power balance without a major deviation in the response. It is worth noticing that the undershoot pattern at  $t = 0.50$  s differs from the pattern of the overshoot at  $t = 0.35$  s due to the substantial changes in phase margin and frequency response between these operational conditions. As a result, the system's response to disturbances varies based on the operating conditions.

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## AUTHOR CONTRIBUTIONS STATEMENT

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C : Conceptualization

M : Methodology

So : Software

Va : Validation

Fo : Formal analysis

I : Investigation

R : Resources

D : Data Curation

O : Writing - Original Draft

E : Writing - Review & Editing

Vi : Visualization

Su : Supervision

P : Project administration

Fu : Funding acquisition

## CONFLICT OF INTEREST STATEMENT

The authors state there is no conflict of interest.

## DATA AVAILABILITY

All data underpinning the findings of this study are available from the corresponding author, [HF], upon reasonable request.

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