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A model predictive control strategy for enhance performance of totem-pole PFC rectifier

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ABSTRACT

This paper proposed a simple but effective finite control set-based model predictive control (FCS-MPC) method to control a totem-pole bridgeless boost PFC rectifier (TBBR). The control algorithm selects from the possible switching states an appropriate one that fulfills a predefined cost function. This method also successfully eliminates the zero-crossing current distortion so that the grid current can synchronize well with the grid voltage. The theoretical analysis was presented and verified by simulation. Finally, a 3.3 kW/400 Vdc prototype was fabricated and investigated through various working conditions to realize the effectiveness of the proposed control strategy. Both simulation and experimental results show that the proposed control method can ensure accurate control of DC link output voltage and sinusoidal input current with unity power factor.

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1. INTRODUCTION

Nowadays, the ongoing revolution of electric vehicles (EV) quickly carries out a production ramp-up, propelling us towards a cleaner and more sustainable transportation landscape, in which there is an essential component that silently but indispensably underpins this progress: the onboard charger (OBC) [1], [2]. This component acts as a versatile bridge, seamlessly transforming the available alternating current (AC) power from our homes and public charging stations into the direct current (DC) energy [3]-[5]. Despite its seemingly simple function, the OBC encompasses a complex configuration that balances power handling capabilities, efficiency, and cost-effectiveness. Since the OBC's operation begins with receiving AC power, a power factor correction (PFC) rectifier is a must for achieving a unity power factor so that all the energy drawn from the AC mains can be put into useful work [3]-[5]. Various approaches exist, with each offering trade-offs between efficiency, cost, and size. Among them, a specific topology, known as the totem-pole boost PFC, stands out for its ability to deliver exceptional efficiency and power density, making it a compelling choice for various applications [6]-[10]. Traditionally, the boost PFC rectifier operates with the aid of the diode bridge rectifier, which introduces some inherent limitations. To address this, the totem-pole bridgeless boost PFC rectifier (TBBR) was devised to eliminate the diode bridge altogether, such that the line-frequency switching MOSFETs are used for rectification; however, it needs more sophisticated control algorithms to ensure proper operation and maintain efficiency across a wider range of operating conditions.

In particular, traditional proportional-integral (PI) and proportional-resonant (PR) controllers [11]-[18] are widely adopted for voltage and current regulation but suffer from phase delays and complex tuning procedures. These issues lead to poor tracking of sinusoidal current references, especially under dynamic

load conditions. Moreover, such methods are ineffective in mitigating current distortion near grid voltage zero-crossing points, which negatively impacts input current total harmonic distortion (THD) and overall power quality. In the situation of a PI controller, at first, the DC-side voltage is obtained, then compared with the reference voltage. Subsequently, the error is processed through a PI regulator, which is configured to generate an error-adjusted command synchronized with the line frequency. Later, the input current reference is determined by the output of the voltage regulator and the AC current signal in the same manner. The current regulator ensures that the input current tracks the reference current until it achieves the desired level. However, the PI controller works well for only DC reference, while it frequently can't be adequate maintained performance if the command is a sinusoidal signal, since the inner PI controller loop introduces a phase delay when tracking the sinusoidal current waveform. The PR controller can resolve the issue, but the design parameters of the PR controller are complicated to fit in varying line frequency [19]-[21]. Several control methods are applied for the PFC to improve the converter dynamics, such as: sliding mode control [22]-[24], hysteresis control [25], [26], fuzzy-logic control [27]. However, with the quick evolution of power devices and digital processors, the PI controller, sliding mode control, and hysteresis control face competition from the predictive control strategies, which offer simpler in concepts, easier implementation, and superior dynamic performance.

Basically, the single-phase TBBR has high-frequency switching MOSFETs on one leg (Q_1 and Q_2) and line-frequency switching MOSFETs on the other leg (S_1 and S_2) as shown in Figure 1. Its operating principle during both positive and negative half cycles of the AC input voltage is determined by the switching sequence. During the positive half cycle, S_2 is the control switch and S_1 is the synchronous switch; simultaneously, Q_1 is turned on and Q_2 is always inactive. When switch S_2 is turned off, the AC source charges the inductor L_g while the output capacitor C_o discharges through the load to maintain a regulated voltage at the output. When switch S_2 is turned on, the inductor L_g discharges the stored energy, generating a current that charges the output capacitor C_o. During the negative half cycle, the operation of the TBBR is similar except the role of switches is swapped, where S_1 becomes the main switch and S_2 turns into a complementary switch, meanwhile Q_2 is turned on, leaving Q_1 inactive.

As described, the TBBR has a simple configuration, and its operation depends on the possible combinations of the on/off switching states of the high-frequency switches. Subsequently, the control algorithm for TBBR can be simplified as selecting from the possible switching states an appropriate one that fulfills a predefined condition. By taking into account the finite set of possible switching states (only 2 applicable sets), it is suggested that finite control set model predictive control (FCS-MPC) is a very powerful concept for designing controllers. The main advantage of this control strategy is that the switching states are directly considered as the control input so that modulation stages are deducted from the overall system. Moreover, it also has fast dynamic response, as well as easy inclusion of nonlinearities and constraints in the design of controller, making it popular in digital control of power converters. Based on discrete model of the converter, the FCS-MPC evaluates a cost function in accordance with the control objectives by enumerating all possible combinations of switching states over a finite horizon. The switching state that results in the minimal value for the cost function is selected as the best switching state within the next switching cycle.

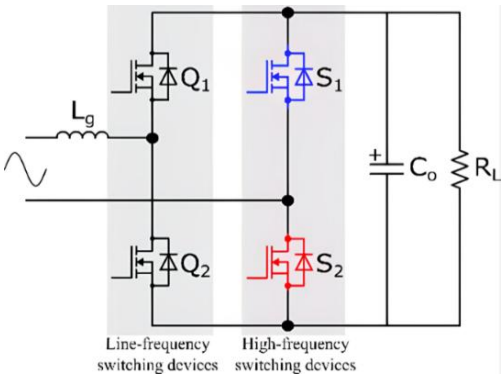

Figure 1. Configuration of a single-phase totem-pole bridgeless boost PFC rectifier (TBBR)

While FCS-MPC has demonstrated benefits in various power electronic applications, its use in TBBR systems remains relatively unexplored—particularly with regard to addressing zero-crossing distortion

and maintaining simplicity in control design. To fill this research gap, this paper proposes a novel two-step prediction horizon FCS-MPC strategy tailored for the TBBR. The main contributions of this work are as follows:

- Development and implementation of a two-step horizon FCS-MPC algorithm that eliminates the need for modulation stages, offering faster dynamic response and simplified control structure.
- Effective mitigation of zero-crossing current distortion, resulting in improved power quality and cleaner input current waveforms.
- Experimental validation using a 3.3 kW, 400 Vdc hardware prototype under both nominal and disturbed grid conditions, demonstrating the practical feasibility of the proposed method.
- Achievement of power factor >0.99 and input current THD <5%, fully compliant with IEC-61000-3-2 Class A standards.

This paper is conducted as follows: i) Section 2 discusses the operating principles of the TBBR and limitations of conventional PI-based controllers ii) Section 3 presents the proposed FCS-MPC approach, including a mathematical predictive model, cost function design, and the optimization routine; iii) Section 4 provides affirmative simulation as well as experimental results that validate the effectiveness of the proposed control strategy; and iv) Finally, section 5 concludes the paper and outlines future research directions.

2. ANALYSIS OF CIRCUIT OPERATION

2.1. Analysis of TBBR converter

This section analyzes the continuous-time operation of the TBBR according to Kirchhoff's laws during both positive and negative half cycles as shown in Figures 2(a) and 2(b), respectively, in accordance with the control switches actions to formulate the future grid current prediction as a function of its present and previous values.

As shown in Figure 2(a), during the positive half cycle, in the interval that S_2 is off, a mesh with the inductor L_g, the switch S_1, the switch Q_1, and the grid voltage source v_g is formed and result in the differential equation, as (1).

$$\frac{di_L}{dt} = \frac{v_g}{L_g}; \frac{dv_o}{dt} = -\frac{1}{R_L C_o} v_o \tag{1}$$

Contrastingly, in the interval that S_2 is on, the current flows through the switch S_2 and the switch Q_1 to the output capacitor and load, which yields as (2).

$$\frac{di_L}{dt} = -\frac{1}{L_g} v_o + \frac{v_g}{L_g}; \frac{dv_o}{dt} = \frac{1}{C_o} i_L - \frac{1}{R_L C_o} v_o \tag{2}$$

Likewise, during the negative half cycle (as can be seen in Figure 2(b)), in the interval that S_2 is off, the current flows through the switch S_1 and the switch Q_2 to the output capacitor C_o and load R_L. The expressions that describe this behavior as (3).

$$\frac{di_L}{dt} = \frac{1}{L_g} v_o + \frac{v_g}{L_g}; \frac{dv_o}{dt} = -\frac{1}{C_o} i_L - \frac{1}{R_L C_o} v_o \tag{3}$$

Conversely, in the interval that S_2 is on, the input current flows through the switch S_2 and the diode Q_2, while the output voltage v_o is held steady by the output capacitor C_o. This operation can be expressed in terms of (4).

$$\frac{di_L}{dt} = \frac{v_g}{L_g}; \frac{dv_o}{dt} = -\frac{1}{R_L C_o} v_o \tag{4}$$

Otherwise, applying forward Euler's method to the current change expression $\frac{di_L}{dt}$ and voltage change expression $\frac{dv_o}{dt}$ for the sampling time ts, the discrete-time approximation can be obtained as (5).

$$\frac{di_L}{dt} = \frac{i_L(k+1) - i_L(k)}{t_s}; \frac{dv_o}{dt} = \frac{v_o(k+1) - v_o(k)}{t_s} \tag{5}$$

Where 'k' represents the current step and '$k+1$' represents the next step.

2.2. Conventional PI controller for power factor correction

A conventional pulse width modulation (PWM) algorithm was presented for generating the gate driving signals of high frequency switching devices. The controller consists of two control loops: the voltage

loop controller which regulates the output voltage of the TBBR and the current loop controller which makes the grid current waveform to be identical to the grid voltage waveform. In voltage loop, the DC output voltage is attained and subtracted from the derived DC output voltage, and the error lately passes through a PI controller to acquire the equivalent input conductance of the converter. The grid current reference is generated by multiplying the equivalent input conductance with the adjusted grid voltage to serve as the input of current loop. In the current loop, another PI controller varies the duty cycle of the switches until the grid current reaches the reference signal. To improve the quality of current control, a duty-ratio feedforward is introduced and combined with the output of current loop controller. The complement of duty-ratio feedforward allows the PI controller to adapt only a small value of input current error, and thus low input current distortion can be maintained by avoidance of high controller gain. The schematic diagram of voltage-current loop PWM controller including duty-ratio feedforward is presented in Figure 3.

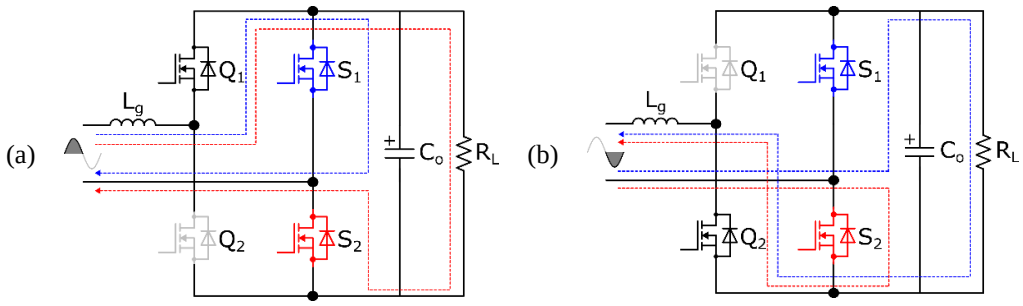

Figure 2. Current flows in TBBR during (a) positive half cycle and (b) negative half cycle

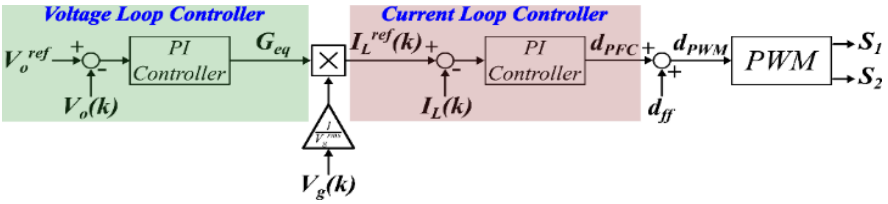

Figure 3. Control diagram of voltage-current loop PWM controller for TBBR

3. PROPOSED FCS-MPC FOR POWER FACTOR CORRECTION

The proposed PFC control diagram for TBBR is shown in Figure 4. An FCS-MPC scheme is employed to generate the driving signals for high-frequency switches. By selecting a proper cost function, the output voltage V_o can be regulated, and the power factor correction of the input current i_L can be realized. FCS-MPC offers precise and dynamic control of the high-frequency switches, allowing for fast response to load changes and grid disturbances, which ensures efficient power conversion and minimizes energy losses. Besides, the conduct time of the line-frequency switches is determined by a zero crossing detection (ZCD) scheme, where the grid voltage is sampled and evaluated to generate the switch gating signals. By ensuring proper synchronization with the grid frequency, ZCD minimizes the risk of malfunction and power quality issues. The detailed implementation of the FCS-MPC will be illustrated in the following:

3.1. Predictive current model

The predicted grid current in the instant '$k+1$' with respect to the positive half cycle is as (6),

$$i_L(k+1) = i_L(k) - \frac{t_s}{L} S_2 v_o(k) + \frac{t_s}{L} v_g(k), \quad S_2 \in \{0,1\} \tag{6}$$

and, for the negative half cycle, the predicted inductor current is as (7).

$$i_L(k+1) = i_L(k) + \frac{t_s}{L} S_2 v_o(k) + \frac{t_s}{L} v_g(k), \quad S_2 \in \{0,1\} \tag{7}$$

In the same manner, the predicted grid current in the instant '$k+2$' can be obtained as (8).

$$i_L(k+2) = i_L(k+1) - \frac{t_s}{L} S_2 v_o(k+1) + \frac{t_s}{L} v_g(k+1), \quad S_2 \in \{0,1\} \tag{8}$$

With $v_0(k+1) = v_o(k) + \frac{t_s}{C_o} i_L(k) - \frac{t_s}{RC_o} v_o(k)$, and as (9).

$$i_L(k+2) = i_L(k+1) + \frac{t_s}{L} S_2 v_o(k+1) + \frac{t_s}{L} v_g(k+1), \quad S_2 \in \{0,1\} \tag{9}$$

With $v_0(k+1) = v_o(k) - \frac{t_s}{C_o} i_L(k) t_s - \frac{t_s}{RC_o} v_o(k)$. The predicted grid voltage $v_g(k+1)$ is a prerequisite for this course and can be estimated by using a second-order extrapolation regarding the present and previous values.

$$v_g(k+1) = 3v_g(k) - 3v_g(k-1) + v_g(k-2) \tag{10}$$

3.2. Reference current estimation

As mentioned previously, the control algorithm for TBBR should drive the grid current i_L perfectly in phase with the grid voltage v_g so that the maximum power transfer can be realized regarding to unity power factor. Applying the time-domain power theory (FBD method), which esteems the TBBR as a conductance from the perspective of mains electricity, the grid current reference i_L^{ref} can be established as (11).

$$i_L^{ref} = \frac{P_o}{V_g^2} v_g \tag{11}$$

Where P_o is the desired DC output power and V_g is the nominal rms value of the grid voltage. Transforming into discrete form, (11) can be rewritten as (12).

$$i_L^{ref}(k) = \frac{P_o}{V_g^2} v_g(k) \tag{12}$$

Obviously, the grid current reference value is linearly scaled to the change of output power P_o, and inherently adjusted regarding the operating condition. Moreover, the waveform of the grid current reference should correspond to the waveform of the grid voltage consistently. As the grid voltage contains redundant harmonics, digital passive filters need to be put into effect, in which the grid current reference exclusively keeps track of the fundamental harmonic of the grid voltage. Then, the grid current reference can carry on a true sinusoidal waveform despite the distortion in the electric power line.

3.3. Cost function and optimization approach

The two-step prediction FCS-MPC strategy predicts the behavior of the TBBR on the next two sampling intervals with two primary objectives: i) accurate tracking of the reference grid current i_L for power factor correction and output voltage regulation, and ii) minimization of grid current harmonics to improve power quality. To achieve these objectives, the cost function associated with the two-step prediction is expressed as (13).

$$J = \sum_{i=1}^{2} \left[i_L^{ref}(k+i) - i_L(k+i) \right]^2 + \lambda_p [i_L(k+i) - i_L(k+i-1)]^2 \tag{13}$$

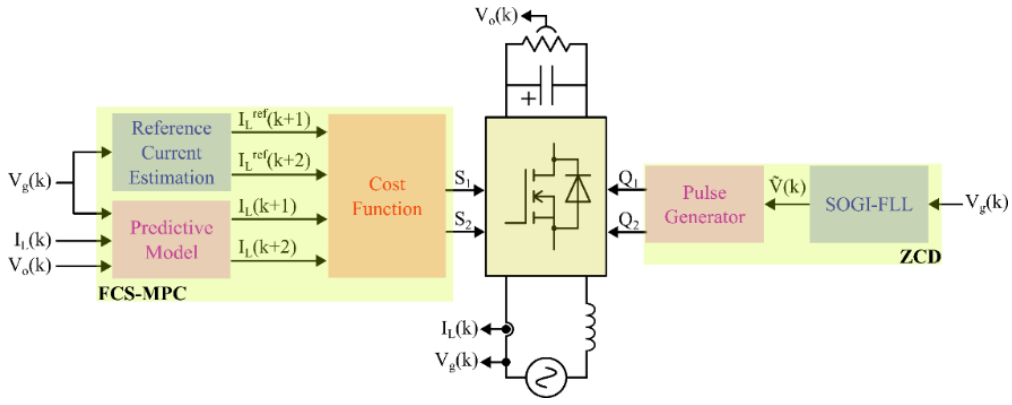

Figure 4. Proposed PFC control block diagram of TBBR

The first term, which minimizes the error between the predicted grid current $i_L(k+i)$ and its reference $i_L^{ref}(k+i)$, ensures that the converter delivers the required power to regulate the output voltage properly. Without this term, the grid current would not follow the desired trajectory, leading to poor voltage regulation. The second term penalizes rapid variations in the grid current, reducing high-frequency harmonics and ensuring a smooth waveform. Without this term, the controller may aggressively switch states, causing high THD and instability in power delivery. By combining both terms, the cost function enables a well-regulated output voltage while maintaining a low-distortion grid current. The sequence minimizing the cost function is selected and employed in the TBBR during the next sampling interval.

The weighting factor λ_p in the cost function of FCS-MPC plays a crucial role in balancing current tracking accuracy and harmonic minimization, directly influencing output voltage regulation and power quality. Its tuning is essential, as an overly small λ_p leads to fast but noisy current tracking with high THD, while an excessively large λ_p results in a smoother current but slower response to load changes. A practical approach to estimating λ_p is given by the formula $\lambda_p = \frac{L}{t_s V_o}$, where L (grid inductance) affects natural current smoothing, t_s (sampling time) determines control reaction speed, and V_o (output voltage) influences power transfer stability. The empirical factor k (typically between 0.1 and 1) is adjusted through simulation and experimental validation to achieve an optimal trade-off. Higher L naturally smooths current, allowing a lower λ_p, whereas shorter t_s improves control accuracy, reducing the need for additional smoothing. A higher V_o increases power fluctuations, necessitating a larger λ_p for better stability. A well-optimized λ_p ensures low THD, fast output voltage stabilization, and compliance with power quality standards.

Current references i_L^{ref} at future time steps '$k+1$' and '$k+2$', which is adapted from (11), can be derived by extrapolating from past and present reference values and finally show up in (14) and (15).

$$i_L^{ref}(k+1) = \frac{P_o}{V_g^2} v_g(k+1) = \frac{P_o}{V_g^2}\left[3v_g(k) - 3v_g(k-1) + v_g(k-2)\right] \quad (14)$$

$$i_L^{ref}(k+2) = \frac{P_o}{V_g^2} v_g(k+2) = \frac{P_o}{V_g^2}\left[6v_g(k) - 8v_g(k-1) + 3v_g(k-2)\right] \quad (15)$$

Due to a very small prediction horizon of FCS-MPC (N = 2) as well as admissible switching states (S = 2), the exhaustive search is a useful method to solve the minimization problem exposed by (13). This method enumerates all possible solution sets and checks each one to see if it satisfies the problem's conditions. The one with the smallest cost is chosen as the control input. For every time-step, the algorithm obeys the following steps: i) Determine all possible switching states over the prediction horizon; ii) For each of these switching states, compute the predicted grid current i_L^{ref} according to (6)-(9) and the predicted grid current reference i_L^{ref} according to (14) and (15); iii) For each switching state, compute the cost J according to (13); and iv) Choose the switching state which minimizes the cost and apply to the TBBR. The procedure for selecting the optimal switching sequence is summarized in Figure 5.

3.4. Analysis and challenges of FCS-MPC

Unlike conventional linear controllers, FCS-MPC is inherently nonlinear and operates in a discrete-time domain, making stability analysis more complex. However, stability can be assessed through Lyapunov-based methods, where a Lyapunov candidate function was selected based on the deviation of the state from its reference, as in (16).

$$V(k) = \frac{1}{2}\left(i_L(k) - i_{L,ref}(k)\right)^2 \quad (16)$$

The difference in the Lyapunov function between two successive time steps is as (17).

$$\Delta V = V(k+1) - V(k) \quad (17)$$

Substituting $i_L(k+1)$ from the system equation, as (18).

$$\Delta V = \frac{1}{2}\left(i_L(k+1) - i_{L,ref}(k+1)\right)^2 - \frac{1}{2}\left(i_L(k) - i_{L,ref}(k)\right)^2 \quad (18)$$

FCS-MPC selects the control action that produces the smallest predicted error in future states, ensuring that the deviation from the reference is reduced in each step. It follows that, as shown in (19) and (20).

$$\left|i_L(k+1) - i_{L,ref}(k+1)\right| < \left|i_L(k) - i_{L,ref}(k)\right| \quad (19)$$

Which implies as (20).

$$\Delta V = V(k+1) - V(k) < 0 \quad (20)$$

Thus, the Lyapunov function is monotonically decreasing, proving asymptotic stability. The weighting factor λ_p helps in ensuring a smooth current response, further preventing instability. To further enhance stability, adaptive tuning of λ_p can be implemented, where its value is adjusted dynamically based on system conditions. Additionally, implementing constraint handling (such as current limits) ensures that the controller does not drive the system into unstable regions.

The implementation of FCS-MPC imposes significant computational requirements due to the need for real-time current prediction, cost function evaluation, and optimal switching state selection within each control cycle. Unlike traditional controllers such as PI or PR controllers, which rely on simple algebraic calculations, FCS-MPC requires solving discrete-time system equations and evaluating multiple switching scenarios at each time step. The computational burden increases with the prediction horizon and the number of switching states considered. In this study, a two-step prediction horizon with two possible switching states per step results in an acceptable computation time. To meet these demands, high-speed digital signal processors (DSPs) or field-programmable gate arrays (FPGAs) are often required. The sampling time determines the maximum allowable computation time per cycle so that if the execution time exceeds this limit, the controller will fail to update switching states in real time, leading to performance degradation. Once settled, FCS-MPC provides ability to directly optimize switching decisions without requiring a modulation stage, offering superior dynamic response and power factor correction.

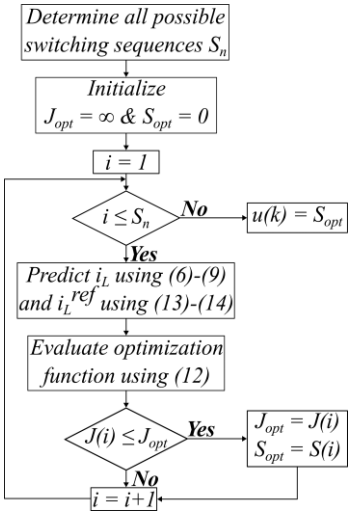

Figure 5. The procedure for the exhaustive search optimization approach

4. RESULTS AND DISCUSSION

4.1. Simulation results

To validate the theoretical analysis, a 3.3 kW TBBR has been designed using PSIM®, where the key parameters of the converter are listed in Table 1. The corresponding gating signals of all active switches during one grid cycle are displayed in Figure 6. Figure 7 shows the steady-state waveform of the grid-side current i_L and grid-side voltage v_g at full load with the implementation of the FCS-MPC method. It indicates that the TBBR achieves a high-power factor of around 0.99 with a low input current THD of 2.67% approximately.

4.2. Experimental results

To verify the theoretical results of the system, some experiments were conducted using the 3.3 kW totem-pole bridgeless boost PFC converter prototype. The key parameters of this prototype are shown in Table 2. Parameters used in the experiment had a slight tolerance during the operation, and the optimal tuning value λ_p achieved through the simulation was recalculated and applied to the experiment.

Figure 8 illustrates the entire structure of the proposed totem-pole PFC rectifier system. The TMS320F28379D DSP collects voltage and current signals via ADCs, processes them through a predictive model and cost function minimization, and generates optimized switching states for the driver board to achieve high power quality. The computation time for the proposed method is 12.2 us. All electrical responses were observed and evaluated by a digital oscilloscope (Siglent SDS2104X Plus) to perceive the overall system's performance in reality.

Figures 9(a) and 9(b) shows the steady-state operating signals of the converter, including output voltage (Chanel 1), grid voltage (Chanel 2) and grid current (Chanel 3), at rated power with resistive load of 50 Ω and 100 Ω, respectively in case of 180 Vrms/50 Hz input voltage. It can be seen that the zero-crossing current distortion is mostly disappeared and the grid current can be well synchronized with the grid voltage. However, the grid voltage contains some harmonic components, such that the power factor was measured to be 0.992. The power factor is obtained at 0.984 since operation at a lighter load as shown in Figure 9(b). The output voltage is regulated at 400 V with a decent fluctuation.

Figure 10(a) illustrates the steady-state operating signals of the converter supplied by residential power lines of 220 Vrms/50 Hz and working at rated power with a resistive load of 50 Ω. The input current is carried out in phase with the input voltage such that the power factor can achieve the value of 0.995. It is concluded that the FCS-MPC method shows a good power factor of well above 0.99 at full power regardless the level of grid voltage. The output voltage of 400 V is well-regulated with acceptable DC-link voltage ripple. Figure 10(b) demonstrates the steady-state operating signals of the converter supplied by residential power lines of 220 Vrms/50 Hz and worked at half of rated power with a resistive load of 100 Ω. By cutting the power load down to 50%, it smooths out the DC-link voltage ripple so that the output waveform then becomes quite flat. The grid-side power factor at 50% load condition was measured to be 0.988. This result shows that the power factor threshold remains the same either when the converter works at full power load or when it runs at half power load, which indicates the benefit of using FCS-MPC method.

Table 1. Parameters used for simulation

Parameters	Symbol	Value
Input voltage	$V_{in,rms}$	220 V
Line frequency	f_g	50 Hz
Line inductance	L_g	3 mH
Rated output power	P_o	3.3 kW
Rated output voltage	V_o	400 V
Output capacitance	C_o	4000 µF
Sampling time	T_s	10 µs

Table 2. Parameters used for the experiment

Parameters	Symbol	Value
Grid voltage (rms)	V_{in}	180 V~220 V
Line frequency	f_g	50 Hz
Line inductance	L_g	3 mH
Rated output power	P_o	3.3 kW
Rated output voltage	V_o	400 V
Output capacitance	C_o	4000 µF
Power switches	S_1, S_2, Q_1, Q_2	NVHL020N120SC

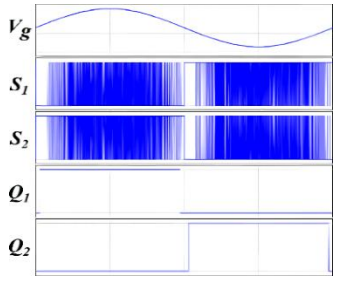

Figure 6. Switching pattern of devices during one grid cycle

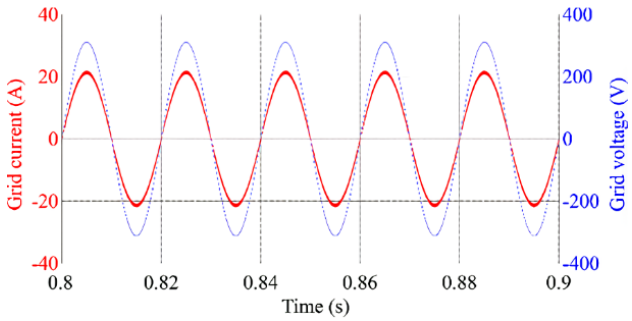

Figure 7. Grid side waveforms during steady state at full load

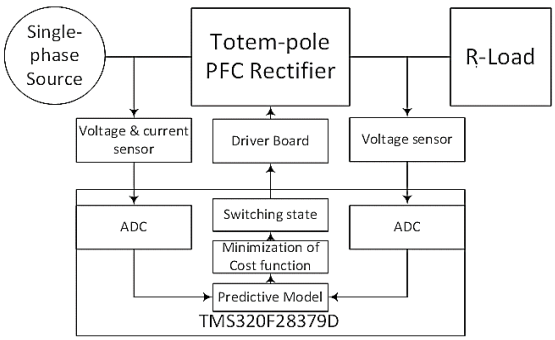

Figure 8. Block diagram of the hardware setup of TBBR

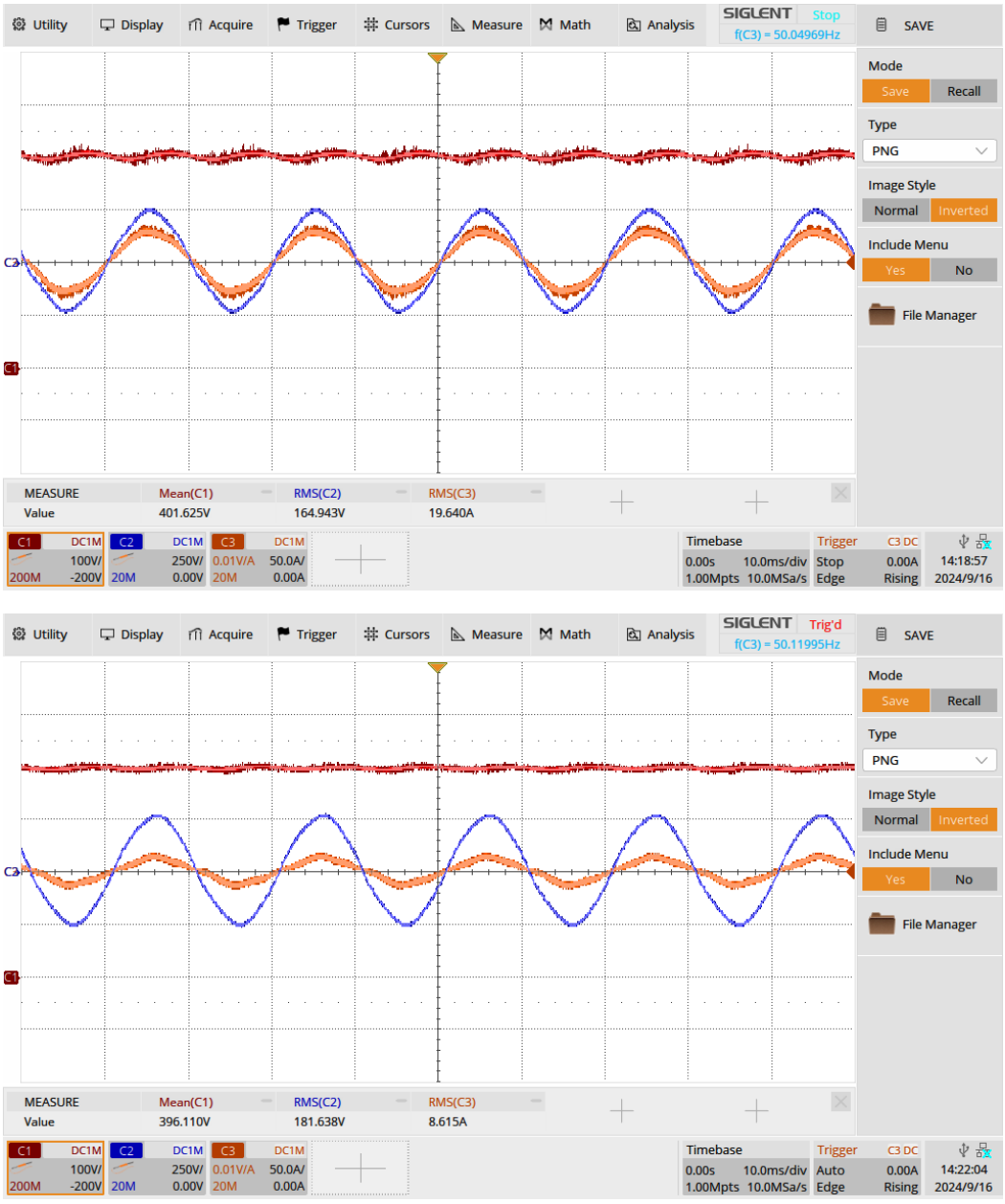

Figure 9. Experimental waveforms of TBBR in case of 180 Vrms AC input: DC output voltage (Chanel 1, 100 V/div), grid voltage (Chanel 2, 250 V/div) and grid current (Chanel 3, 50 A, div) with resistive load of (a) 50 Ω and (b) 100 Ω

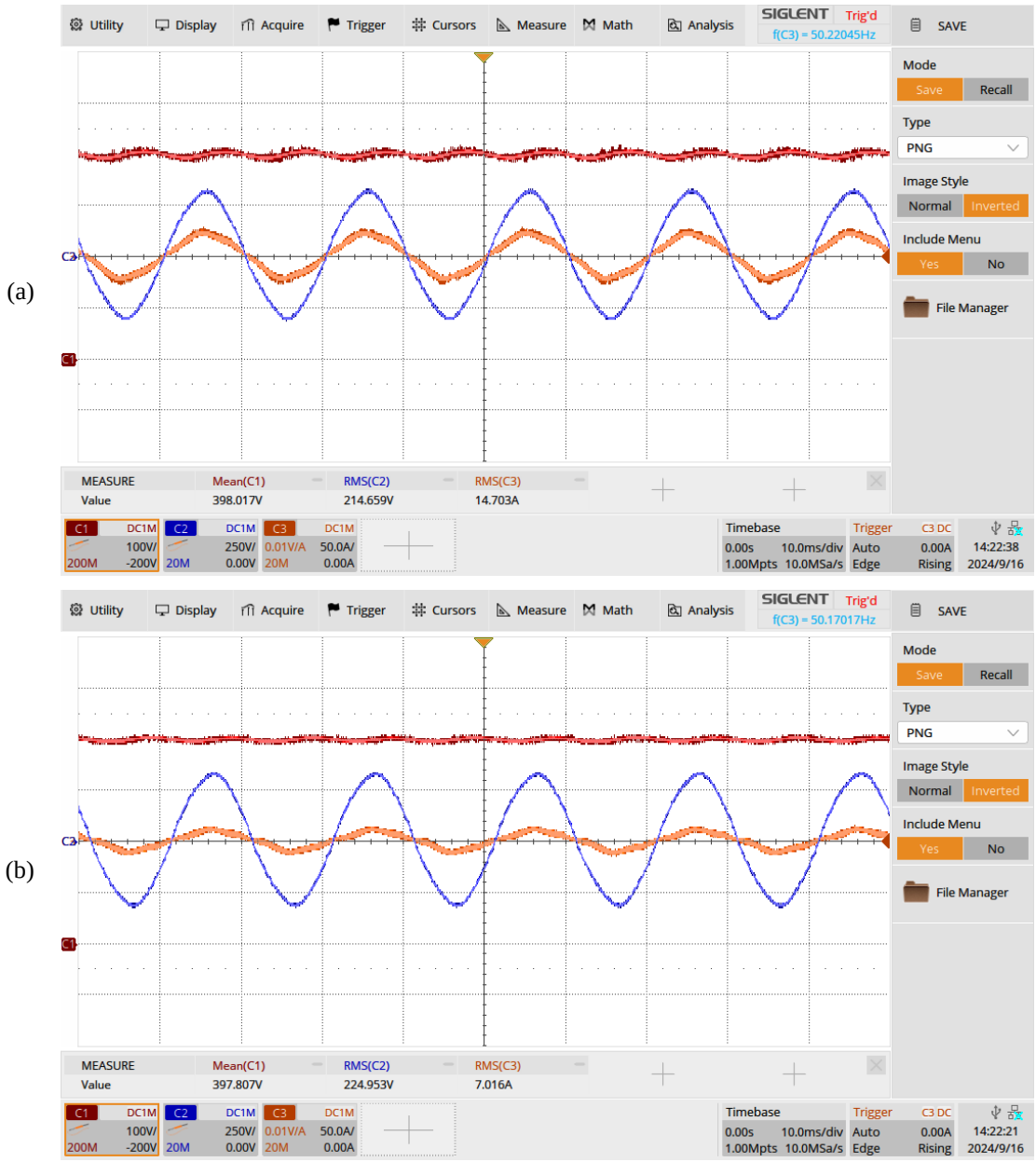

Figure 10. Experimental waveforms of TBBR in case of 220 Vrms AC input: DC output voltage (Chanel 1, 100 V/div), grid voltage (Chanel 2, 250 V/div), and grid current (Chanel 3, 50 A, div) with resistive load of (a) 50 Ω and (b) 100 Ω

Figure 11 displays the input current THD analysis with the FCS-MPC method, where the converter operates at 220 Vrms/50 Hz input and full load condition. Obviously, the amplitude of a particular harmonic current satisfies its corresponding requirement prescribed in the IEC-61000-3-2 Class A standard. The total harmonic distortion of the input current is smaller than 5%. A step load change from half to full load using a resistive load is illustrated in Figure 12. The waveforms of the input voltage and current, as well as the output voltage, confirm that the output voltage remains tightly regulated throughout the transient, with only a slight and brief dip (5%~20 V). These results highlight the converter's fast dynamic response and strong control performance under sudden load variations.

As shown in Figure 13, the efficiency of the implemented PFC circuit has been measured across a wide range of load power levels, from 0.3 kW to 3.3 kW. The results demonstrate that the circuit maintains high efficiency throughout the entire operating range, with a minimum efficiency of 92.15% at light load and a maximum efficiency of 98.82% at full load. This trend clearly indicates the strong performance of the power stage under varying load conditions. Additionally, the input current THD was also measured and

included in Figure 13 to provide a more comprehensive evaluation of the circuit's power quality. The measured THD values decrease from 12.39% at light load to 4.97% at full load, further supporting the effectiveness of the circuit in shaping the input current."

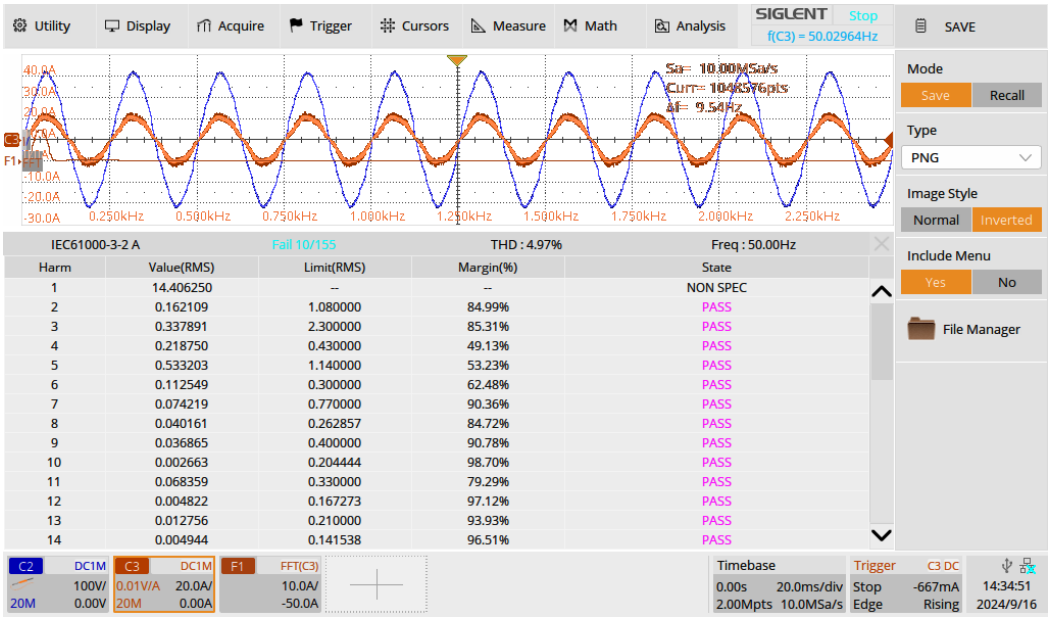

Figure 11. Input current THD analysis with the FCS-MPC method, where the converter operates at 220 Vrms/50 Hz input and full load condition

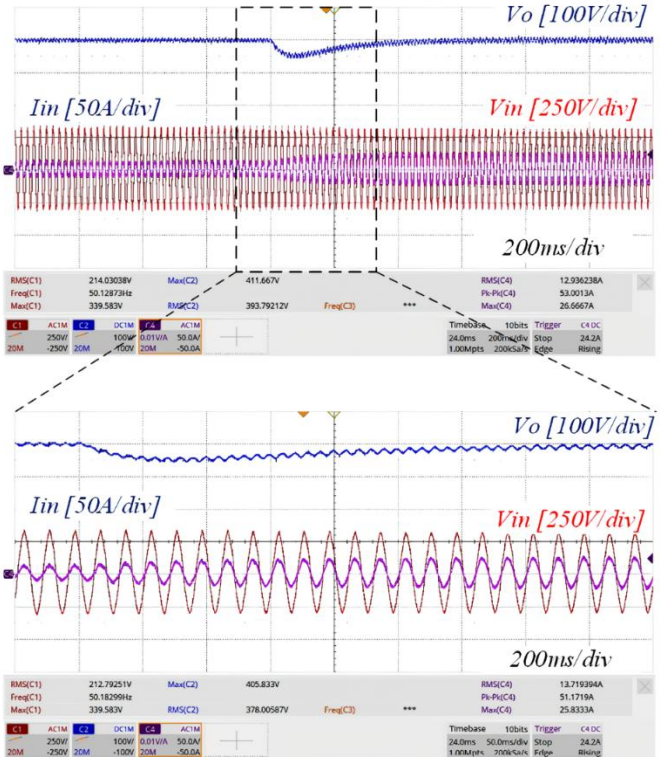

Figure 12. The dynamic process of the TBBR when the load changes from 50% load to full load

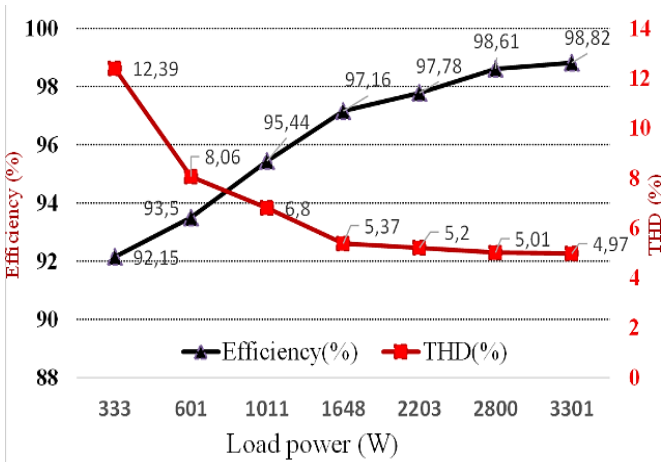

Figure 13. The performance of the proposed method for TBBR, including the efficiency and THD

From the experimental results, the proposed FCS-MPC control strategy demonstrated excellent power quality performance across a range of operating conditions. Specifically, the system achieved a high power factor of 0.995 at full load and maintained values above 0.98 at partial load, effectively minimizing reactive power and fulfilling one of the core design objectives. Further, the input current THD remained below 5%, thereby complying with IEC-61000-3-2 Class A standards, and confirming the method's capability in producing clean, sinusoidal current waveforms. Another significant achievement is the elimination of zero-crossing current distortion, as evidenced by the experimental waveforms. The proposed method successfully mitigated current spikes that typically occur around the zero-voltage crossing, which had been a major challenge for traditional controllers and one of the primary motivations for this study.

5. CONCLUSION

This paper proposed a cost-effective control method based on two-step FCS-MPC for implementing the power factor correction of the single-phase TBBR. Since it is an FCS-MPC-controlled converter, the pulse width modulator is not necessary; alternatively, the switching sequence is determined by a predefined cost function and predictive model deduced from system states. Accordingly, the discrete-time mathematical expressions of single-phase TBBR are used to obtain predicted current in the next instants, and lately, the cost function, which derives from reference current error and previous current error, is accomplished. Finally, the sequence minimizing the cost function is fed into the high frequency switching devices. Based on the relevant theories, a computer simulation is carried out with the results that the FCS-MPC-controlled TBBR attains the near unity power factor with no current spikes at zero-crossing points. For practical validation, a 3.3 kW-400 Vdc prototype of TBBR was fabricated. The experimental results demonstrate that the converter successfully provides the power factor of around 0.99 at both full load and half load condition, which indicates the effectiveness of the proposed control strategy.

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AUTHOR CONTRIBUTIONS STATEMENT

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C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

Derived data supporting the findings of this study are available from the corresponding author [NDT], on request.

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