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Multi-carrier PWM techniques to assess the performance of a 5-level diode clamped multilevel inverter fed PMSM drive

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ABSTRACT

The advantages of multilevel inverters (MLIs) have led to their increased use in high- and medium-voltage power applications. These inverters reduce harmonic content, common-mode voltage, dv/dt stress on switches, and electromagnetic interference, among other things. In recent decades, drives for permanent magnet synchronous machines (PMSMs) that rely on inverters have become increasingly popular in both commercial and residential settings due to their great performance. Phase disposition (PD), phase opposition disposition (POD), and alternate phase opposition disposition (APOD) are three multi-carrier pulse width modulation (MCPWM) approaches that were simulated in this work to explore a 5-level DCMLI-fed PMSM. In order to create control pulses, each method compares reference signals with carrier signals that are either triangular or trapezoidal. Detailed comparisons with conventional three-level voltage source inverters (VSIs) are made based on the results. A 63.21 percent improvement in the total harmonic distortion (THD) of the output voltage and a 26.52% improvement in the THD of the stator current are both supported by experimental evidence.

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1. INTRODUCTION

Due to their superior output waveform, multilevel inverters are used in medium/high-power applications [1]. The previous works of literature propose and account for the neutral point clamped (NPC), flying capacitor (FC), and cascaded H-Bridge (CHB) multilevel inverters [2]-[5]. Due to its modularity and controllability, the CHB architecture is popular [6]. In multilayer inverters, pulse width modulation (PWM) helps maximize output. Other modulation methods include selective harmonic elimination PWM (SHE-PWM), space vector PWM (SVPWM), and multi-carrier PWM (MCPWM) [7], [8]. The primary drawback of SHE-PWM and SVPWM is the difficulty in calculating to regulation of multilayer inverters [9].

The MCPWM approach is the most popular because it generates multilayer pulses to control power switches for any output-level inverter by comparing reference signals with triangle signals [7], [10]. Broadly, multicarrier PWM is classified by carrier and modulating signals. PWM can be used to implement any type

of inverter. There are five well-known carrier signals: phase disposition (PD), phase opposition and disposition (POD), alternate phase opposition disposition (APOD), carrier overlapping (CO), and phase shifted (PS) [11]-[15]. However, level-shifted PWM approaches are best for the NPC and inappropriate for the CHB owing to power balance issues [4], [16]. In several studies, researchers have recommended employing level-shifted PWM to solve the CHB power balance problem [17]-[20]. Phase-shifted PWM (PSPWM) balances power in FC and CHB using carrier signals from each power cell. There are several modulating signals, such as sinusoidal PWM (SPWM), third harmonic injected PWM (THPWM), 60˚ modulated sinusoidal PWM (SDPWM), and trapezoidal PWM (TRPWM), each with pros and cons [21]-[24]. SPWM is the most popular reference signal since it's easy to make. Flattening the top of THPWM, SDPWM, and TRPWM reference signals allows linear modulation.

Carrier and modulating signals allow amplitude, frequency, and phase independence. Multiple multilayer PWM may be formed from carrier and modulating signals [25]. Several researchers have proposed and demonstrated multicarrier PWM algorithms for specific applications in recent years [26]-[28]. No literature exists on the simplest approach to creating multicarrier PWM signals for n-level inverters and THD analysis and comparison. This article simulates a 5-level DCMLI-fed PMSM using three carrier PWM methods. SPWM, THIPWM, and SVPWM are modulation techniques employed here. Phase disposition, phase opposition, and alternate phase opposition are these modulation methods. In all modulation schemes, triangular carrier and trapezoidal carrier signals are compared to reference signals to create control pulses. The findings have been analyzed and compared to experimental data for the fundamental component of output voltage and %THD. Multi-level inverters provide several potentials due to the synthesis of many voltage levels. In recent decades, inverter-based PMSM motor drives have achieved great performance and have been used in numerous home and industrial applications. Figure 1 shows the MLI architecture of fed PMSM drive.

The key contributions of this work are summarized as follows: i) A comprehensive performance evaluation of PD, POD, and APOD multi-carrier PWM techniques applied to a 5-level diode-clamped multilevel inverter feeding a PMSM drive; ii) Quantitative comparison of harmonic distortion under constant and variable speed conditions; iii) Demonstration of significant THD reduction compared to conventional 3-level VSI-based drives; and iv) Validation of the proposed scheme under realistic operating conditions, highlighting its suitability for high-performance motor drive applications.

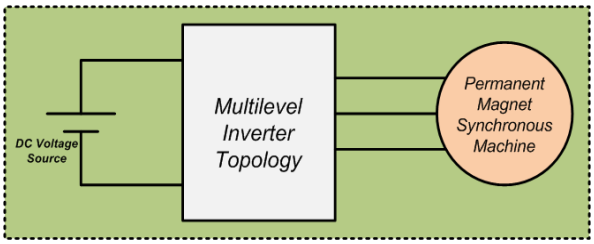

Figure 1. Representation of a multilevel inverter-fed PMSM drive

2. DIODE CLAMPED MULTILEVEL INVERTER

In their initial proposal for a multilayer inverter (MLI) architecture, study in [29] used the diode clamped multilayer inverter (DCMLI) topology. Because of its durability, DCMLI is a desirable high-voltage multilevel inverter. A string series of capacitors is used to separate the single DC bus used by the diode clamped multilevel inverter (DCMLI) into many voltage levels. To block a voltage level of Vdc/(m-1), where m is the number of levels, each active switching device is sufficient; however, to block the reverse voltage, the clamping diodes must have different voltage ratings. For every stage, you'll need (m-1)*(m-2) diodes. With this value, we can see that m has increased quadratically. The system becomes unworkable as the number of levels grows due to the exponential growth in the number of diodes. When designing a high-voltage, high-power inverter using the pulse width modulation (PWM) approach, the reverse recovery of the clamping diodes becomes the most significant challenge.

3. MULTI-CARRIER PULSE-WIDTH MODULATION SCHEMES

To generate specified voltage levels at the output terminals of different MLI topologies, the well-known multi-carrier pulse-width modulation (MC-PWM) schemes give the basic switching states [19]. The primary goal of a pulse width modulation (PWM) scheme is to reduce load side filter units by converting

low-order harmonics to high-order harmonics. Reduced effects on the output voltage, near-sinusoidal RMS voltage, little filtering, and so on are all results of low levels of high-order harmonics relative to low-order harmonics. Both basic or low switching frequency, known as voltage-pulse approaches, and high switching frequency, known as multi-carrier modulation schemes, are often used to operate conventional VSIs and MLI topologies [30], [31]. During a single operation, these basic or low switching frequency systems need components with a high commutation frequency and have limited controllable features. One reference signal and many carrier signal transformations are required to provide practical switching states in an appealing high-switching-frequency-based modulation system. One triangular carrier signal and one sinusoidal reference signal are needed by the sinusoidal pulse-width modulation (S-PWM) scheme, the most important system [32]. Both the reference and carrier signals are related to each other by using a relational operator for attaining a feasible switching pattern controlled by the modulation index mci. The index represents the controlled magnitude at output terminals based on the relation of the amplitude of the reference signal (Vr) and carrier signals (Vcr), which varies from 0<mci<1.

The modulation index is expressed as (1).

$$m_{ci} = \frac{V_r}{V_{ar}} \ (m_{ci} \leq 1) \tag{1}$$

The output staircase voltage relies on this modulation index concerning the input DC voltage, as shown in (2).

$$V_o = m_{ci} * V_{dc} \tag{2}$$

Where, V_dc represents the input DC voltage or a combination of many DC inputs, m_ci represents the modulation index ratio. The multi-carrier pulse-width modulation schemes are divided based on the frequency range of the carrier signal; the high switching frequency type plays a more significant role over the fundamental frequency type. The output staircase voltage relies on this modulation index concerning the input DC voltage, as shown in (2).

3.1. Level-shifted pulse-width modulation (LS-PWM) scheme

Level-shifted modulation technique (LS-PWM) is the second most important multi-carrier modulation method [24]. Its concept is “transforming the several carrier signals with amplitude”. All LS-PWM triangular carrier signals have identical frequency ratios but varying peak amplitudes based on voltage levels [33]. The operation of LS-PWM is the same as phase-shifted, except that the carrier signals are arranged according to the PD, POD, and APOD schemes. Figure 2 shows that phase disposition (PD) modulates all carrier signals. Phase opposition disposition (POD) modulation techniques mean that the carrier signals above the zero line of the sinusoidal modulating waveform are 180° out of phase, compared with the carrier signal below the zero line shown in Figure 3. Alternative phase opposition disposition (APOD), modulation techniques mean that each carrier signal is phase shifted by 180° from its adjacent carriers as shown in Figure 4. Several applications are studied, and attractive multi-carrier modulation methods are implemented. This study evaluates the suitability of LSPWM for controlling the output voltage of a DCMLI topology-supplied PMSM motor drive. Figures 5-7 depict a modulation signal carrier-based PWM on several techniques, including PD, POD, and APOD [34].

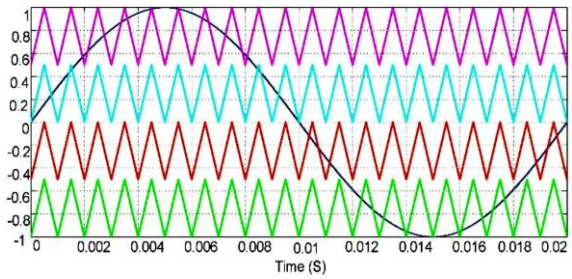

Figure 2. Phase disposition (PD) modulation technique for five-level DCMLI

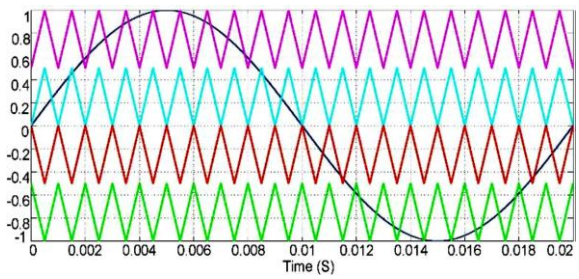

Figure 3. Phase opposition disposition (pod) modulation technique for five-level DCMLI

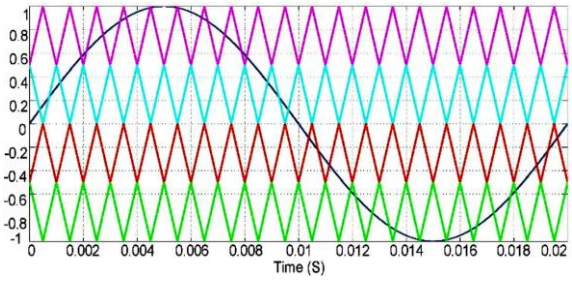

Figure 4. Alternative phase opposition disposition (APOD) modulation technique for five-level DCMLI

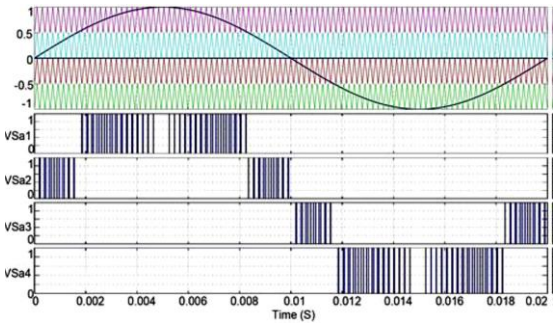

Figure 5. Modulation signal of SPWM inverter on PD modulation technique

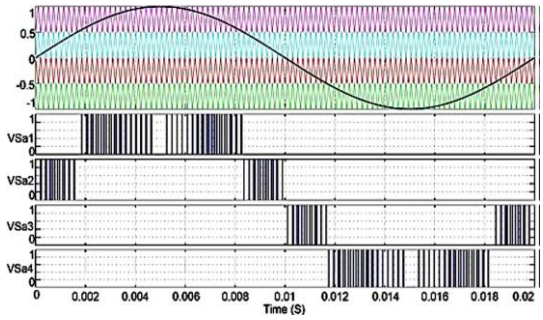

Figure 6. Modulation signal of SPWM inverter on POD modulation technique

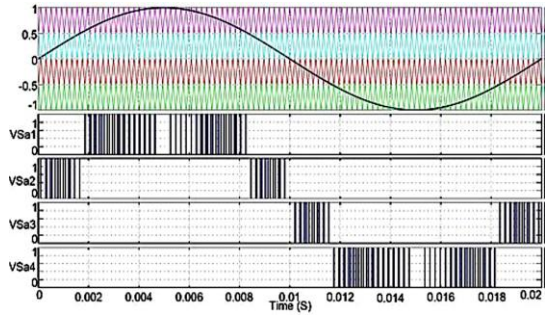

Figure 7. Modulation signal of SPWM inverter on APOD modulation technique

4. 5-LEVEL DCMLI TOPOLOGY FOR PMSM DRIVE

Figure 8 shows a 5-level DC-MLI structure. For the accurate current path (n-1)×(n-2), basic 5-level DCMLI architecture requires 2(n-1) positive and/or negative section switches: Sr1/Sr1', Sr2/Sr2', Sr3/Sr3', and Sr4/Sr4'. Clamping diodes are Da1/Da1', Da2/Da2', Da3/Da3', and DC-link source is (n-1) capacitors. Output voltage levels determine DC-link voltage Vdc. Series-integrated DC-link capacitors Cr4 and Cr3, in the bottom portion, and Cr2 and Cr1 for a 5-level output voltage are distinguished by a common neutral point (N). Synthesized output voltage wave-shape Vout had five levels: 0 Vdc, Vdc/4, -Vdc/4, Vdc/2-Vdc/2, and neutral point (N).

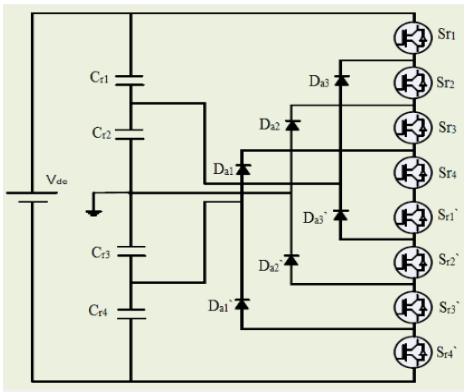

Figure 8. Configuration of 5-level DC-MLI topology

Table 1 shows the ideal switching states for 5-level DC-MLI. The staircase 5-level output voltages are synthesized at load terminals between the neutral point (N) and the output node (Vo). The top switches Sr2, Sr3, and Sr4, and the bottom switch Sr1' are switched ON in the positive half-cycle for Vdc/4 at the output terminal Vo in mode-A. The top switches Sr1, Sr2, Sr3, and Sr4 are turned on in a positive half-cycle

to produce Vdc/2 at the output terminal Vo in mode B. Mode C produces 0Vdc by turning on top switches Sr3, Sr4, and bottom switches Sr1', Sr2'. In mode-D, the top switch Sa4 and bottom switches Sr1', Sr2', and Sr3' are turned on in the negative half-cycle to provide -Vdc/4 at the output terminal Vo. Using viable switching states, mode-E changes all bottom switches Sr1', Sr2', Sr3', and Sr4' on in the negative half-cycle to provide -Vdc/2 at output terminal Vo [35].

Table 1. Switching states of the 5-level DC-MLI topology

Mode	Output voltage (VO)	Conducted switches							
		S_{r1}	S_{r2}	S_{r3}	S_{r4}	S_{r1}'	S_{r2}'	S_{r3}'	S_{r4}'
Mode-A	Vdc /4	F	N	N	N	N	F	F	F
Mode-B	Vdc/2	N	N	N	N	F	F	F	F
Mode-C	0 Vdc	F	F	N	N	N	N	F	F
Mode-D	-Vdc/4	F	F	F	N	N	N	N	F
Mode-E	-Vdc/2	F	F	F	F	N	N	N	N

5. MATLAB/SIMULINK RESULTS AND DISCUSSION

Using the system characteristics shown in Table 2, the proposed 5-level DCMLI-fed PMSM motor drive's performance is assessed under both fixed and variable speed situations using the MATLAB/Simulink tool. Figure 9 shows 5-level DCMLI-supplied PMSM drive performance at constant speed. That is 5-level DCMLI output voltage (Figure 9(a)), stator current (Figure 9(b)), rotor speed 9 Figure 9(c)), electromagnetic torque (Figure 9(d)), rotor angle (Figure 9(e)), 5-level output voltage THD analysis (Figure 9(f)), and stator current THD analysis (Figure 9(g)). DCMLI topology staircase 5-level output voltage is 500V directly supplied to the PMSM motor drive, which consumes 10 A sinusoidal stator current. PMSM speed is continuous to attain the 3000-rpm reference speed. The PMSM drive starts with 9 N-m of torque and subsequently stabilizes at 5 N-m of rated electromagnetic torque. PMSM drive rotor angle is measured by Hall sensors at 6.282 rad/sec, indicating 360º consecutive rotation, enhancing drive system stability [36]. Due to the staircase 5-level voltage wave-shape from the DCMLI interface with reduced harmonic content and low-range filtering circuits, the 5-level DCMLI THD analysis is 26.36% [37]. The stator current THD analysis is 0.28%, within IEEE-519/1992 limits.

In the proposed 5-level diode-clamped multilevel inverter (DCMLI), the input DC link voltage of 500 V is divided across the DC-link capacitors. Consequently, the phase output voltage is not equal to the full DC-link voltage, but rather a fraction of it, depending on the switching state. Specifically, i) The maximum phase voltage of the 5-level DCMLI is ±(Vdc/2), i.e., ±250 V; ii) The output shown in Figure 9(a) corresponds to the phase voltage, not the line-to-line voltage; and iii) The line-to-line voltage available at the motor terminals satisfies the required RMS voltage for the PMSM operation. Therefore, the inverter is operating within its designed voltage limits, and the PMSM receives the appropriate effective voltage required for rated operation. The motor speed and torque responses shown in Figure 9 are obtained through proper modulation of the inverter output frequency and voltage, not by exceeding the rated DC-link voltage.

Table 2. Operating parameters

S. No	Operating parameters	Values
01	Input DC voltage	Vin-500 V
02	PMSM motor drive	Rated voltage-500 V; Current-10 A; Rated power: 5 KW Torque-5 N-m Stator resistance-18.7 Ω
03	Carrier frequency	15.05 KHz

Figure 10 shows the 5-level DCMLI-fed PMSM drive performance under varied speeds. DCMLI's 5-level output voltage of 500 V, and the PMSM motor drive's 10 A sinusoidal stator current remains constant under varying speed circumstances. To reach the reference speed, the PMSM speed is adjusted with time: 2000 rpm at t-0 sec and 3500 rpm at t-0.25 sec. The PMSM drive starts with 9 N-m of torque and subsequently stabilizes at 5 N-m of rated electromagnetic torque. PMSM drive rotor angle is measured by Hall sensors at 6.282 rad/sec, indicating 360º consecutive rotation, enhancing drive system stability. Due to the staircase 5-level voltage wave-shape from the DCMLI interface with reduced harmonic content and low-range filtering circuits, the 5-level DCMLI THD analysis is 24.87% [38]. The stator current THD analysis is 0.88%, within IEEE-519/1992 limits.

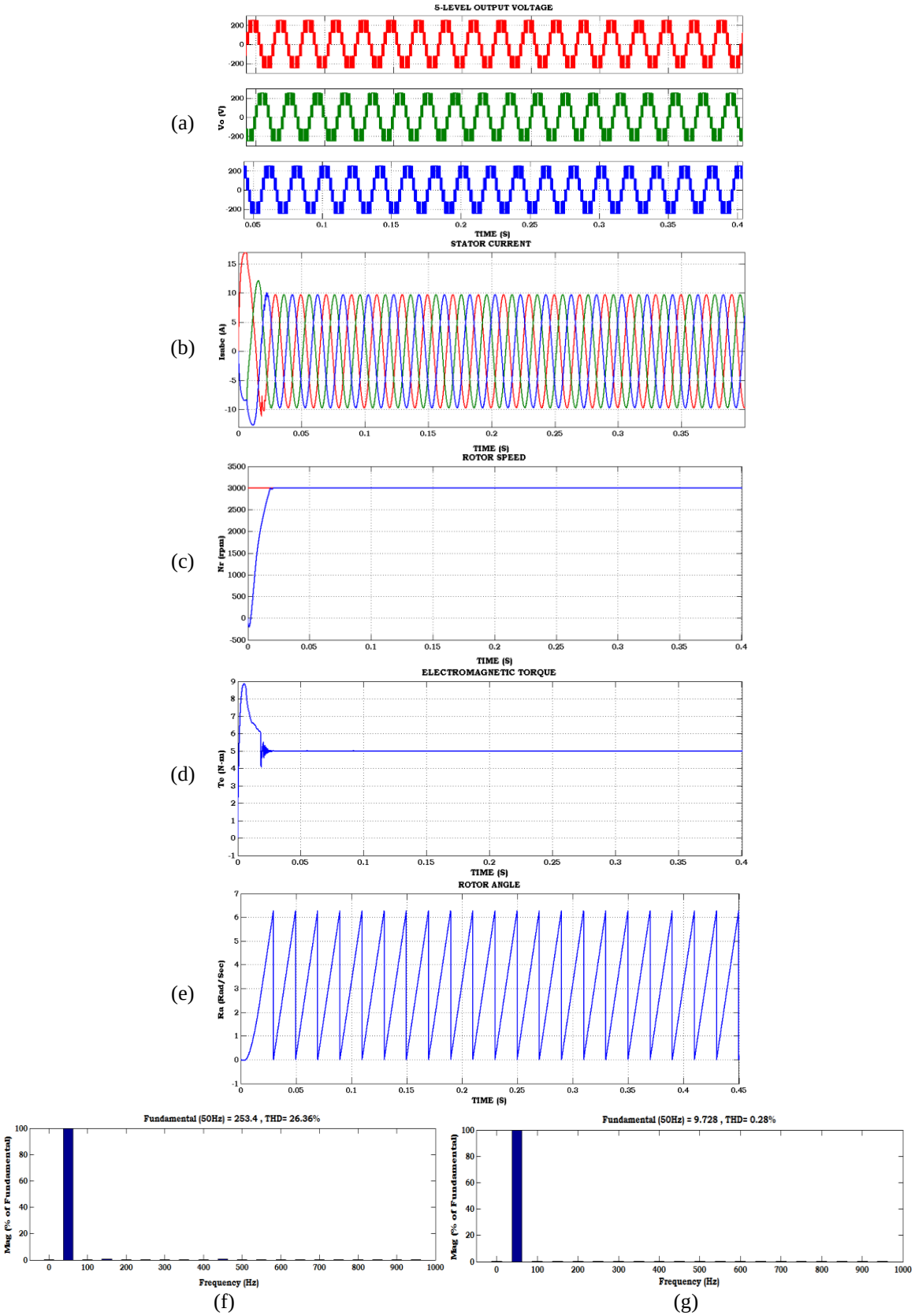

Figure 9. Simulation results of 5-level DCMLI-fed PMSM drive under constant speed condition: (a) 5-level DCMLI output voltage, (b) stator current, (c) rotor speed, (d) electromagnetic torque, (e) rotor angle, (f) THD analysis of 5-level DCMLI output voltage, and (g) THD analysis of stator current

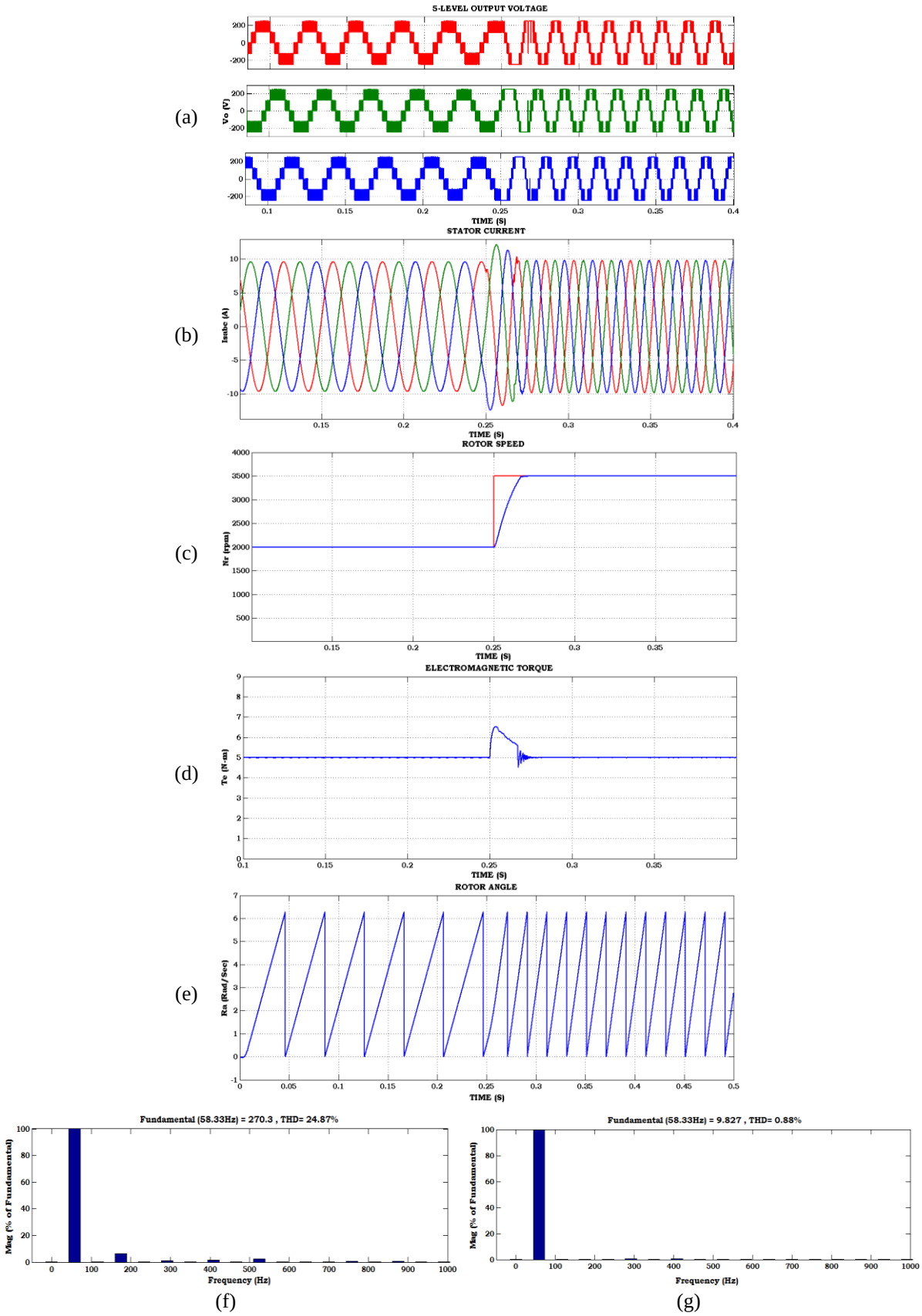

Figure 10. Simulation results of a 5-level DCMLI-fed PMSM drive under variable speed conditions: (a) 5-level DCMLI output voltage, (b) stator current, (c) rotor speed, (d) electromagnetic torque, (e) rotor angle, (f) THD analysis of 5-level DCMLI output voltage, and (g) THD analysis of stator current

Table 3 compares the THD of 3-level VSI and 5-level DCMLI topologies fed a PMSM drive at a constant speed. Because quasi-square wave voltage uses high-range filtering units, 3-level output voltage THD is 67.13%, and stator current THD is 0.51%, which is considerably higher than the above suggested 5-level DCMLI topologies. Since the staircase voltage wave-shape uses low-range filtering units, the 5-level output voltage THD is 26.36%, and the stator current THD is 0.28%, which is low compared to 3-level VSI topologies. Table 4 compares THD of 3-level VSI, 5-level, and 7-level DCMLI topologies fed a PMSM drive at changing speed. The THD of the 3-level output voltage is 67.61%, and the stator current is 0.88%, which is high for the suggested 5-level DCMLI topologies because quasi-square wave voltage uses high-range filtering units. Since the staircase voltage wave-shape uses low-range filtering units, the 5-level output voltage THD is 24.87%, and stator current THD is 0.52%, which is low compared to 3-level VSI topologies. Figures 11 and 12 show a graphical view of the comparison of various topologies under constant speed and variable speed conditions, respectively.

Table 3. THD comparison of traditional 3-level VSI and proposed 5-level DCMLI topologies fed PMSM drive under constant speed condition

THD (%)	Traditional 3-level VSI	Proposed 5-level DCMLI
Output Voltage	67.13%	26.36%
Stator Current	0.51%	0.28%

Table 4. A comparison of 3-level VSI and 5-level DCMLI topologies for fed PMSM drives operating at variable speeds

THD (%)	Traditional3-level VSI	Proposed 5-Level DCMLI
Output voltage	67.13%	26.36%
Stator current	0.51%	0.28%

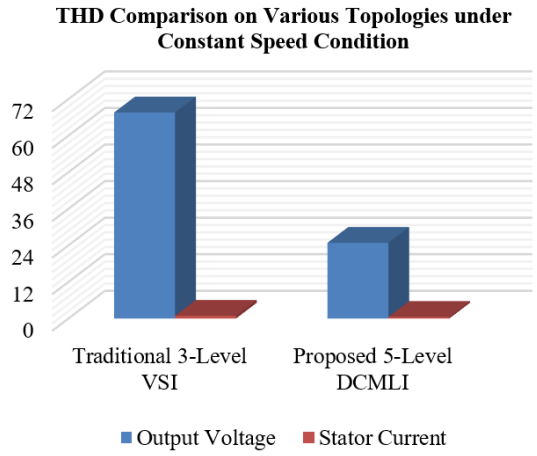

Figure 11. Graphical view of THD comparison on various topologies under constant speed conditions

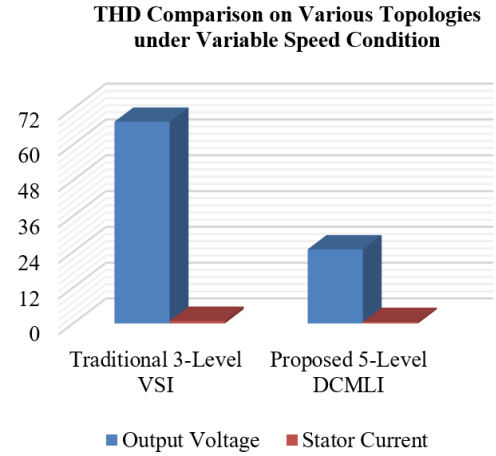

Figure 12. Graphical view of THD comparison on various topologies under variable speed conditions

6. CONCLUSION

In conclusion, a 5-level diode-clamped multilevel inverter (DCMLI) is proposed to improve the performance of permanent magnet synchronous motor (PMSM) drives in water-pumping irrigation systems with an intermediary VSI interface. Unlike the conventional 3-level VSI, which produces a quasi-square waveform at the PMSM terminals and suffers from high harmonic distortion, extensive LC filter requirements, high switching losses, low efficiency, and significant dv/dt stress, the proposed 5-level DCMLI topology creates a staircase-shaped waveform with improved characteristics.

The total harmonic distortion (THD) analysis under constant and variable speed conditions reveals significant improvements. Under constant speed, the THD in the output voltage decreases from 67.13% with the traditional 3-level VSI to 26.36% with the proposed 5-level DCMLI, while the THD in the stator current reduces from 0.51% to 0.28%. These reductions demonstrate the enhanced harmonic performance of the proposed topology.

Simulations conducted using MATLAB/Simulink validate that the proposed 5-level DCMLI topology achieves low harmonic content, reduced switching loss, minimized dv/dt stress, a smaller range of required LC filter units, and improved efficiency. Additionally, the system's THD for both stator current and output voltage complies with IEEE-519/1992 standards. The recommended 5-level DCMLI, employing the level-shifted pulse width modulation (LSPWM) technique, offers substantial benefits over the conventional 3-level VSI architecture for PMSM drives in water-pumping applications, optimizing both operational stability and efficiency.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

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K. B. Anilkumar	✓		✓	✓	✓					✓	✓			

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

Data availability does not apply to this paper as no new data were created or analyzed in this study.

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