Optimal gating angles for a three-phase 60 Hz voltage source multi-level inverter based on intelligent algorithms

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ABSTRACT

The three-phase multi-level inverter is considered one of the main power sources in industrial applications as well as in renewable energy applications. Therefore, researchers are interested in improving the efficiency of the inverter by reducing the total harmonic distortion (THD) value to its lowest limits. Also, one of the factors for improving the efficiency of the inverter is reducing the number of switches used, as it contributes to reducing the resulting losses. This research resorts to using many optimal algorithms to find the optimal values for the inverter gating angles that ensure reducing the THD value, as well as using a suitable topology with a least number of switches. The research used five algorithms known for their accuracy and efficiency, genetic algorithm (GA), gray wolf optimization (GWO), particle swarm optimization (PSO), slime mould algorithm (SMA), and whale optimization algorithm (WOA) separately. Then, extracting the distinctive characteristics of these algorithms in a hybrid curve and using it in driving the three-phase multi-level inverter (MLI) with 31 levels. The research displays the voltages and currents of the inverter as well as the frequency analysis for three-phase inductive load resulting from simulating the inverter using MATLAB software.

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1. INTRODUCTION

Multi-level inverter (MLI) is widely used within high power and medium voltages, and this requires a combination of several factors to obtain high efficiency for the system [1]. First, numerous DC sources are necessary to generate the required multiple levels in the output waveform. Therefore, the challenge is to use the least number of these DC sources and simultaneously securing the required voltage levels [2]. The output waveform's multiple levels are accomplished by adding or subtracting these DC sources from each other at each step. The second factor relates to the number of power switches used. These switches provide paths for the electrical currents through continuous opening and closing. The fewer the switches, the less electrical power is wasted, which reduces the total loss of the inverter and contributes effectively to higher efficiency. The most critical third factor is selecting the optimal switching times for the operation of the switches [3]. Hence, this requires complex algorithms to find the optimal switching times to operate these power switches. Optimal timing effectively contributes to diminishing the total harmonic distortion (THD) in the inverter output waveform. Lower THD is important to comply with the grid standards. The race is now on how to find the best multi-level inverter circuit topology that has the fewest DC sources and the fewest number of switches. After that, the optimal switching time to operate the power switches can be obtained by using intelligent algorithms [4]. The algorithms can contribute to reducing the total harmonic distortion in the output waveform MLI. The output waveform consists of staircase-like levels, and when analyzed further with the Fourier series, it results in a set of trigonometric harmonic equations accompanying the fundamental harmonic. The inverter switching times depend on the modulation index. To find the optimal switching times, intelligent algorithms can be used. These algorithms result in different THD values associated with a particular value of (m). This paper aims to address the above-mentioned research problems currently found in three-phase MLIs i.e., to deploy the minimal number of DC sources, to use the minimum number of power switches, and to apply intelligent algorithms to get minimum THDs for a broad spectrum of modulation indices. This research concentrates on designing a 3-phase MLI composed of thirty-one levels and optimal gating angles derived from genetic algorithms (GA), gray wolf optimization (GWO), particle swarm optimization (PSO), slime mould algorithm (SMA), and whale optimization algorithm (WOA). Ultimately, the research studies indicate that the stepped wave MLI is the best way to obtain reduced THD values, and the success lies in using the best methods to control the operation of the inverters. The stages of operation for different control methods are presented and the solution of the trigonometric equations accompanied with stepped wave output of MLI are explained.

2. METHOD

This section describes the design and implementation of a 3-level three-phase MLI used as a three-phase voltage source with a minimum number of DC sources and switches, reducing the power losses and enhancing efficiency. The control method relies on selective harmonic elimination based on intelligent algorithms to achieve minimum percentage values of THD. The implementation of 31-level three-phase inverter for MATLAB simulation starts with writing the trigonometric equations for selective (targeted) harmonic elimination (SHE) to get the optimal solution of the optimal angles using the five selected algorithms, i.e. GA, GWO, PSO, SMA, and WOA. The next step is to select the optimal angles from the appropriate algorithm based on the hybrid optimization curve. These optimal angles are used as gate signals to power switches to simulate the 31-level three-phase inverter.

2.1. Three-phase 31-level MLI topology

The first stage includes designing a basic unit for single-phase MLI as shown in Figure 1. In general, the basic unit can provide $2^n - 1$ levels, where n is the number of DC sources. For instance, if n=2, then the basic unit provides 2^2-1 = 3 levels for the positive half cycle of the inverter output voltage, and similarly another 3 levels for the negative half cycle, hence a total of 7 levels for one electrical cycle (the zero level is repeated) as shown in Figure 2.

The basic unit can be extended to provide any required level. For example, to get 15 levels, two basic units are put together with 4 DC sources, i.e. $2^4 - 1$=15 levels per half cycle are generated as depicted in Figure 3, making 31 levels in one complete cycle. The output voltage waveform has a stepped waveform, and each step represents the value of V_{DC}. To obtain a 31-level voltage waveform from a single-phase MLI, the magnitude of the DC sources is set as V_{DC}, 2 V_{DC}, 5 V_{DC}, and 10 V_{DC}, respectively, as shown in Figure 4. The process of addition and subtraction of these DC sources will result in 31 levels, including the zero level of the voltage output from the inverter [5].

The theory of Fourier series for a stepped periodic function can be presented by (1) [6].

$$v_0(t) = \frac{a_o}{2} + \sum_{k=0}^{n} a_n \cos(nwt) + b_n \sin(nwt) \tag{1}$$

Where a_o, represents the average value of the output voltage, a_n and b_n, are even and odd parameters of the staircase periodic signal, respectively. The stepped waveform exhibits a quarter wave symmetry which establishes a_o , a_n and the even b_n values to zero and modifies in (1) to (2).

$$v_0(t) = \sum_{i=1,3,5,7,9,11\ldots\ldots}^{n} b_n \sin(nwt) \tag{2}$$

Where b_n is found to be (3).

$$b_n = \frac{4V_{dc}}{n\pi} \sum_{k=1,3,5,7,9,11\ldots\ldots}^{m} \cos(n\,\Phi_k) \tag{3}$$

In three-phase systems, the triplen harmonics (3^{rd},9^{th}, 15^{th}, 21^{st}, and 27^{th}) are eliminated implicitly. The (3) is to be solved for the optimized 15 angles of 31-level MLI to eliminate the explicit 14 harmonics (5^{th}, 7^{th}, 11^{th}, 17^{th}, 19^{th}, 23^{rd}, 25^{th}, 29^{th}, 31^{st}, 35^{th}, 37^{th}, 41^{st}, and 43^{rd}).

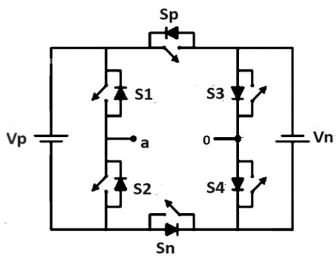

Figure 1. Basic unit of the inverter

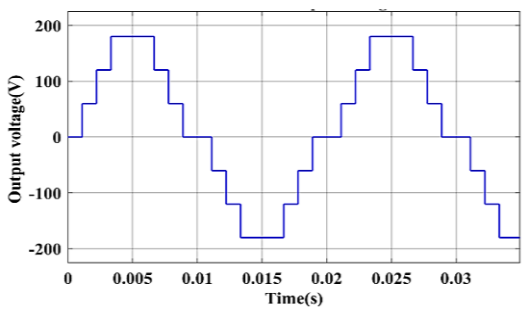

Figure 2. 7-level voltage waveform

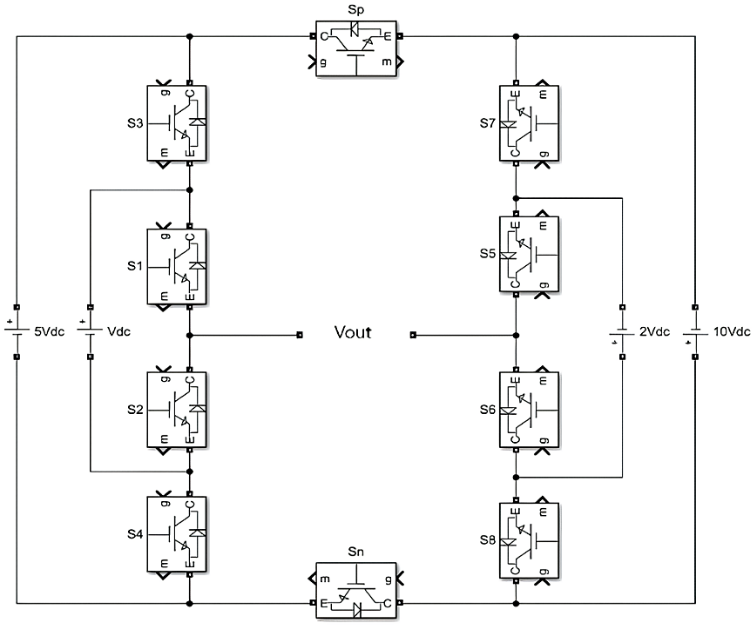

Figure 3. 31-level single-phase inverter

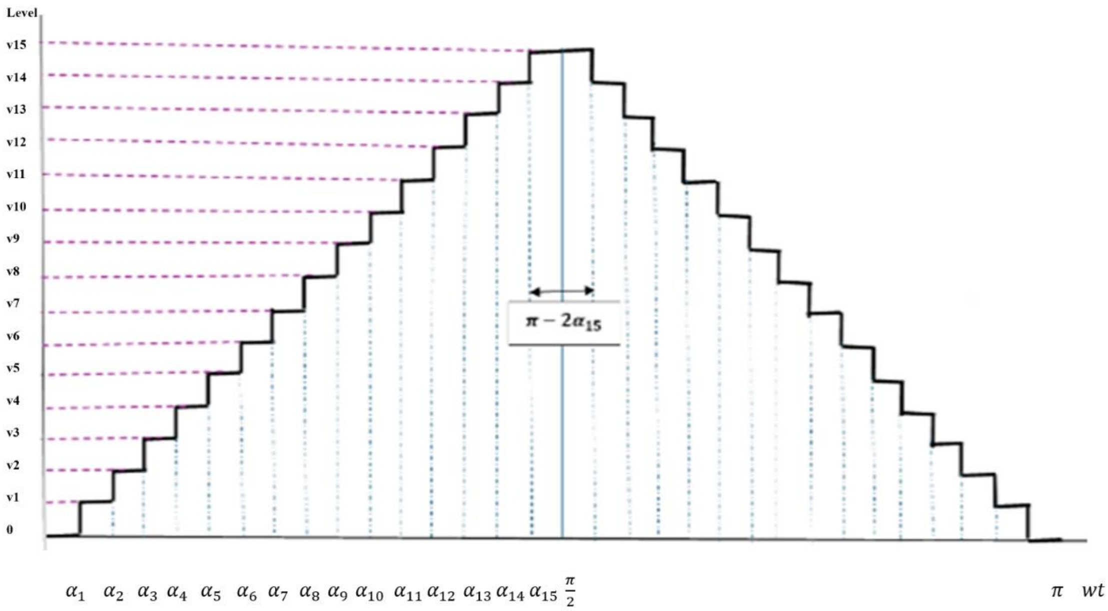

Figure 4. 31-level stepped waveform

2.2. Optimization techniques

Five algorithms known for their efficiency and widely used in practical applications in the multi-level inverter field, namely genetic algorithm (GA) [7]-[11], gray wolf optimization (GWO) [12]-[16], particle swarm optimization (PSO) [17]-[22], slime mould algorithm (SMA) [23]-[28], and whale optimization algorithm (WOA) [29]-[33] are calculated for finding the optimal gating angles of the power switches for whole range of modulation index (m), 0<m<1. Figure 5 shows the MATLAB calculated optimized angles for GA, while THD% vs modulation index for GA is shown in Figure 6. THD% is between 4% to 13%, approximately, depending on the value of the modulation index. Figure 7 shows the MATLAB calculated optimized angles for GWO. THD% vs modulation index for GWO is shown in Figure 8. THD% is between 2% to 24%, approximately, depending on the value of the modulation index. MATLAB calculated optimized angles for PSO are shown in Figure 9, while Figure 10 shows THD% vs modulation index for PSO. THD% is between 3% to 22%, approximately, depending on the value of the modulation index.

The optimized angles calculated by MATLAB for SMA are shown in Figure 11. THD% vs modulation index for SMA is shown in Figure 12. THD% is between 2% to 28%, approximately, depending on the value of the modulation index. Figure 13 shows the MATLAB calculated optimized angles for WOA and Figure 14 shows THD% vs modulation index for WOA. THD% is between 2.5% to 14%, approximately, depending on the value of the modulation index. An optimal hybrid curve (OHC) is derived from the five algorithms, i.e. GA, GWO, PSO, SMA, and WOA by taking the lowest value of the THD% for a specific value of modulation index as shown in Figure 15. This optimal relationship is employed to calculate the fifteen angles corresponding to every value of the modulation index.

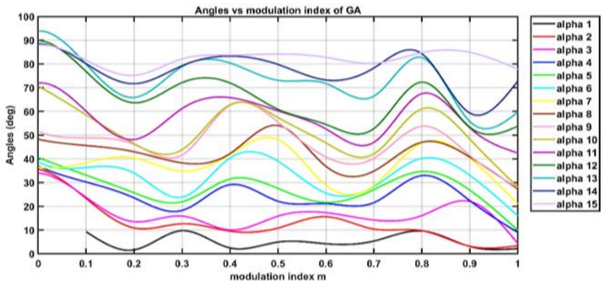

Figure 5. Angles vs m for GA

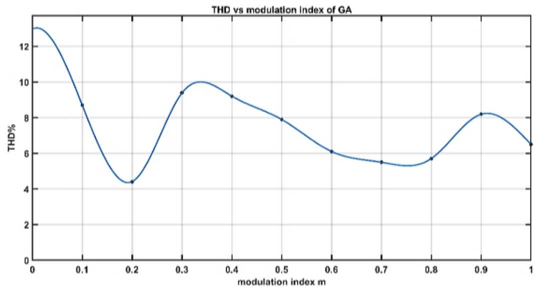

Figure 6. THD% vs m for GA

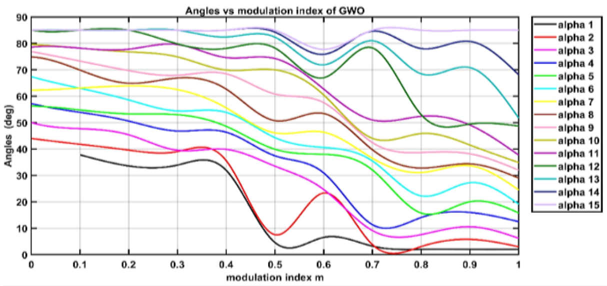

Figure 7. Angles vs m for GWO

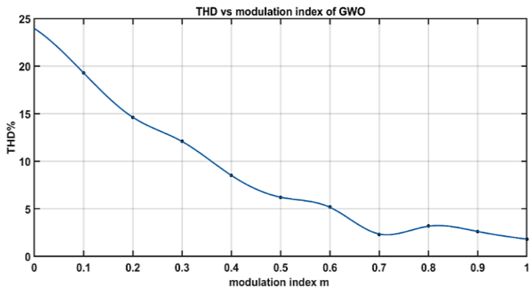

Figure 8. THD% vs m for GWO

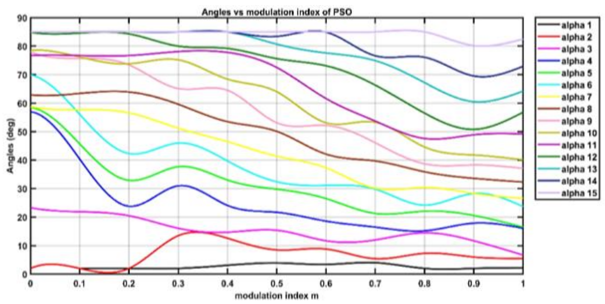

Figure 9. Angles vs m for PSO

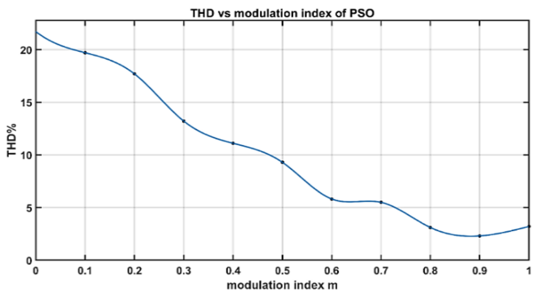

Figure 10. THD% vs m for PSO

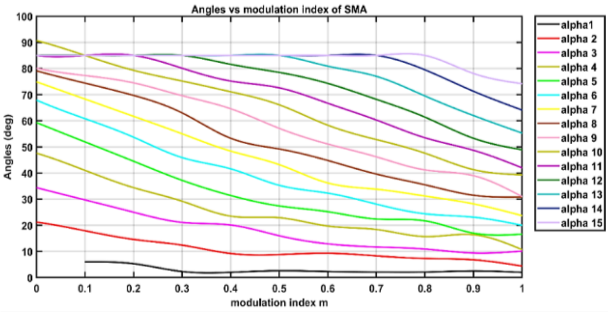

Figure 11. Angles vs m for SMA

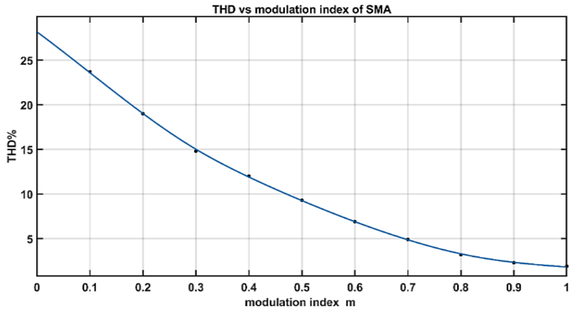

Figure 12. THD% vs m for SMA

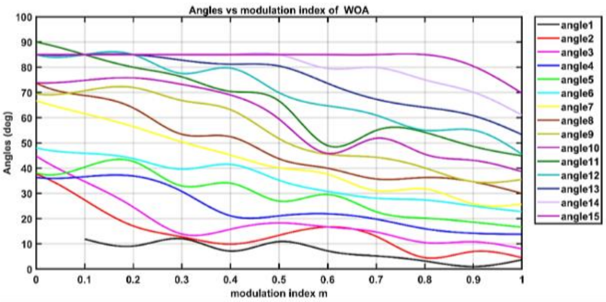

Figure 13. Angles vs m for WOA

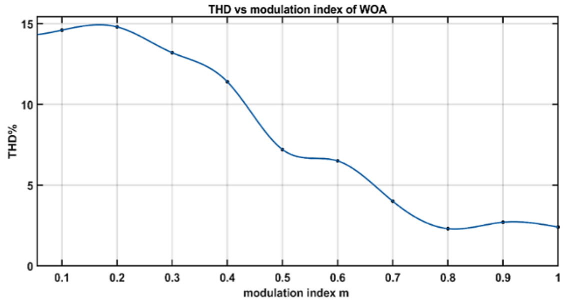

Figure 14. THD% vs m for WOA

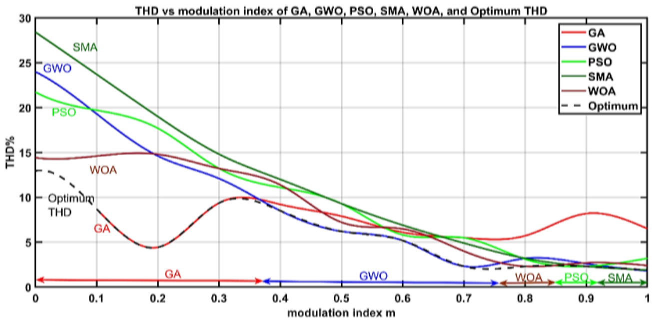

Figure 15. Optimal hybrid curve derived from GA, GWO, PSO, SMA, and WOA vs THD%

According to the chosen modulation index the user can index the appropriate algorithm from the OHC which assures the lowest THD% for the given modulation index as tabulated in Table 1. One of the five algorithms can be adopted according to the range of m to be used as depicted in Table 2. This is to ensure that minimum THD% is always achievable at the MLI output.

Table 1. THD% values achieved using OHC versus individual algorithms

Algorithm	Modulation index									
	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1
GA	9	4.2	9.8	9.7	8	6	5.8	5.9	8.1	6.8
GWO	19	14.9	12.5	9	6	5	2.4	3.8	2.8	2.3
PSO	19.8	17.2	13.8	10.9	9.8	5.9	5.3	3.9	2.5	3.8
SMA	24	19	15	12.5	9.8	7.5	5	3.8	1.2	0.9
WOA	14.8	15	13.8	11.9	7.2	6.1	4.8	2.5	3	2.6
OHC	9	4.2	9.8	9	6	5	2.4	2.5	1.2	0.9

Table 2. Modulation index range vs algorithm used

Modulation index range	Algorithm used	Modulation index range	Algorithm used
0-0.38	GA	0.86-0.92	PSO
0.39-0.75	GWO	0.93 -1	SMA
0.76-0.85	WOA		

3. RESULTS AND DISCUSSION

3.1. MATLAB Simulink simulation

To obtain the output voltage of the three-phase inverter with 31 levels, Table 3 is prepared, which represents the state of the switches for the positive half-cycle. For the negative half-cycle, a phase difference of 180° is added. The required tables for the three phases are prepared, considering the 120° difference between the three phases.

A proposed three-phase 31 multi-level inverter (MLI) is star connected as shown in Figure 16 with 12 DC sources and 30 IGBT's ensuring the least possible loss of power resulting from the on-off operation of these switches. The three-phase inverter is simulated in the MATLAB program and the Simulink model for the switches gating of the positive half cycle of phase A is shown in Figure 17. Figure 18 represents the 120° phase difference between the three phases, while Figure 19 shows the gating angles for the S1, S3, S5, S7, and S9 switches for phase A, which represents the complements of S2, S4, S6, S8, and S10, respectively. These switches operate with different frequencies according to Table 3. To simulate a 60 Hz power source with phase voltage V_{rms} = 120 V, these DC voltage sources are used: VDC =12 V, 2 V_{DC} = 24 V, 5 V_{DC} = 60 V, and 10 V_{DC} =120 V.

Table 3. Phase A switches states for the positive cycle

S1 S2 *	S3 S4 *	S5 S6 *	S7 S8 *	S9 S10 *	Level	Duration	DC sources
1	1	1	1	1	0	Φ_1	No DC source
0	1	1	1	1	1	$\Phi_2-\Phi_1$	V_1
1	1	0	1	1	2	$\Phi_3-\Phi_2$	V_2
0	1	0	1	1	3	$\Phi_4-\Phi_3$	$V_{1+}V_2$
1	0	1	1	1	4	$\Phi_5-\Phi_4$	V_5-V_1
0	0	1	1	1	5	$\Phi_6-\Phi_5$	V_5
1	0	0	1	1	6	$\Phi_7-\Phi_6$	$V_5+V_2-V_1$
0	0	0	1	1	7	$\Phi_8-\Phi_7$	V_5+V_2
1	1	1	0	1	8	$\Phi_9-\Phi_8$	$V_{10}-V_2$
0	1	1	0	1	9	$\Phi_{10}-\Phi_9$	$V_{10}-V_2+V_1$
1	1	0	0	1	10	$\Phi_{11}-\Phi_{10}$	V_{10}
0	1	0	0	1	11	$\Phi_{12}-\Phi_{11}$	$V_{10}+V_1$
1	0	1	0	1	12	$\Phi_{13}-\Phi_{12}$	$V_{10}-V_2-V_1+V_5$
0	0	1	0	1	13	$\Phi_{14}-\Phi_{13}$	$V_{10}-V_2+V_5$
1	0	0	0	1	14	$\Phi_{15}-\Phi_{14}$	$V_{10}-V_1+V_5$
0	0	0	0	1	15	$\pi-2\Phi_{15}$	$V_{10}+V_5$
1	0	0	0	1	14	$\Phi_{15}-\Phi_{14}$	$V_{10}-V_1+V_5$
0	0	1	0	1	13	$\Phi_{14}-\Phi_{13}$	$V_{10}-V_2+V_5$
1	0	1	0	1	12	$\Phi_{13}-\Phi_{12}$	$V_{10}-V_2-V_1+V_5$
0	1	0	0	1	11	$\Phi_{12}-\Phi_{11}$	$V_{10}+V_1$
1	1	0	0	1	10	$\Phi_{11}-\Phi_{10}$	V_{10}
0	1	1	0	1	9	$\Phi_{10}-\Phi_9$	$V_{10}-V_2+V_1$
1	1	1	0	1	8	$\Phi_9-\Phi_8$	$V_{10}-V_2$
0	0	0	1	1	7	$\Phi_8-\Phi_7$	V_5+V_2
1	0	0	1	1	6	$\Phi_7-\Phi_6$	$V_5+V_2-V_1$
0	0	1	1	1	5	$\Phi_6-\Phi_5$	V_5
1	0	1	1	1	4	$\Phi_5-\Phi_4$	V_5-V_1
0	1	0	1	1	3	$\Phi_4-\Phi_3$	$V_{1+}V_2$
1	1	0	1	1	2	$\Phi_3-\Phi_2$	V_2
0	1	1	1	1	1	$\Phi_2-\Phi_1$	V_1
1	1	1	1	1	0	Φ_1	No DC source

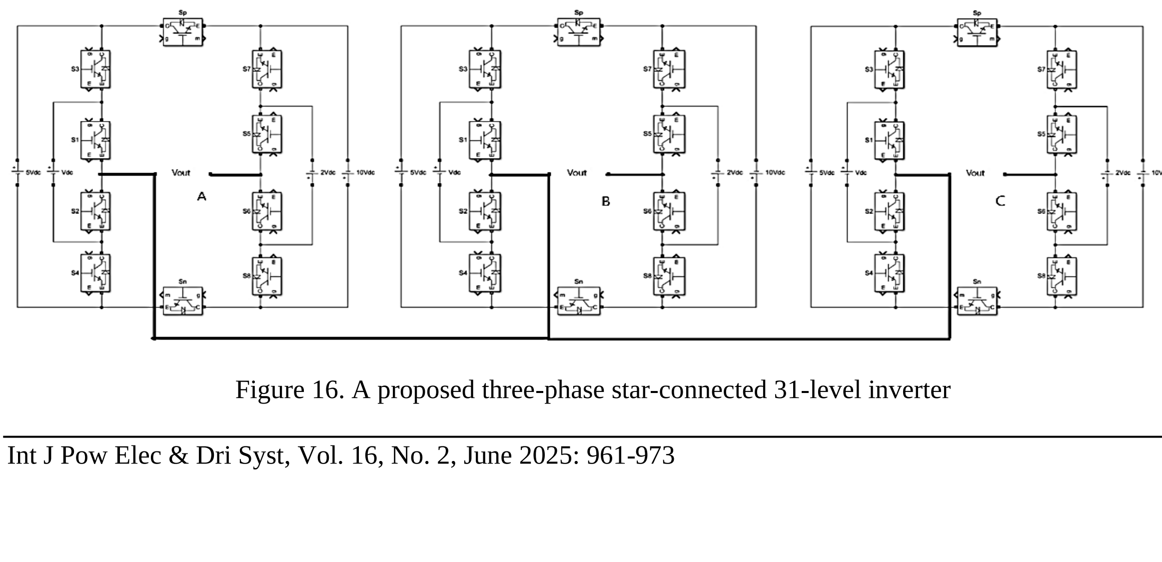

Figure 16. A proposed three-phase star-connected 31-level inverter

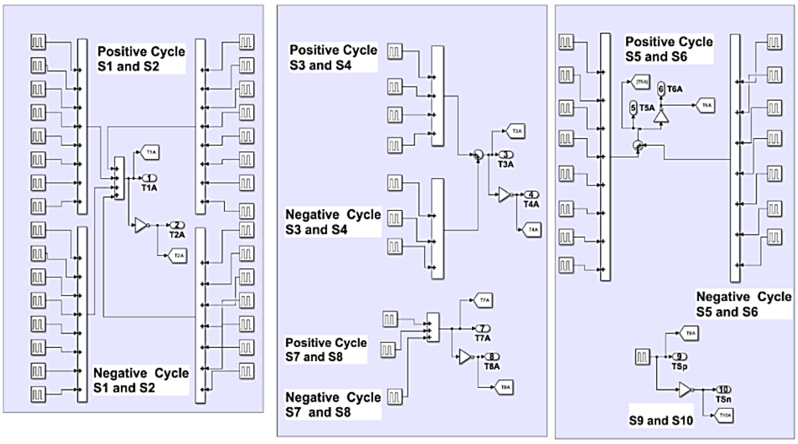

Figure 17. Simulink model for the switch gating of the positive half cycle of phase A

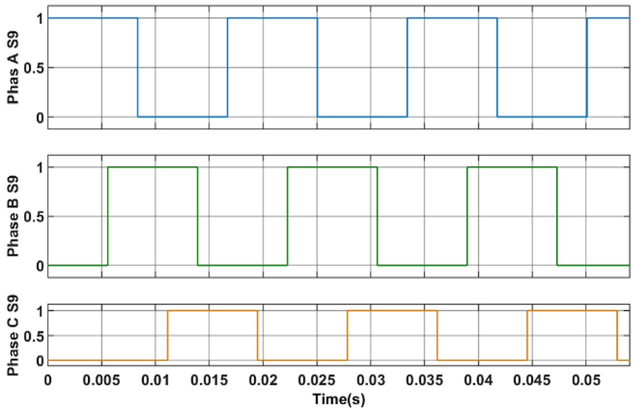

Figure 18. 120° phase difference between the three phases

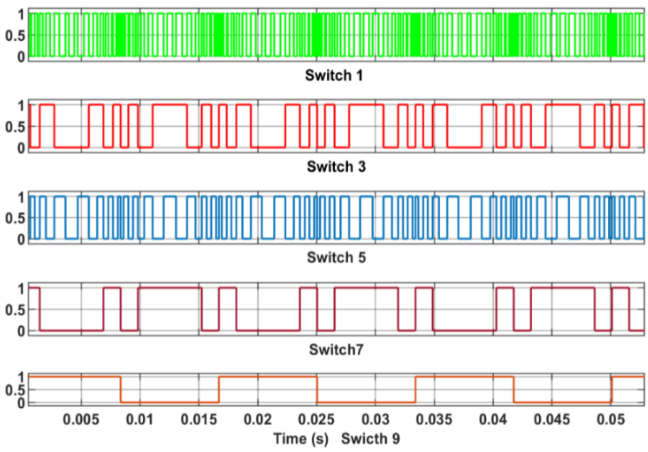

Figure 19. Gating angles for the ten power switches for phase A

Figure 20 shows the three-phase voltages, where the phase difference between the three phases is noted. Figure 21 shows the line voltages. The phase difference between the phase voltage and the line voltage is 30° as shown in Figure 22. The current drawn from the inductive load (R = 5 Ω, L = 20 mH) is illustrated in Figure 23. The current waveform is very close to a typical sine wave.

The phase difference between the phase voltage and current caused by the inductive load is shown in Figure 24. The neutral current I_n is very close to zero, which supports the precise operation of the three-phase inverter, as shown in Figure 25. To measure the THD of voltages and currents, the FFT tool in

MATLAB is used. Figure 26 shows THD% = 4.71% for the phase voltage, THD% = 4.05% for the line voltages are shown in Figure 27, and THD% = 0.72% for the load current is illustrated in Figure 28. These THD% are considered low values according to the standard IEEE 519-2014 permissible values for the voltage range $V \leq 1.0\ kV$ is 12%. The more angles, the lower values of THD% are obtained.

To test the three-phase inverter for dynamic loads, the inverter is loaded with a three-phase asynchronous motor with 460 V, 60 Hz specifications. To adjust the values of the DC sources to suit the characteristics of the motor the following DC sources are employed V_{DC} = 24 V, 2 V_{DC} = 48 V, 5 V_{DC} = 120 V, and 10 V_{DC} = 240 V. Figures 29 and 30 show the phase and line voltages suitable to drive three-phase dynamic loads.

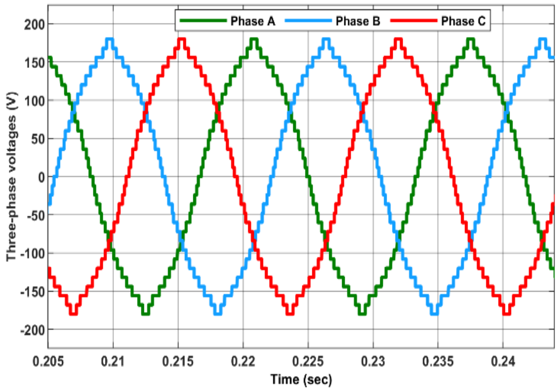

Figure 20. Three-phase voltages of the 31-level MLI

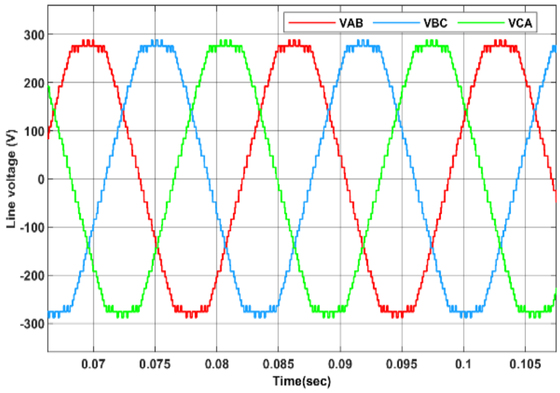

Figure 21. Three-line voltages of the 31-level MLI

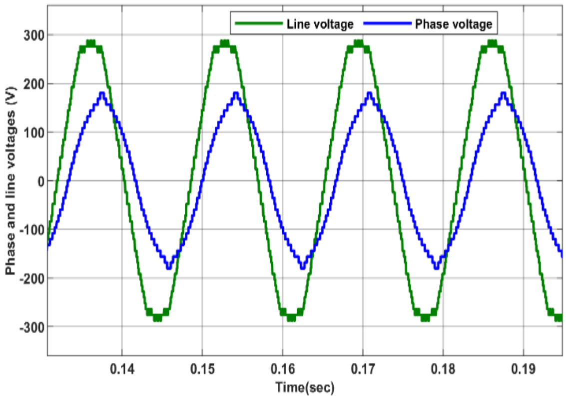

Figure 22. Phase difference phase-line voltages (RL load)

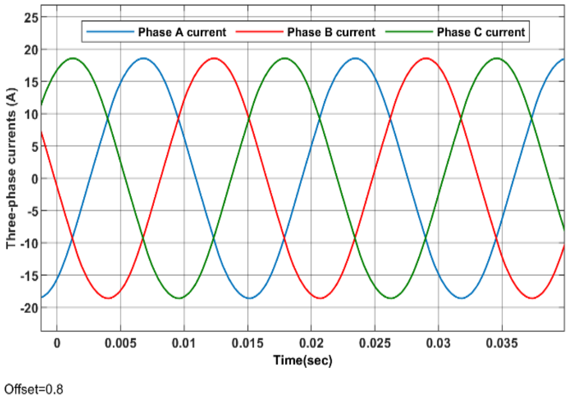

Figure 23. Three-phase current (RL load)

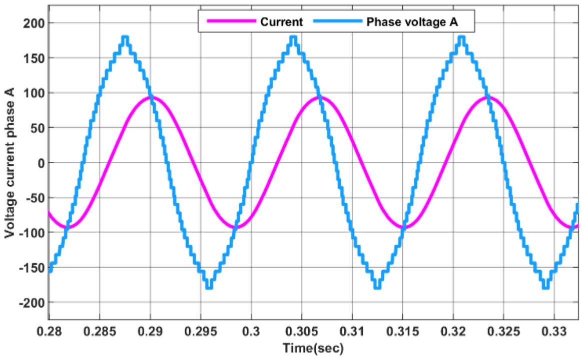

Figure 24. Phase difference voltage and current (RL load)

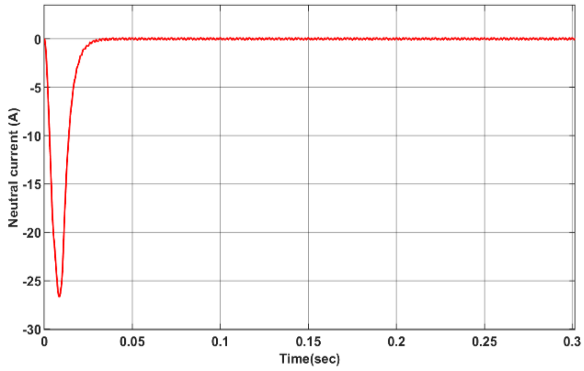

Figure 25. Neutral current I_n

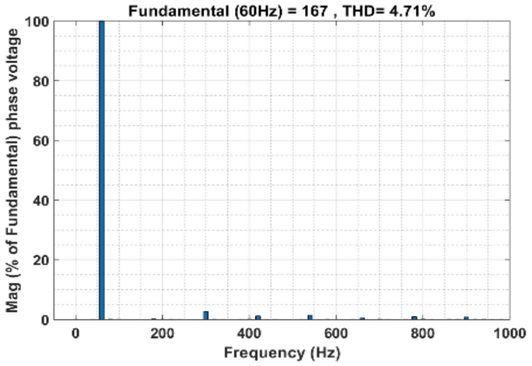

Figure 26. Phase voltage THD%

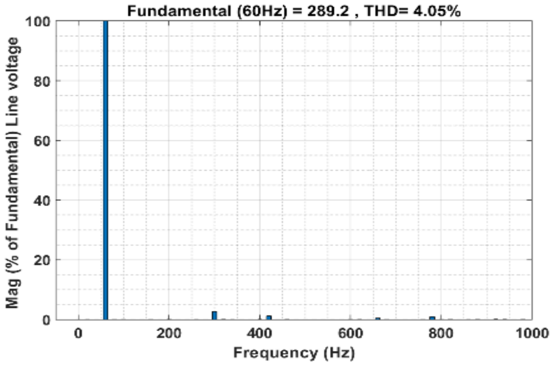

Figure 27. Line voltage THD%

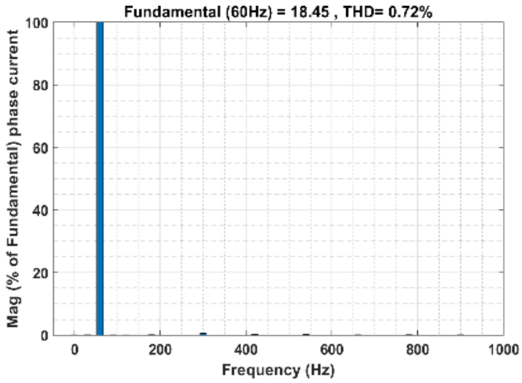

Figure 28. Load current THD% (RL)

The motor speed, electromagnetic torque, and current drawn are monitored. The motor is subjected to an external torque at 0.5 (sec) and 0.8 (sec) of the running time in succession. A fast response of all the mentioned variables is observed. Finally, the motor lost its speed at the timing 1 (sec) after being subjected to an external torque higher than the motor operating specification, as illustrated in Figure 31.

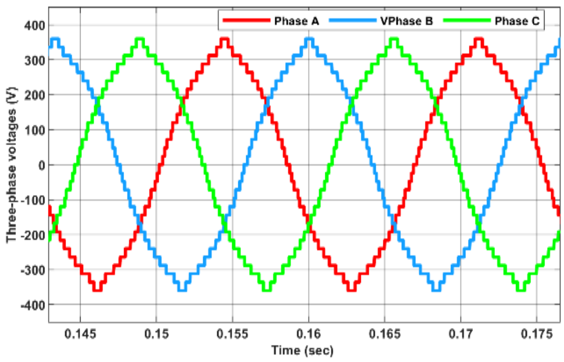

Figure 29. Three-phase 31-level MLI phase voltages

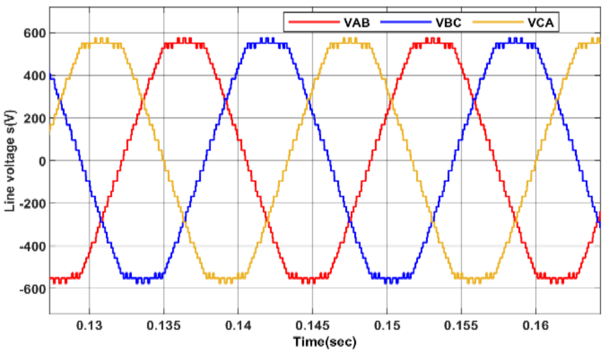

Figure 30. Three-line voltages 31-level MLI

3.2. FPGA simulation based on Spartan 3E controller

FPGA simulation utilizes the Spartan 3E controller as its processing unit. The controller operates at clock frequency of 50 MHz, resulting in a clock period of 20 ns. To complete a 60 Hz AC cycle supply at the inverter output, 833,333 clock cycles from the Spartan 3E controller are required. The gating of the thirty power transistor switches is programmed by employing the Spartan 3E by writing a program in VHDL for the 31-level three-phase MLI. Figure 32 shows the Spartan 3E simulation results, including clock frequency and the simulated pulses for the thirty power transistors. The VHDL file (UCF) indexing the addresses of the thirty output pins used to gate the thirty power transistors is shown in Figure 33. These Spartan 3E thirty-pin can be connected to the gates of the power transistors via optocouplers to build an experimental setup for a 31-multi-level inverter.

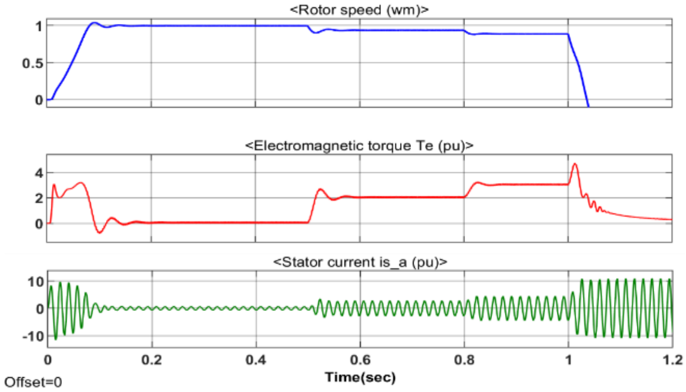

Figure 31. Rotor speed, electromagnetic torque, and stator current of the squirrel cage motor

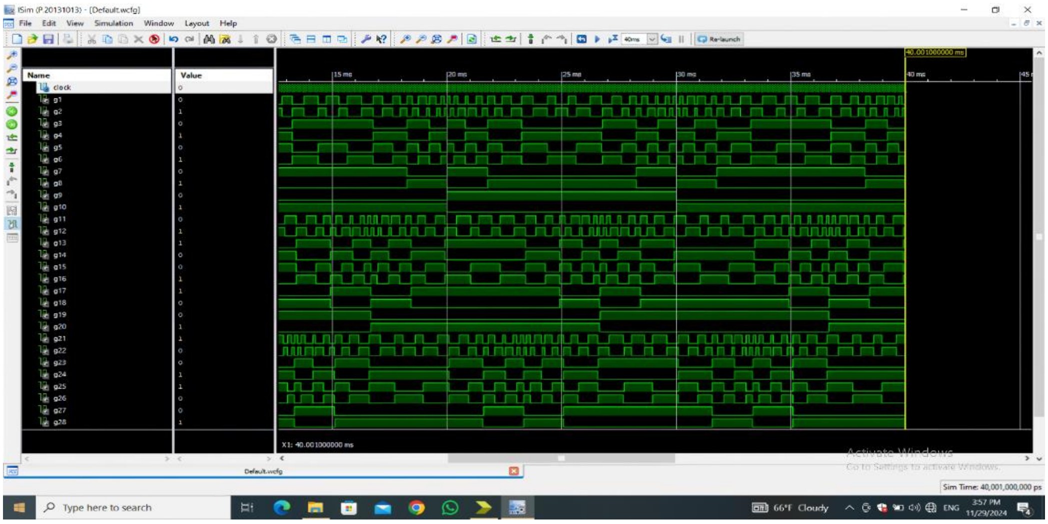

Figure 32. Clock frequency and the simulated pulses for the thirty power transistors

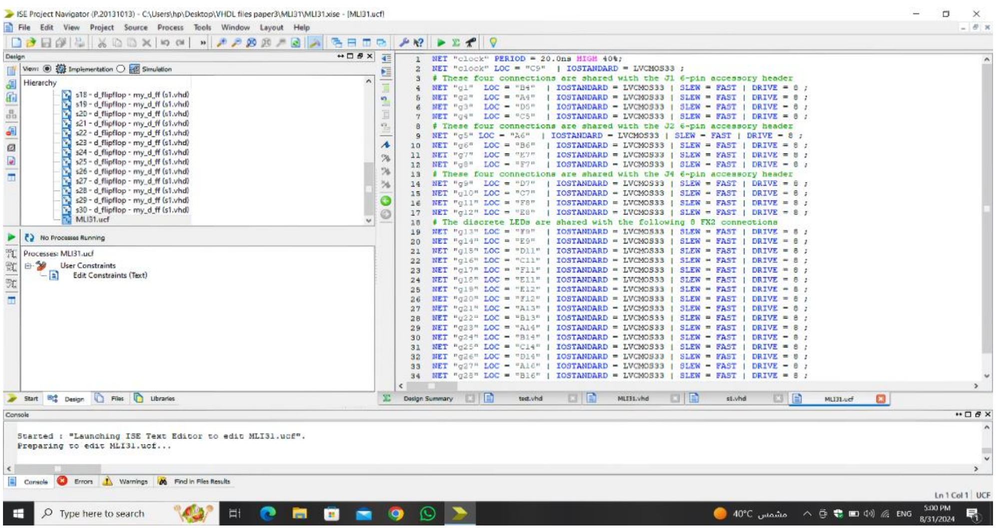

Figure 33. Addresses of the Spartan 3E output pins to gate thirty power transistors

4. CONCLUSION

The first objective is the topological design of a 3-phase inverter to be used as a 3-phase voltage source. The goal is that the design comprises the minimal number of DC sources and the least number of power switches. After an extensive review of the research related to this objective, a 31-level three-phase is designed, where the required number of DC sources for each phase are 4 sources and the required number of power switches is 10, and in total 12 DC sources and 30 power switches for the three phases. The second objective is to lower the THD value of the MLI output waveform based on intelligent optimal algorithms. The characteristics of several intelligent optimal algorithms are reviewed in section 2 and five algorithms known for their extensive use by researchers are evaluated, namely, GA, GWO, PSO, SMA, and WOA, to achieve low THD% values over a wide modulation index range (0<m<1). An optimal hybrid curve (OHC) is derived from the five algorithms i.e. GA, GWO, PSO, SMA, and WOA by taking the lowest value of the THD for a specific value of modulation index and is employed for the performance of 31-level MLI with static and dynamic loads. The third objective is to evaluate the efficiency of the proposed 31-level MLI integrated with intelligent optimization algorithms through model simulation. The thirty-one-level multi-level inverter is simulated by building a Simulink model in MATLAB using the optimal angles extracted from the hybrid optimization curve. A set of variables such as currents and voltages at the inverter output are monitored, and the frequency pattern analysis for different cases. A distinctive response to changes due to changing loads is observed, which makes the inverter reliable as a three-phase voltage source. The THD% are within 4% for inverter voltages and within 1% for the currents which is considered low values according to the IEEE standards.

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AUTHOR CONTRIBUTIONS STATEMENT

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Mohamed Salem		✓	✓		✓			✓	✓				✓	

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

The authors confirm that the data supporting the findings of this study are available within the article.

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