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Study of asymmetrical-multi level inverter using two switching angle techniques

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ABSTRACT

An inverter is a device that transforms DC power into AC power. Inverters can be categorized into single-level inverters and multilevel inverters. This paper discusses two controlled strategies—equal step angle and sinusoidal switching angle—for a multilevel inverter, highlighting their effectiveness in harmonic mitigation as the number of voltage levels increases. The simulation software used to generate 3-15 level voltage outputs is PSIM, which allows for the adjustment of switching angles based on both equal step and sinusoidal switching values. Various types of DC sources are connected to H-bridge units, with MOSFET driving signals applied via gating blocks. The study demonstrates a notable reduction in total harmonic distortion (THD) when the switching angles are altered in equal and sinusoidal steps. Initially, the output signal generates a square wave without a filter. However, after implementing an LC filter, the output voltage signal more closely resembles an AC signal, and THD values are further reduced. Additionally, the output voltage signal's fast Fourier transform (FFT) is presented.

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1. INTRODUCTION

A multi-level inverter (MLI), is a power electronics circuit that can deliver the desired alternating voltage output with adjustable voltage and frequency from a single DC source or multiple lower-level DC inputs [1]. The three-level converter [2] initiated the development of MLI. High-power industries have shown increasing interest in MLI recently [3]-[5]. By carefully arranging various voltage sources, it is possible to generate high voltages with low harmonics without the need for transformers or series-connected switches [6]. MLIs have drawn the interest of electrical engineers because of their low switching losses, high voltage capacity, high power quality, and minimal electromagnetic interference [7]-[11].

Some issues with typical MLI include the need for more semiconductor switching devices in a neutral point clamped inverter, the necessity to equalize the voltage across the capacitors in a flying capacitor design, and, in a cascaded H-bridge topology, the need higher number of sources [12], [13]. In order to overcome the problems with traditional MLI, various topologies were proposed [14]-[19]. 15-level MLI is one such topology that has been proposed [20]. This proposed topology features an asymmetrical layout of DC voltage sources and includes components like fewer switches, an assessment of a comparison with alternative topologies, the total standing voltage, and three DC sources. The topologies examined in previous research [21], [22] outline the drawbacks of the traditional Module. The topology proposed by Alishah *et al*. [22] utilizes two T-type arrangements connected in reverse and without using an H-bridge

configuration, which generates a 17-level output. In the study by Hosseinzadeh *et al*. [23], a modified H-bridge topology was created using capacitors, diodes, and DC voltage sources. The capacitors charge to double the DC voltage supply, producing several output modulation levels.

The simplest way to create an MLI is by connecting traditional inverters in parallel or series. An MLI's main purpose is to produce a desired AC voltage level from multiple DC sources, which may be unequal. The AC output typically resembles a sinusoidal waveform, but one issue with MLIs is the difficulty in achieving a sinusoidal shape regarding harmonics. The staircase waveform generated can lead to abrupt transitions, adversely impacting power quality. However, MLIs improve AC power quality by converting power in smaller voltage steps, thereby reducing harmonics. As a result, there has been significant research interest in MLIs in recent years.

MLIs have certain drawbacks, particularly the need for a large number of power switches, which complicates the design. Even when using low-voltage switches, each one requires its own gate driver and protection circuitry, making the system more expensive and complex. To address this issue, researchers have proposed innovative MLI topologies that reduce the number of power switches and DC voltage sources compared to traditional designs [24]-[28]. However, these new inverters still require many bidirectional switches to achieve an output voltage with consistent step levels.

A new topology has been suggested in [28]. That paper presents a cascaded MLI topology that increases output voltage levels while reducing driver circuits, power switches, and inverter costs. The design utilizes unidirectional power switches and has been compared to other typologies. Its performance was assessed in generating all voltage levels in a 7-level inverter configuration. However, it requires a higher total DC link voltage and an adequate multilevel modulation technique.

There are so many works on equal step angle in which the inverter produced higher total harmonic distortion (THD). There are very few works on sinusoidal switching angle, but most of the researchers in their work did not mention how to calculate the sinusoidal switching angle values, and also did not perform an experiment-based study. Most of them used MATLAB and MULTISIM. It is difficult to generate a converter using MATLAB/MULTISIM. That's why, in this research, PSIM has been used. In this article, a novel asymmetrical MLI topology is introduced, featuring fewer power electronic switches compared to traditional designs. By using a simple mathematical equation to determine the sinusoidal angle for the different levels of inverter and reducing the number of IGBTs, power diodes, and gate drivers, this proposed inverter aims to lower costs, enhance efficiency, and simplify control methods. The study focuses on designing and modeling MLIs with equal-angle switching and sinusoidal angle switching to show the comparison of THD. The study focuses on varying the sinusoidal switching angles to minimize the THD of the output voltages. The suggested design, which has between 3 and 15 levels, is tested using the PSIM software for both equal-step and sinusoidal-switching angles, and the results are confirmed with a physical hardware setup.

2. THE PROPOSED METHOD

In an MLI, identifying the switching angle, also known as the conduction angle, is crucial for generating gating signals for power-switching devices. The switching angle specifies how long a switch stays in the ON and OFF positions. There are two main techniques for utilizing the switching angle:

- Equal angle technique: This method ensures that the conduction time for each ON and OFF state is uniform across all levels.
- Sinusoidal angle technique: This approach allows for variations in the conduction time between ON and OFF states. To calculate these variations in conduction time, a specific formula (referred to as (1) is used. The formula is:

$$\theta = sin^{-1}(Vo/Vm) \quad (1)$$

The output voltage at a specific moment is represented by *Vo*, while the total output voltage is denoted as *Vm*.

The workflow outlined in Figure 1 involves several key steps. First, the appropriate type of switch, such as a MOSFET or IGBT, is selected. Next, the inverter level is determined. Following this, the circuit is designed using PSIM software, incorporating the calculated step angles for both Equal Step and Sinusoidal Switching Angle methods. The simulation is then executed to generate output waveforms. Finally, the output is analyzed to determine the fast Fourier transform (FFT) values and THD values, which are recorded in a table. This entire process is illustrated in the flow diagram.

This work presents a proposed MLI circuit consisting of four single-phase H-bridge inverter units, configured in series which as shown in Figure 2. The MLI aims to produce a specific output voltage from

four DC sources drawn from batteries: 12 V, 24 V, 36 V, and 48 V. Each unit is connected to a separate DC source. The cascaded inverter architecture connects AC terminal voltages in series, eliminating the need for voltage-clamping diodes or capacitors. Bridge units include four IRF540 MOSFET switches, identified as MOS-1, MOS-2, MOS-3, and MOS-4, with different designations for each level inverter.

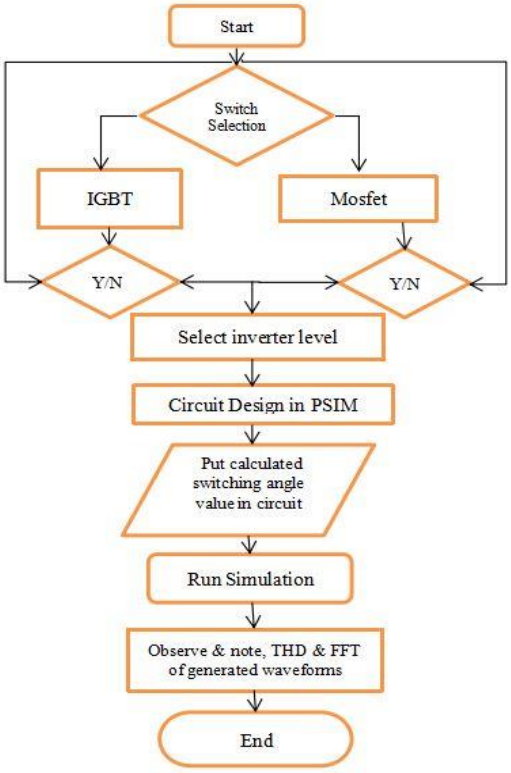

Figure 1. Flow diagram of this work

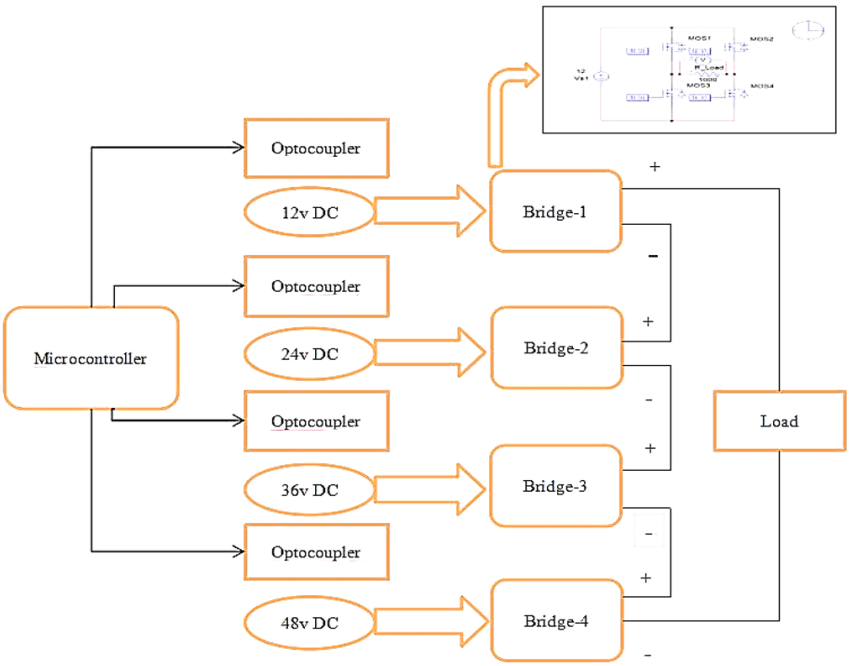

Figure 2. Flow diagram of the experimental work

An Arduino Mega 2560 micro-controller, which has a 16 MHz crystal oscillator, I/O digital pins 54, 16 analogue inputs, Connectivity of USB, a reset button and a power jack, controls this inverter system. The required control signals for the IGBT switches are generated by this micro-controller through programming. An opto-coupler is used to isolate each switch from the main power circuit. The opto-coupler receives pulses from the micro-controller via a resistor. The outputs from the four inverters are added to provide the phase output voltage, as seen in Figure 2. Three distinct voltage outputs can be produced by each inverter level by varying the combinations of the four switches connected to the AC: +Vdc, 0Vdc, and -Vdc. The output voltage of H-bridge-1 is controlled by varying combinations of four switches, with the output voltage dropping to +Vdc when switch (sw)1 and switch 4 are activated, and zero when sw3 and sw4 are turned on.

The driver circuit triggers IGBTs in the primary multilevel inverter circuit, enabling the desired multilayer output. Four IGBTs create a single-phase cascaded asymmetrical switching DC voltage source-based MLI with 3 levels of DC voltage output. An H-bridge with sixteen additional IGBTs produces 15-level AC output voltage, which is sent to the load.

3. SIMULATION METHOD

There is various simulation software available for electronic circuit simulation, including PSIM, MATLAB/Simulink, Multi-Sim, Proteus, and PS-Pice. Among these, PSIM stands out as the most suitable choice for developing and simulating power electronic circuits [23]. PSIM has several advantages over other tools:

– It is simpler to use than many other simulation programs.
– It provides faster simulation times compared to its competitors.
– Its user-friendly interface has led to its popularity in the simulation and design sector.

This study aims to implement a multilevel inverter in a real-world application, using DC source values that correspond to actual battery specifications. The schematic diagram of the 3 to 15 level inverters are shown in Figures 3 to 9.

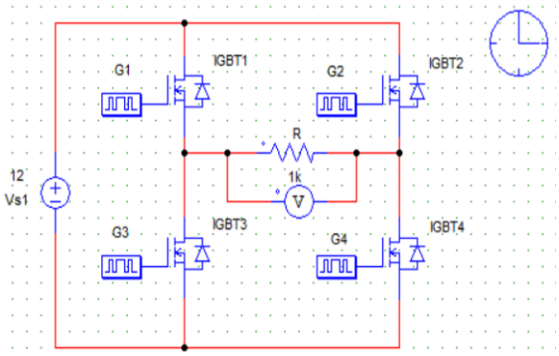

Figure 3. Circuit diagram of 3-level MLI inverter

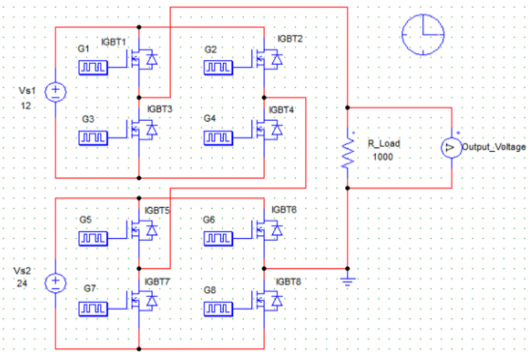

Figure 4. Circuit diagram of 5-level MLI inverter

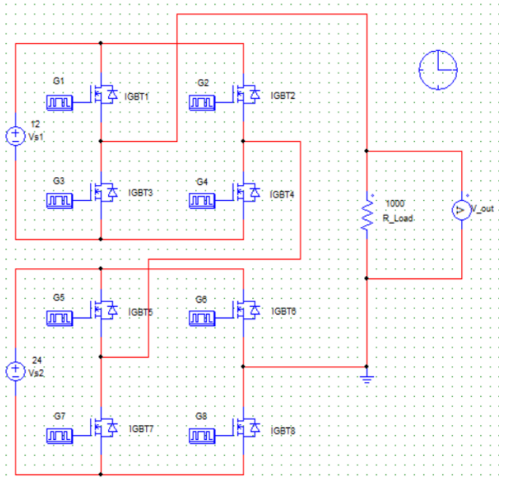

Figure 5. Circuit diagram of 7-level MLI inverter

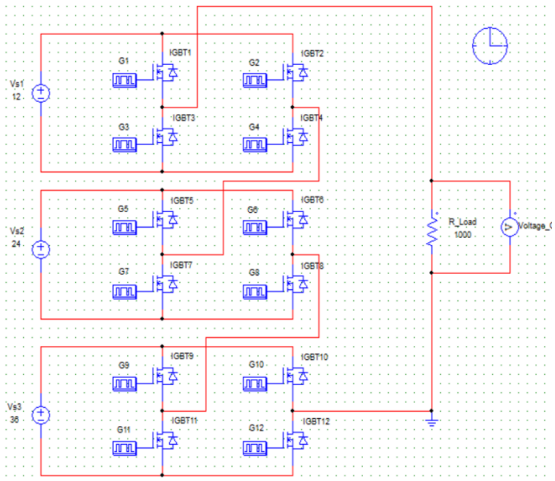

Figure 6. Circuit diagram of 9-level MLI inverter

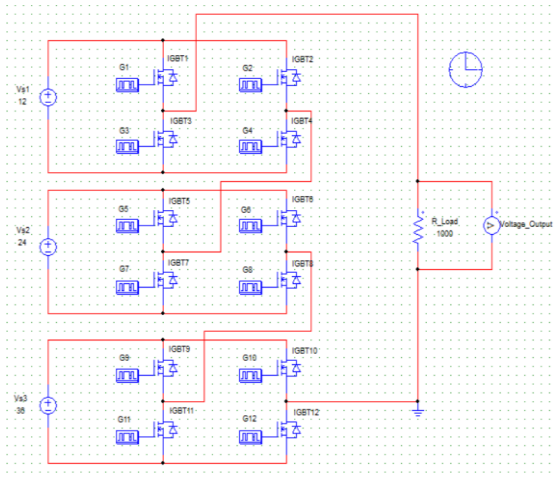

Figure 7. Circuit diagram of 11-level MLI inverter

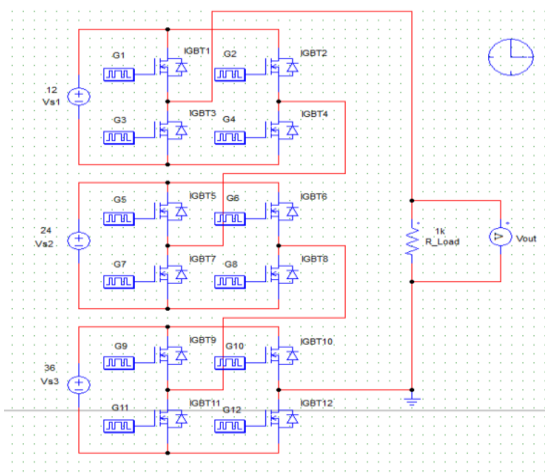

Figure 8. Circuit diagram of 13-level MLI inverter

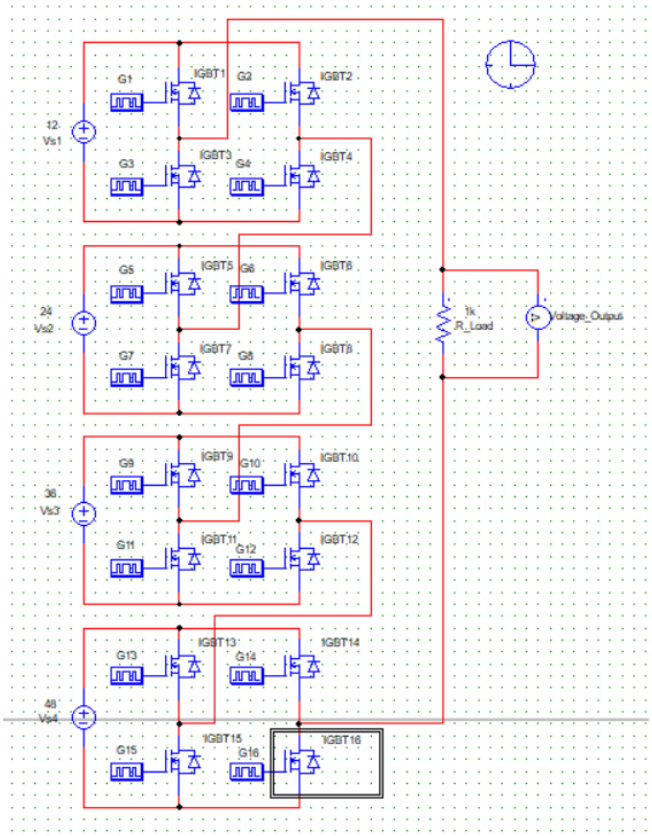

Figure 9. Circuit diagram of a 15-level MLI inverter

4. RESULTS AND DISCUSSION

PSIM software was used to simulate multi-level inverters with 3 to 15 output levels. Two switching angle strategies were applied: equal step and sinusoidal step methods. The output voltage waveforms resulting from both methods are shown in Figures 10 to 23. After applying the LC filter for both equal step and sinusoidal step, we get the values of THD, are shown in Table 1. Graphical representations of level versus percent of THD are shown in Figure 24. From this figure, it is observed that as the level is increased, the THD decreases. For an equal step angle, the decrease of THD is less than that of an equal step angle. In the case of an equal step angle, the THD decreases drastically.

Table 1. Level vs without filter vs with filter for THD values

Number of levels	THD without LC filter for equal step angle	THD with LC filter for equal step angle	THD without LC filter for sinusoidal step angle	THD with LC filter for sinusoidal step angle
3	48.31%	48.07%	37.28%	36.18%
5	28.99%	28.76%	19.88%	18.68%
7	21.63%	21.41%	15.49%	14.98%
9	18.12%	17.91%	14.15%	13.88%
11	16.29%	16.12%	13.98%	10.77%
13	15.14%	14.99%	7.12%	3.88%
15	12.11%	11.09%	6.71%	2.75%

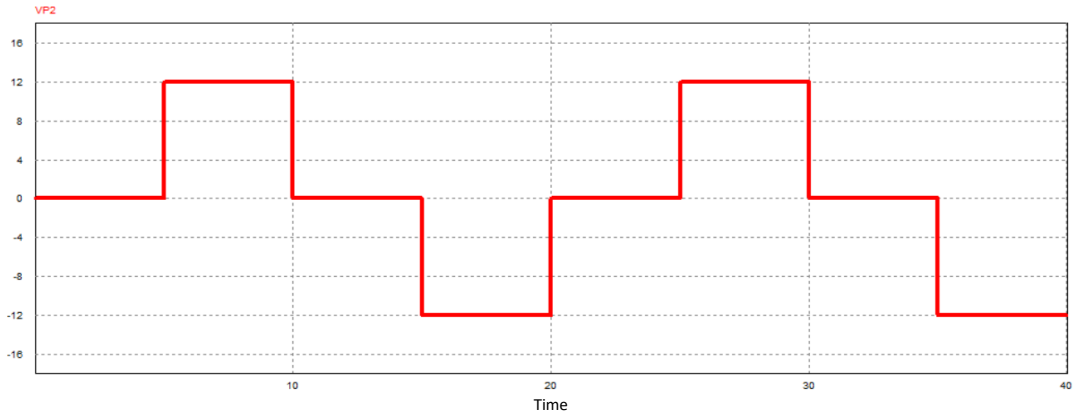

Figure 10. 3-level equal step MLI output voltage waveform

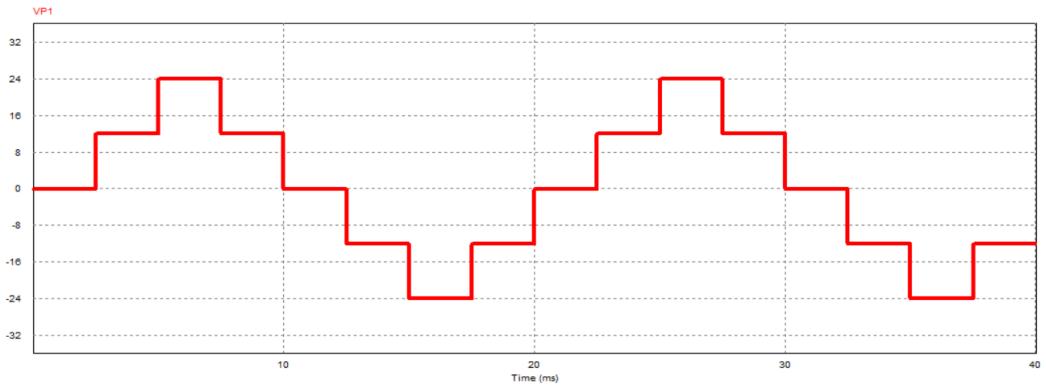

Figure 11. 5-level equal step MLI output voltage waveform

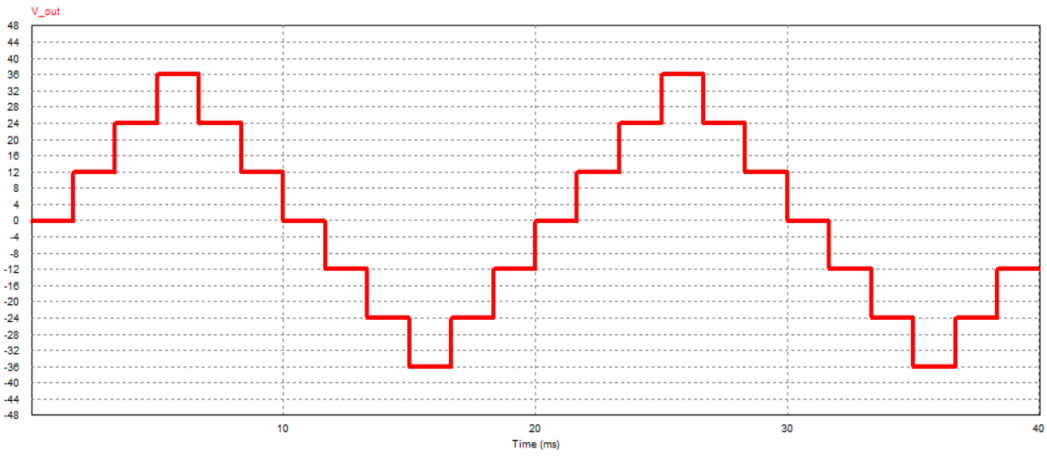

Figure 12. 7-level equal step MLI output voltage waveform

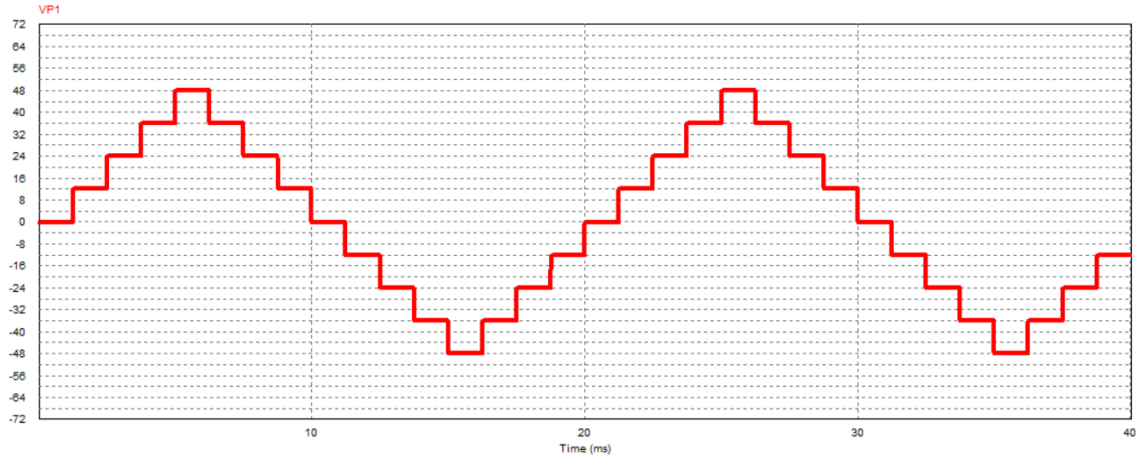

Figure 13. 9-level equal step MLI output voltage waveform

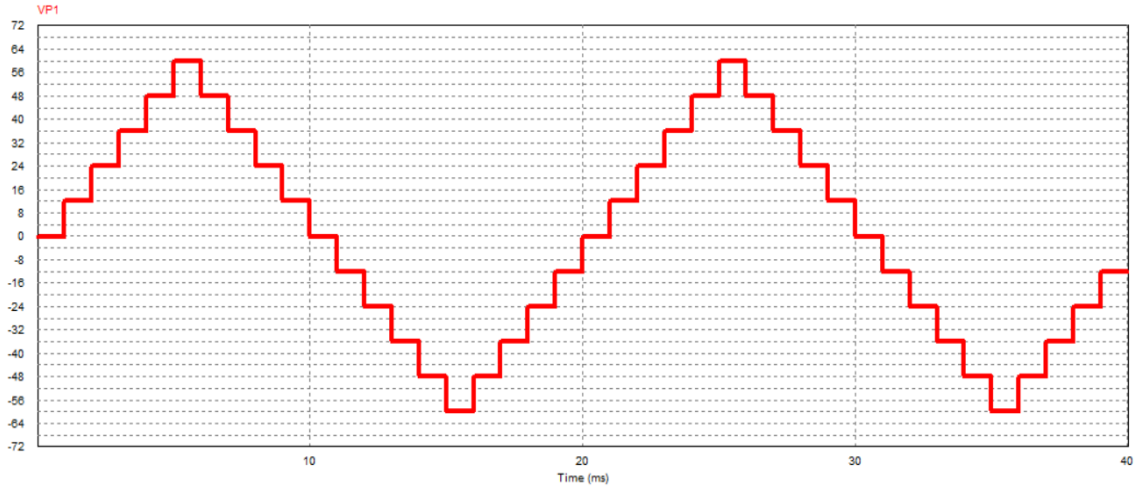

Figure 14. 11-level equal step MLI output voltage waveform

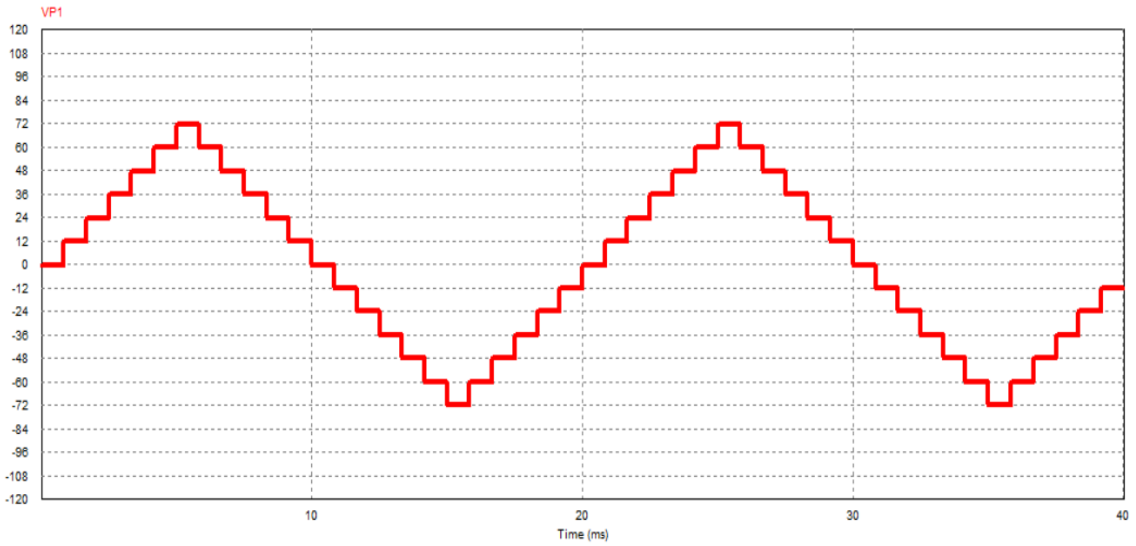

Figure 15. 13-level equal step MLI output voltage waveform

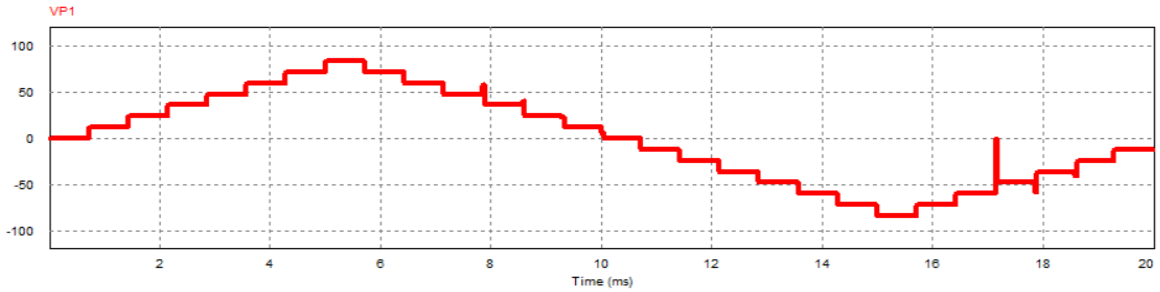

Figure 16. 15-level equal step MLI output voltage waveform

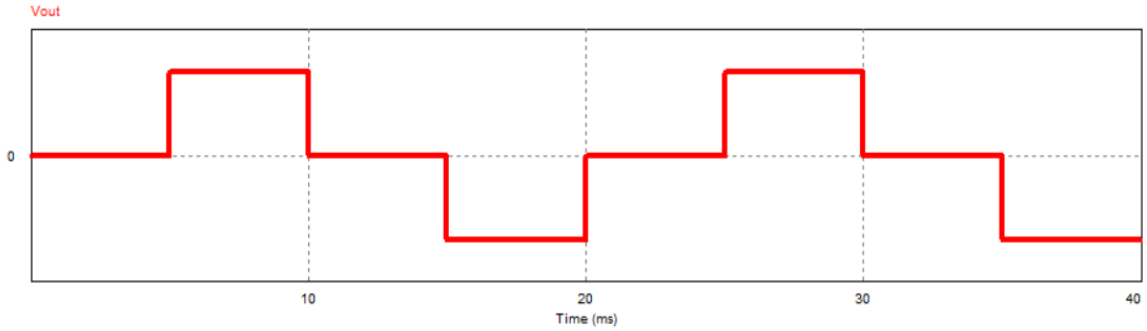

Figure 17. 3-level sinusoidal step output voltage waveform

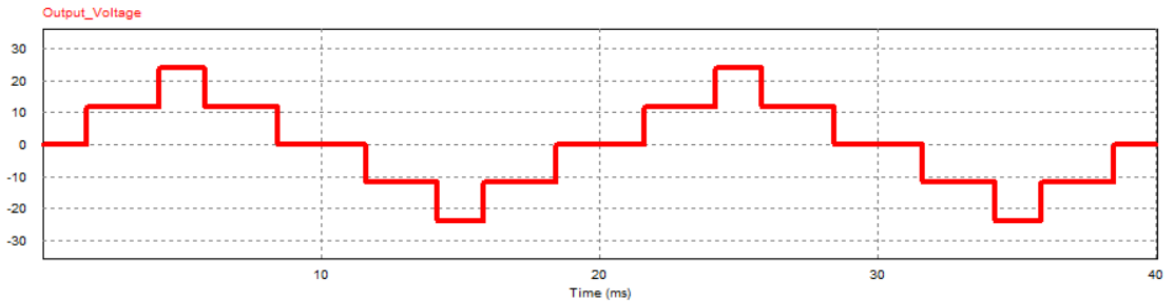

Figure 18. 5-level sinusoidal step output voltage waveform

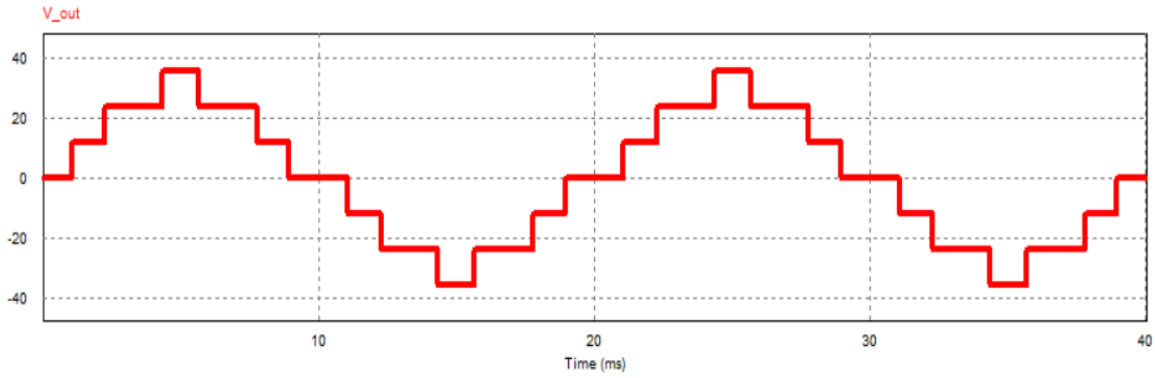

Figure 19. 7-level sinusoidal step output voltage waveform

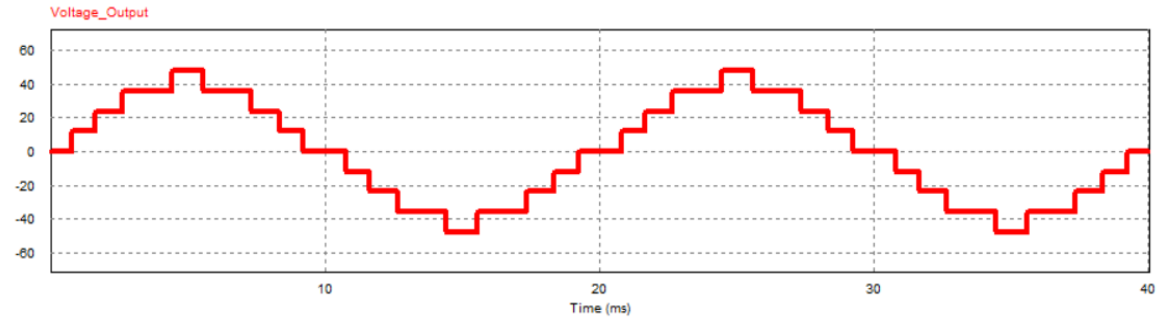

Figure 20. 9-level sinusoidal step output voltage waveform

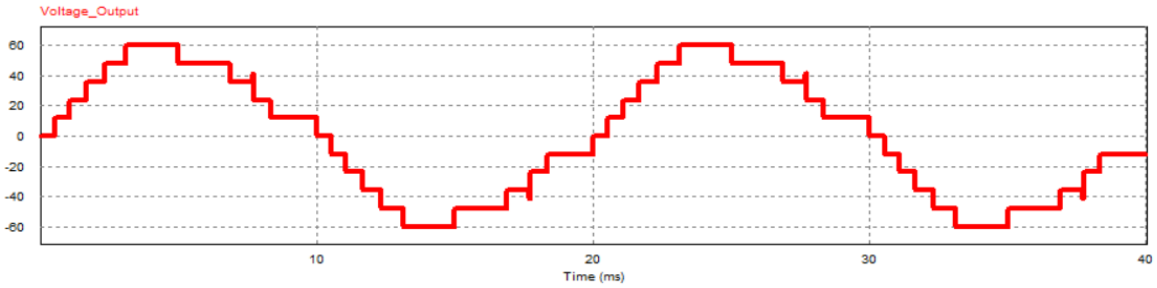

Figure 21. 11-level sinusoidal step output voltage waveform

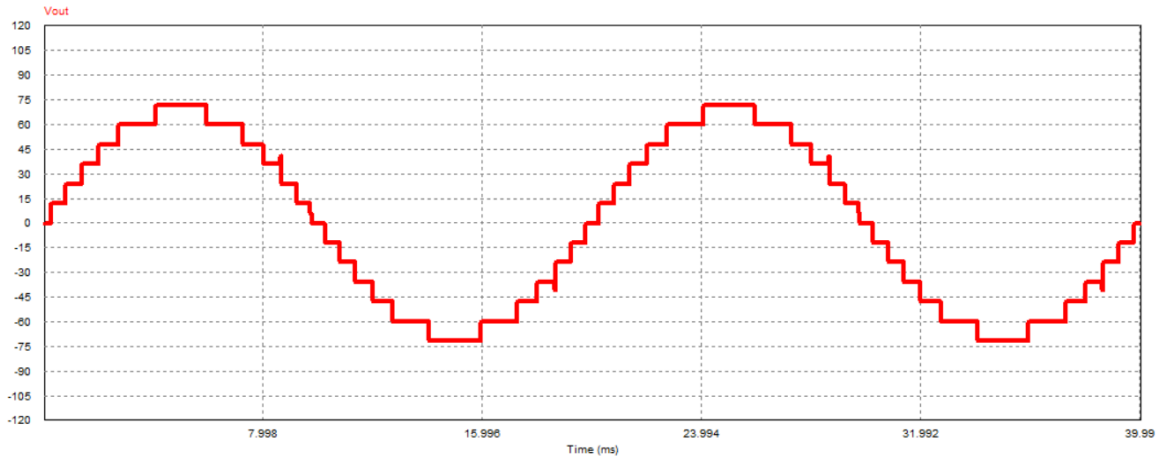

Figure 22. 13-level sinusoidal step output voltage waveform

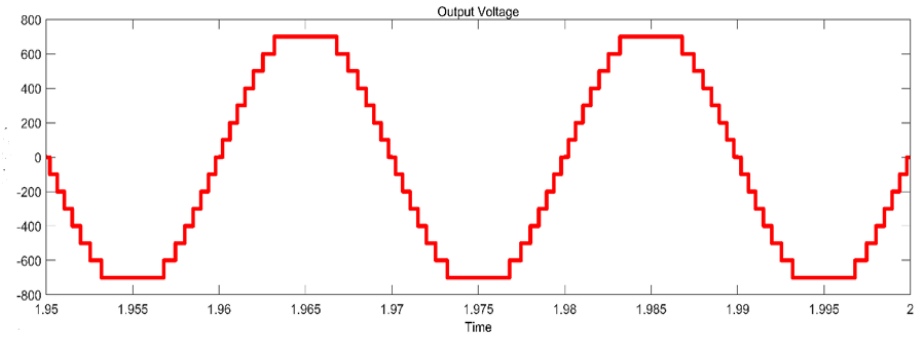

Figure 23. 15-level sinusoidal step output voltage waveform

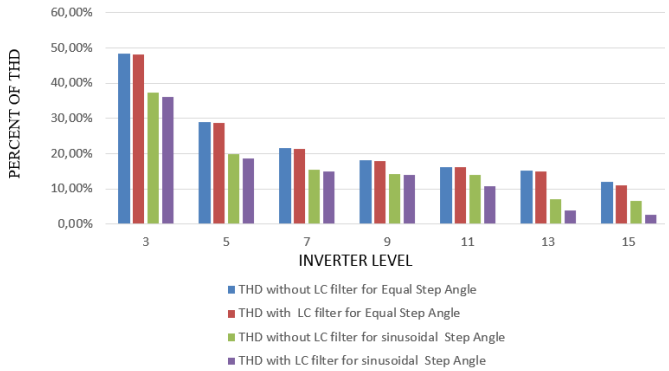

Figure 24. Level vs percent of THD

5. EXPERIMENTAL PART

For the 7-level MLI, the experimental setup and generated output waveform by using our proposed sinusoidal formula are shown in Figures 25 and 26. After the application of the LC filter in the practical device, it gives a more accurate sinusoidal signal at the output, which is shown in Figure 26. But it's a zoom-out picture. There are many spikes found in the output sinusoidal signal.

Figure 25. Experimental setup of 7-level MLI

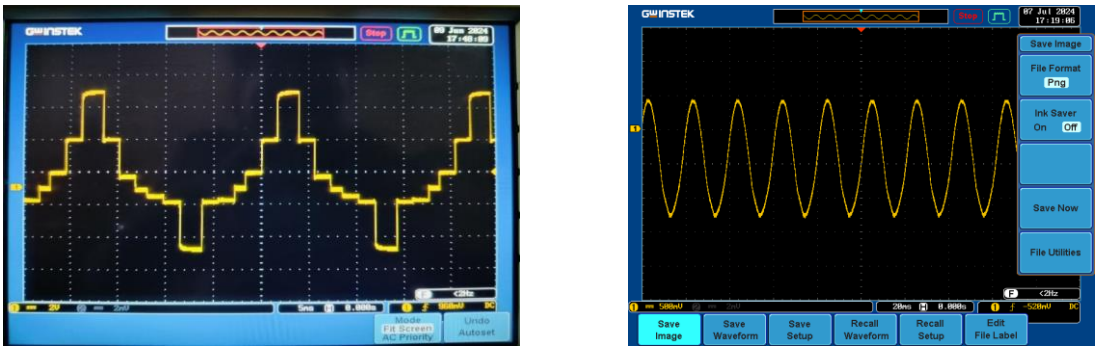

Figure 26. Experimental output waveform without applying the LC filter and after applying the filter

6. CONCLUSION

In this research, a very simple formula is used to determine the step of the sinusoidal angle. Without using any kind of modulation technique, an inverter can be designed as shown in this work. In both cases, as the number of levels increases, THD (%) decreases. The results indicate that applying the sinusoidal angle technique significantly reduces THD (%) compared to the equal step angle approach. After using the LC filter, the value of THD is decreasing more. In simulation, IGBTs have zero on/off time because it takes all the IGBTs as ideal devices. It is also important to note that any switching spikes do not appear on the output voltage at simulation work, but there is a spike found on the practical output waveform on the oscilloscope screen. Switching spikes maybe removed by introducing a suitable death time. As the level increases, the

number of switching losses will also increase. The future goal of this research is to do more experimental work for levels 9 to 15, to minimize the switching spikes that arrive on the experimental output waveform, determine the formula for calculating switching loss, and calculate the switching loss for every specific switch. Additionally, we need to determine which level will produce a more efficient output at less cost.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

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Tapan Kumar Chakraborty	✓	✓	✓		✓	✓		✓	✓	✓	✓	✓		

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author, [DAR], upon reasonable request.

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