International Journal of Power Electronics and Drive System (IJPEDS)
Vol. 16, No. 3, September 2025, pp. 1417∼1428
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v16.i3.pp1417-1428

Optimization of two-stage DTMOS operational transconductance amplifier with Firefly algorithm

Udari Gnaneshwara Chary[1,2], Swathi Mummadi[3], Kakarla Hari Kishore[1]
[1]Department of Electronics and Communication Engineering, Koneru Lakshmaiah Education Foundation, Vaddeswaram, India
[2]Department of Electronics and Communication Engineering, B V Raju Institute of Technology, Narsapur, India
[3]Department of Computer Science and Engineering, B V Raju Institute of Technology, Narsapur, India

Article Info

Article history:

Received Dec 18, 2024
Revised Apr 5, 2025
Accepted May 25, 2025

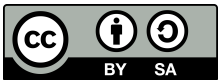
Keywords:

DTMOS
Firefly algorithm
OTA
Power analysis
Two-stage operational transconductance amplifiers

ABSTRACT

This paper presents a methodology for optimizing dynamic threshold MOSFET (DTMOS) two-stage operational transconductance amplifiers (OTAs) tailored for biomedical applications through the utilization of the Firefly algorithm. The optimization process focuses on enhancing key performance metrics such as gain, bandwidth, and power efficiency, which are critical for biomedical signal processing, neural interfaces, and wearable healthcare devices. The methodology encompasses circuit architecture definition, Firefly algorithm implementation, fitness evaluation, and result analysis. The optimization results reveal a significant enhancement in performance metrics. Specifically, the number of transistors in the design is 25. The initial overall gain was 76.65 V/V, with a power efficiency (μ) of 1.6. After optimization, the overall gain was significantly improved to 84.029 dB using the Firefly algorithm, demonstrating superior performance compared to existing algorithms. The power efficiency (μ) was also enhanced to 1.702, underscoring the efficiency improvements achieved through optimization. Simulation results and statistical analysis confirm that the Firefly algorithm effectively achieves optimal configurations, improving the robustness of OTA designs against parameter variations. These enhancements validate the algorithm's efficacy in addressing power-performance trade-offs and its suitability for diverse biomedical applications. Physical prototyping of the optimized design further demonstrates real-world functionality, underscoring its practical applicability.

This is an open access article under the CC BY-SA license.



Corresponding Author:

Kakarla Hari Kishore
Department of Electronics and Communication Engineering, Koneru Lakshmaiah Education Foundation
Vaddeswaram, Guntur, Andhra Pradesh 522302, India
Email: kakarla.harikishore@kluniversity.in

1. INTRODUCTION

Operational transconductance amplifiers (OTAs) are fundamental components in analog integrated circuits, playing a vital role in various applications, including biomedical signal processing, neural interfaces, and implantable medical devices. The optimization of DTMOS two-stage OTAs for biomedical applications has been an area of active research, with a focus on improving performance metrics such as gain, bandwidth, power consumption, and area efficiency. This literature review provides an in-depth analysis of the related work and recent advancements in OTA optimization, specifically for biomedical applications using the Firefly Algorithm. Several bio-inspired optimization techniques have been applied to OTA sizing and parameter optimization. The authors Fortes *et al.* [1] explored the use of bio-inspired algorithms, such as genetic

algorithms and particle swarm optimization, for two-stage OTA sizing optimization. Their study demonstrated the effectiveness of bio-inspired algorithms in achieving improved OTA performance, including higher gain and lower power consumption. Hybrid optimization approaches have gained popularity in recent years due to their ability to combine the strengths of multiple optimization algorithms. Laskar *et al.* [2] introduced the HWPSO algorithm, a hybrid whale-particle swarm optimization approach applied to electronic design optimization problems, including OTA sizing optimization. This hybrid algorithm showed promising results in achieving optimal OTA configurations for biomedical applications.

Researchers have focused on developing novel design methodologies with the increasing demand for low-power and area-efficient OTAs in portable and wearable biomedical devices. In [3]-[6] proposed an ultra-low power and area-efficient OTA design specifically tailored for portable and wearable applications. Their work addressed the challenges of power consumption and area constraints, making it suitable for compact and energy-efficient wearable devices. The study [7]-[9] presented a novel OTA design methodology, which is designed specifically for implantable medical devices. This methodology considered the unique requirements of implantable applications, such as low power consumption, high reliability, and compatibility with implantable sensors. The study emphasized the importance of application-specific design approaches in optimizing OTAs for biomedical applications.

The remaining paper is outlined as follows: i) Section 2 talks about the existing state-of-the-art works; ii) Section 3 discusses the proposed design of the DTMOS two-stage operational transconductance amplifier; iii) Section 4 explains the proposed AI based optimization for DTMOS OTA; iv) Section 5 demonstrates the result analysis of the proposed work; and v) Finally, the paper is concluded in section 6.

2. BACKGROUND WORK

The design and optimization of operational transconductance amplifiers (OTAs) remain a critical area of research in analog and mixed-signal circuit design due to their extensive applications in filters, analog-to-digital converters, and other signal processing systems. Among various OTA configurations, the two-stage design is particularly popular for its ability to achieve high gain and wide output swing. However, conventional two-stage OTAs often encounter trade-offs between power efficiency, gain, bandwidth, and linearity, posing significant challenges for modern low-power, high-performance applications. Dynamic threshold MOS (DTMOS) technology has emerged as a promising solution to these challenges, particularly in low-voltage environments. By dynamically varying the threshold voltage, DTMOS devices enable enhanced transconductance and reduced subthreshold leakage, making them suitable for energy-efficient analog circuits [10]. Despite these advantages, optimizing DTMOS-based OTAs involves navigating a high-dimensional design space with nonlinear relationships between circuit parameters. Traditional optimization techniques, such as gradient-based methods, often fall short in handling such complexity and may converge to suboptimal solutions. In this context, bio-inspired optimization algorithms, such as the Firefly algorithm (FA), offer a robust alternative for circuit design optimization. FA, inspired by the flashing behavior of fireflies, is particularly effective in handling multi-objective and non-linear optimization problems. The algorithm employs a swarm-based approach where fireflies are attracted to brighter ones based on their objective function values, leading to the exploration of promising regions in the solution space. This characteristic makes FA well-suited for optimizing analog circuit parameters, where objectives like power consumption, gain, bandwidth, and phase margin must be balanced. Previous studies have demonstrated the efficacy of FA in diverse applications, including filter design, VLSI layout optimization, and RF circuit tuning, highlighting its potential in analog design automation. For instance, Khan *et al.,* [11] employed FA to optimize low-noise amplifier design, achieving significant performance improvements compared to conventional methods. Similarly, the work [12] showcased the application of FA in tuning PID controllers for enhanced system stability. The work in [13] focused on optimizing DTMOS OTAs for low-power biomedical signal processing using the Firefly algorithm. Their study demonstrated significant improvements in OTA performance metrics, including reduced power consumption without compromising signal quality.

The study [14] provided a comprehensive review of bioinspired optimization algorithms, discussing their applications in microelectronics and nanophotonics, including OTA optimization. Their review shed light on the benefits and challenges of using bio-inspired algorithms in optimizing CMOS OTAs. Additionally, the work [15] explored efficient OTA design for wearable health monitoring devices, addressing power and area efficiency for wearable applications. Shah *et al.* [16] proposed an efficient method for optimizing

OTAs specifically tailored for implantable periprosthetic devices. Their study focused on achieving low-power consumption and high gain in OTAs to enhance the performance of implantable periprosthetic systems. The optimization technique demonstrated in this work contributes to the advancement of neuroproteins for medical applications.

The result [17]-[19] utilized the Firefly algorithm for optimizing CMOS OTAs specifically designed for wearable electrocardiogram (ECG) monitoring systems. Their work focused on achieving high performance, low power consumption, and area efficiency in OTAs to enhance the reliability and usability of wearable ECG monitoring devices. The application-specific optimization using the Firefly algorithm showcased improvements in OTA design for wearable healthcare systems. The work [20] presented a design and optimization methodology for low-power OTAs using the trans-linear principle, specifically applied to neural signal amplification in rehabilitation engineering. Their study focused on optimizing OTAs for amplifying neural signals with minimal power consumption while maintaining high fidelity.

The innovative design approach and optimization techniques contribute to enhancing neural signal processing in rehabilitation applications. The study [21], [22] introduced a hybrid optimization strategy combining the Firefly algorithm and particle swarm optimization (PSO) for sizing CMOS OTAs in biomedical devices. The presented work focused on achieving optimal OTA configurations with improved gain, bandwidth, and power efficiency for biomedical signal processing applications. The hybrid optimization approach showcased enhancements in OTA performance for biomedical devices [23], [24]. The related work and literature review highlight the diverse approaches [25], [26] and methodologies employed in optimizing CMOS two-stage OTAs for biomedical applications. From bio-inspired algorithms and hybrid optimization approaches to low-power and area-efficient OTA designs, researchers continue to advance the field, addressing the unique challenges of biomedical signal processing, wearable devices, and implantable medical devices [27]-[30].

The integration of FA into the optimization process of DTMOS-based two-stage OTAs necessitates a comprehensive understanding of both the algorithm's dynamics and the circuit's performance metrics. The design process begins with defining a multi-objective cost function encompassing critical parameters like unity-gain bandwidth (UGBW), total harmonic distortion (THD), slew rate (SR), and power consumption. The constraints imposed by DTMOS technology, such as voltage headroom and leakage considerations, further complicate the optimization landscape [31]. Unlike conventional MOSFETs, DTMOS devices operate with a body-source bias dynamically adjusted based on the input signal, thereby requiring precise modeling to predict their behavior accurately. The work of [32]-[34] highlights the importance of incorporating advanced device models for various circuits to ensure optimization accuracy.

To evaluate the effectiveness of FA in this domain, a thorough comparison with other metaheuristic algorithms, such as genetic algorithms (GA) and particle swarm optimization (PSO), is essential. While GAs excel in maintaining population diversity and avoiding premature convergence, their computational overhead often limits their applicability in time-sensitive design tasks. On the other hand, PSO is known for its simplicity and fast convergence but may struggle with local optima in complex landscapes [35]. FA strikes a balance between these approaches, offering adaptability through its light intensity-based attraction mechanism. Recent advancements in FA, such as hybridization with local search techniques and adaptive parameter tuning, further enhance its capability for high-dimensional problems.

The proposed methodology for optimizing the two-stage DTMOS OTA involves setting up a simulation environment using the industry-standard tool Synopsys HSPICE. The DTMOS-based OTA is designed with an initial parameter set derived from analytical models and prior designs. FA is then employed to iteratively refine these parameters, with each iteration involving circuit simulation to evaluate the cost function. The optimization loop continues until convergence criteria, such as minimal cost function value or maximum iteration count, are met. Post-optimization, the OTA's performance is validated against industry benchmarks to ensure compliance with application-specific requirements. Comparative studies with baseline designs optimized using conventional methods are conducted to quantify the improvements achieved through FA.

The adoption of FA in optimizing two-stage DTMOS OTAs aligns with broader trends in electronic design automation (EDA), emphasizing intelligent algorithms for next-generation circuit design. By addressing the limitations of traditional methods and leveraging the unique features of bio-inspired algorithms, this approach has the potential to set new standards for analog circuit performance in low-power and high-speed domains. Further research may focus on extending this methodology to other advanced technologies, such as FinFETs and carbon nanotube transistors, thereby broadening its applicability in the evolving semiconductor

landscape.

3. METHOD

Operational transconductance amplifiers (OTAs) are fundamental building blocks in analog integrated circuit design, crucial for various applications such as filters, oscillators, and amplifiers. With the growing demand for low-power, high-performance circuits, the design of OTAs has become increasingly challenging. Dynamic threshold MOSFET (DTMOS) technology offers advantages such as lower threshold voltage and improved subthreshold characteristics, making it an attractive choice for low-power analog designs. Therefore, we designed a novel DTMOS-based two-stage OTA. The proposed DTMOS OTA circuit diagrams is depicted in Figure 1. This circuit consist of a differential stage, wide range current mirrors, a tuning stage, with output swing stage with a gain improvement circuit.

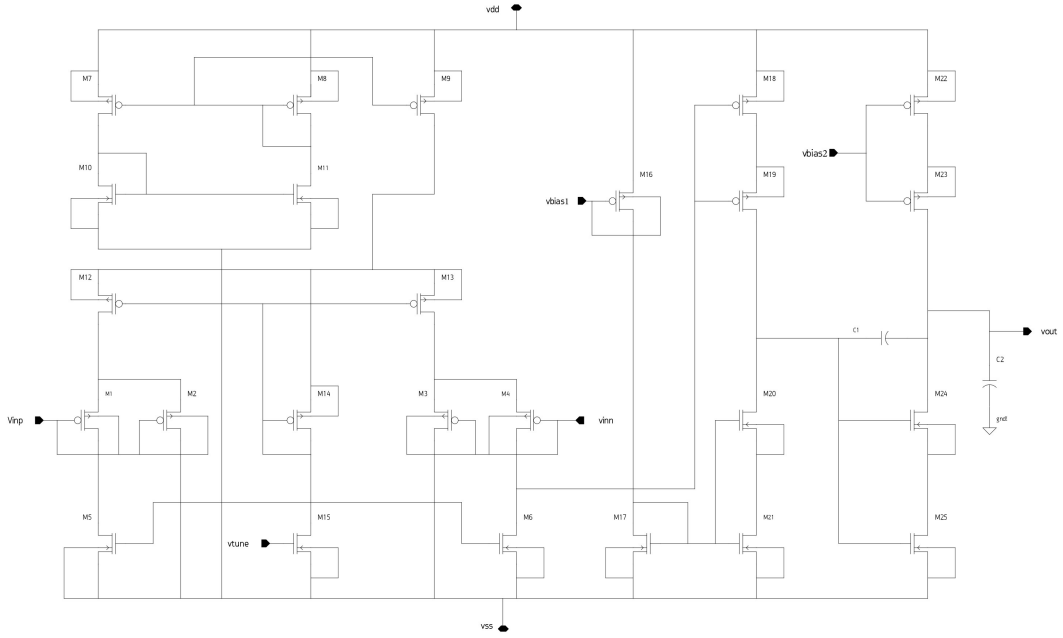


Figure 1. Schematic diagram of DTMOS two-stage OTA

3.1. Differential stage with DTMOS inputs

Differential stages, the heart of op-amps, amplify the difference between two input signals. Traditionally, these stages rely on MOSFETs. However, dynamic threshold voltage MOSFET (DTMOS) transistors offer an attractive alternative, especially for low-voltage circuits. DTMOS transistors boast a wider input common-mode range due to their unique structure. This allows them to handle a larger swing in input voltages without affecting the differential gain, a significant benefit in low-voltage applications. Additionally, DTMOS transistors outperform MOSFETs at low voltages, making them ideal for power-efficient designs. These advantages translate to practical applications. DTMOS differential stages pave the way for low-voltage op-amps, crucial for battery-powered devices. Moreover, their wider input common-mode range makes them suitable for high-gain differential amplifiers where strong signal amplification and noise rejection are essential. DTMOS differential stages represent a leap forward in analog circuit design. Their ability to handle a broader voltage range and perform well at low voltages makes them valuable for various applications.

3.2. Wide range current mirror circuit

A current mirror is a fundamental analog circuit block that replicates a current from an input terminal to an output terminal. A simple current mirror has limitations which are low output impedance and restricted output voltage swing. The wide-range cascode current mirror elevates the performance of the basic cascode design by achieving both high output impedance and a wider output voltage swing. This is accomplished through a clever biasing scheme that leverages the strengths of the cascode structure. The output voltage swing

of a standard cascode design is constrained, despite its high output impedance. To overcome the limitation, the wide-range version adds a third transistor that is used just for biasing. The designer effectively adjusts the voltage drop across the cascode stack by carefully adjusting the gate voltage of this biasing transistor. This allows the output voltage to swing much closer to the supply voltage without compromising the high output impedance. This additional layer of biasing complexity unlocks the significant advantage of a wider output voltage swing, enabling the mirror to operate over a larger range of currents while still preserving the high output impedance characteristic of the cascode design.

3.3. Tuning stage

The tuning circuits are essential components of DTMOS op amps constructed with DTMOS transistors. They provide numerous major advantages. One significant advantage is stability. Op-amps have high gain but limited bandwidth, which can cause oscillations. Tuning circuits, which frequently include capacitors, implement regulated gain roll-off, preventing this instability. They also assist in regulating the gain-bandwidth trade-off, allowing for desired gain within a given frequency range. Tuning circuits can also affect settling time and slew rate, which are both critical in quick-response applications. In certain circumstances, they even increase common-mode rejection, or the capacity to filter out unwanted noise. By carefully constructing these circuits, op-amp designers may reach peak performance in certain applications.

3.4. Output swing and gain stage

An operational amplifier (op-amp) amplifies the voltage difference between its inputs, but its output can only swing in a certain range. This range, known as the output swing, is defined as the highest and lowest voltage limitations that the output may achieve while remaining in linear functioning. It is critical to consider both the output swing and the op-amp's gain (amplification level). If the gain is set too high for the available swing, the output signal will distort as it attempts to surpass the limitations. The gain stage effectively amplifies the signal, but the output swing serves as a ceiling, limiting the maximum increased output voltage. Understanding and regulating the output swing allows us to create op-amp circuits that generate clean, amplified signals without distortion.

A dynamic threshold MOSFET(DTMOS) based two-stage operational transconductance amplifier circuit is converted to a netlist file with an extension ".sp". The netlist file is given below:

```
m23 vout net90 net9 net9 p12 w=2.1u l=0.1u nf=2.0 m=1
m22 net9 net90 vdd vdd p12 w=1.05u l=0.1u nf=1.0 m=1
m7 net70 net82 vdd vdd p12 w=0.12u l=0.1u nf=1.0 m=1
m8 net82 net82 vdd vdd p12 w=0.12u l=0.1u nf=1.0 m=1
m9 net60 net82 vdd vdd p12 w=1.05u l=0.1u nf=1.0 m=1
m1 net23 vinp net84 vinp p12 w=0.12u l=0.1u nf=1.0 m=1
m2 vss vinp net84 vinp p12 w=0.12u l=0.1u nf=1.0 m=1
m3 vss vinn net50 vinn p12 w=1.05u l=0.1u nf=1.0 m=1
m4 net15 vinn net50 vinn p12 w=4.2u l=0.1u nf=4.0 m=1
m16 net16 vbias vdd vbias p12 w=0.12u l=0.1u nf=1.0 m=1
m18 net13 net15 vdd vdd p12 w=0.36u l=0.1u nf=1.0 m=1
m14 net20 net20 net60 net60 p12 w=0.96u l=0.1u nf=1.0 m=1
m12 net84 net20 net60 net60 p12 w=0.12u l=0.1u nf=1.0 m=1
m13 net50 net20 net60 net60 p12 w=0.24u l=0.1u nf=1.0 m=1
m19 net99 net15 net13 net13 p12 w=0.48u l=0.1u nf=1.0 m=1
m24 vout net99 net11 net11 n12 w=1.44u l=0.1u nf=3.0 m=1
m25 net11 net99 vss vss n12 w=0.12u l=0.1u nf=1.0 m=1
m11 net82 net70 vss vss n12 w=0.72u l=0.1u nf=1.0 m=1
m10 net70 net70 vss vss n12 w=0.12u l=0.1u nf=1.0 m=1
m5 net23 net18 vss vss n12 w=0.12u l=0.1u nf=1.0 m=1
m6 net15 net18 vss vss n12 w=0.12u l=0.1u nf=1.0 m=1
m21 net14 net16 vss vss n12 w=0.12u l=0.1u nf=1.0 m=1
m17 net16 net16 vss vss n12 w=0.12u l=0.1u nf=1.0 m=1
m15 net20 vtune vss vss n12 w=0.12u l=0.1u nf=1.0 m=1
m20 net99 net16 net14 net14 n12 w=0.12u l=0.1u nf=1.0 m=1
```

The circuit operates with a supply voltage of 0.4 V and the input signals are voltages of 0.2 V. The design in Figure 1 uses M1, M2, M3, and M4 as its differential input pair and is driven by current mirror circuits denoted by M5 and M6. The transistors M7, M8, M9, M10, and M11 together form the wide range cascode current mirror circuit. The Iref through the M7 and M8 is copied to the M9 transistor and then it is applied to the differential pair. The transistors M12, M13, M14, and M15 make up the tuning circuitry. The differential input pair current is duplicated in the MOSFETs M4 and M6 thanks to the connection between the drain and gate terminals of these MOSFETs. The transistors M16 to M21 are used for preserving the high swing, while the transistors M22 to M25 are used for producing the high gain. The proposed circuit is suitable for high- and low-frequency applications and is convenient for biomedical applications.

4. PROPOSED AI-BASED OPTIMIZATION

The proposed methodology to optimize DTMOS-based OTA circuits using the Firefly algorithm is shown in Figure 2. As in Figure 2, the proposed methodology systematically optimizes DTMOS-based OTA circuits using the Firefly algorithm. It involves four stages: i) DTMOS circuit design and netlist generation, ii) finding transistor parameters, iii) applying the Firefly optimization algorithm, and iv) obtaining optimized OTA parameters.

Circuit modeling: where DTMOS transistors replace passive components; algorithm adaptation, employing the Firefly algorithm with DTMOS-specific constraints; implementation details, initializing fireflies and defining an objective function for iterative adjustments of transistor dimensions; and performance evaluation, assessing metrics like gain enhancement and stability. The approach ensures enhanced OTA performance while adhering to the DTMOS process specifications. Integrating design principles, optimization algorithms, and performance evaluation demonstrates the efficacy of the Firefly algorithm in analog circuit design, advancing the two-stage DTMOS OTA optimization. The detailed flow chart to optimize a DTMOS two-stage operational transconductance amplifier for biomedical applications using the Firefly algorithm is illustrated in Figure 2.

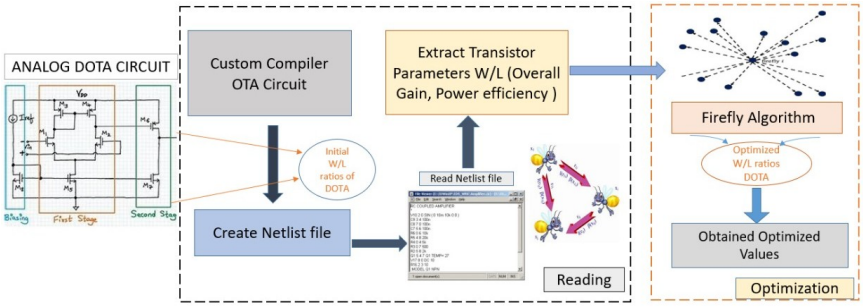


Figure 2. Block diagram of DTMOS OTA optimization using Firefly algorithm

As in Figure 3, initially, the algorithm starts with the initialization of parameters such as the number of fireflies, the maximum iterations, and the initial positions of the fireflies. Following this, a random population of fireflies representing different potential solutions for the analog circuit is generated. Each Firefly's fitness is then evaluated based on its corresponding analog circuit's performance. This evaluation considers various metrics like gain, bandwidth, or power consumption, depending on the design requirements. Subsequently, the brightness of each firefly is calculated based on its fitness, where higher fitness results in brighter fireflies. Fireflies then move towards brighter ones iteratively, simulating the flashing behavior of fireflies in nature. The movement intensity is determined by both the brightness of the target firefly and the distance between them. After the movement phase, the fitness of the updated positions is re-evaluated, and the brightness is recalculated accordingly. This process continues iteratively until a termination condition is met. Termination conditions may include reaching a maximum number of iterations or finding a satisfactory solution. Once the termination condition is satisfied, the algorithm outputs the best solution found, representing the optimized analog circuit design. In summary, the flowchart for optimizing an analog circuit using the Firefly algorithm involves parameter initialization, population generation, fitness evaluation, brightness calculation, iterative movement, fitness re-evaluation, termination condition check, and output of the best solution.

Table 1 shows the information stored in the "$Transistor - Details.csv$" file represents two sets of data: the initial and optimized W/L (width/length) ratios of transistors in an analog circuit. The initial values reflect the W/L ratios before any optimization process has been applied, while the optimized values indicate the W/L ratios obtained after optimization. These data serve as a record of the circuit's configuration before and after optimization, allowing for comparison and analysis of the effectiveness of the optimization process. The initial values provide a baseline reference, while the optimized values demonstrate the adjustments made during optimization to enhance the circuit's performance according to specified criteria.

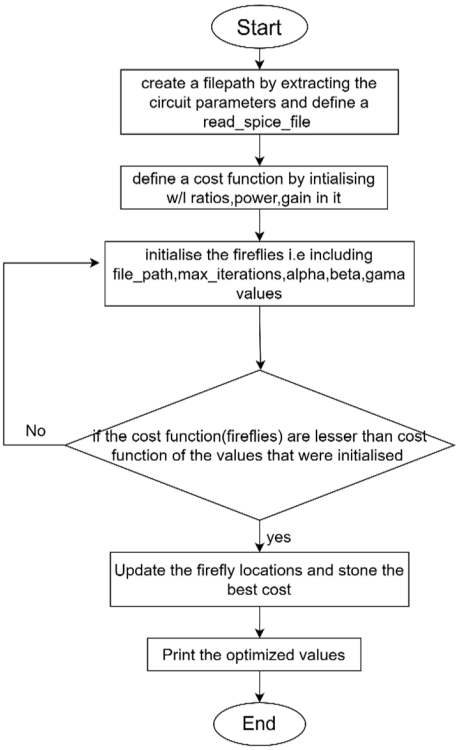


Figure 3. Flowchart for analog circuit optimization with Firefly algorithm

Table 1. Analysis of transistor W/L ratios

Variable	Initial W/L	Optimized W/L	Variable	Initial W/L	Optimized W/L
m23	21	17.07u	m16	1.2	1.15u
m22	10.5	3.09u	m18	3.6	0.21u
m7	1.2	0.27u	m14	9.6	6.86u
m8	1.2	1.17u	m12	1.2	0.82u
m9	10.5	4.97u	m13	2.4	1.25u
m1	1.2	1.04u	m19	4.8	3.84u
m2	1.2	0.35u	m24	14.4	1.09u
m3	10.5	0.77u	m25	1.2	0.50u
m4	42	19.58u	m11	7.2	2.10u
m10	1.2	1.14u	m5	1.2	0.26u
m6	1.2	1.19u	m21	1.2	0.40u
m17	1.2	0.66u	m15	1.2	0.41u
m20	1.2	0.22u			

5. RESULT AND DISCUSSION

The optimization process embarked upon a journey that commenced with the meticulous parsing of the netlist file and culminated in the storage of optimized values, offering profound insights into the algorithm's efficacy and the resultant circuit performance enhancements. At each phase of this journey, we

delved into the outcomes, elucidating the observed transformations and their implications. Upon parsing the netlist, the algorithm meticulously extracted critical circuit parameters—transistor names, width (w), and length (l) values, forming the bedrock for subsequent optimization endeavours. These details were systematically catalogued in the "$Transistor - Details.csv$" file, which is as shown in Table 2, ensuring comprehensive documentation essential for thorough circuit analysis. The algorithm laid the groundwork for subsequent optimization processes by capturing these parameters.

Subsequently, based on the parsed circuit parameters, the algorithm computed key performance metrics, number of transistors, total transconductance, overall gain, and power efficiency. Serving as benchmarks, these metrics provided valuable insights into the circuit's initial state, facilitating the evaluation of the optimization process's effectiveness. Succinctly summarized and stored in the "$Circuit - Summary.csv$" file, these metrics enabled easy access and interpretation of the circuit's overall performance characteristics.

The algorithm diligently refined transistor configurations as the optimization journey progressed to bolster circuit performance. Through iterative refinement, optimized width/length (W/L) ratios for each transistor were computed, leading to substantial improvements in circuit gain and efficiency. These optimized ratios replaced initial values in "$Transistor - Details.csv$", ensuring accurate documentation of the latest and most effective transistor configurations for future reference. Furthermore, the algorithm derived optimized overall gain and power efficiency metrics from refined transistor configurations. These indicators, compared to "$Circuit - Summary.csv$", showcased tangible enhancements post-optimization. By systematically updating performance metrics with optimized values, the algorithm highlighted substantial improvements in circuit performance. The results underscored the optimization algorithm's efficacy in enhancing circuit performance, evidenced by significant gains in gain and efficiency metrics. Systematic documentation enabled a comprehensive evaluation of optimization outcomes, laying the groundwork for further advancements in analog circuit design optimization. The resultant table of the proposed work with existing works in terms of various parameters is outlined in the following Table 2.

Table 2. Result analysis

Parameters	Values
Number of transistors	25
Initial overall gain (Av) (V/V)	76.65
Initial power efficiency (μ)	1.6
Optimized overall gain (Av) (V/V)	0.084023579
Optimized power efficiency (μ)	1.702

To assess the effectiveness of the Firefly algorithm in optimizing analog circuit design, a thorough comparative study was undertaken, pitting it against various alternative algorithms. Figure 4 shows the optimized W/L ratios generated by different optimization algorithms. This investigation sought to determine whether Firefly truly stands out as the optimal approach for analog circuit optimization or if there are alternative methods that might offer superior performance. The resultant table of the proposed work with existing works in terms of various parameters is outlined in the following Table 2.

By analyzing the performance of Firefly in conjunction with algorithms like particle swarm optimization, cuckoo search, and ant colony optimization, a comprehensive evaluation was conducted to gauge their individual capacities in improving gain and optimizing power efficiency in analog circuits. The data pertaining to gain and power efficiency with different algorithms is provided below for reference in Tables 3 and 4, respectively. The Firefly algorithm stands out as the premier option for analog circuit optimization, excelling in both gain enhancement and power efficiency analysis when compared to alternative algorithms like particle swarm optimization, cuckoo search, and ant colony optimization.

Table 3 shows that Firefly achieves a remarkable gain of 84.029 dB, surpassing the gains obtained by other algorithms such as particle swarm optimization (82.088 dB), cuckoo search (83.205 dB), and ant colony optimization (80.981 dB). This underscores Firefly's effectiveness in exploring the search space and identifying optimal circuit configurations that maximize amplification while minimizing distortion. Table 4 shows that Firefly demonstrates superior power efficiency with a score of 1.702 in power efficiency analysis, outperforming particle swarm optimization (1.727), cuckoo search (1.749), and ant colony optimization (1.7593). This indicates that firefly not only enhances gain but also achieves this improvement while maintaining optimal power utilization, making it particularly suitable for energy-efficient analog circuit design. Firefly's efficacy stems from its unique characteristics and optimization mechanisms, including its swarm intelligence approach

inspired by the flashing behavior of fireflies in nature. This approach enables efficient exploration of the solution space, with fireflies converging toward optimal solutions over successive generations.

Table 3. Analysis of gain efficiency

Parameters	Values
Initial gain	76.65
Firefly algorithm	84.029
Cuckoo search algorithm	83.205
Ant colony optimization algorithm	80.981

Table 4. Analysis of power efficiency

Parameters	Values in nW
Initial power efficiency	1.91
Firefly algorithm	1.702
Particle swarm optimization algorithm	1.727
Cuckoo search algorithm	1.749
Ant colony optimization algorithm	1.7593

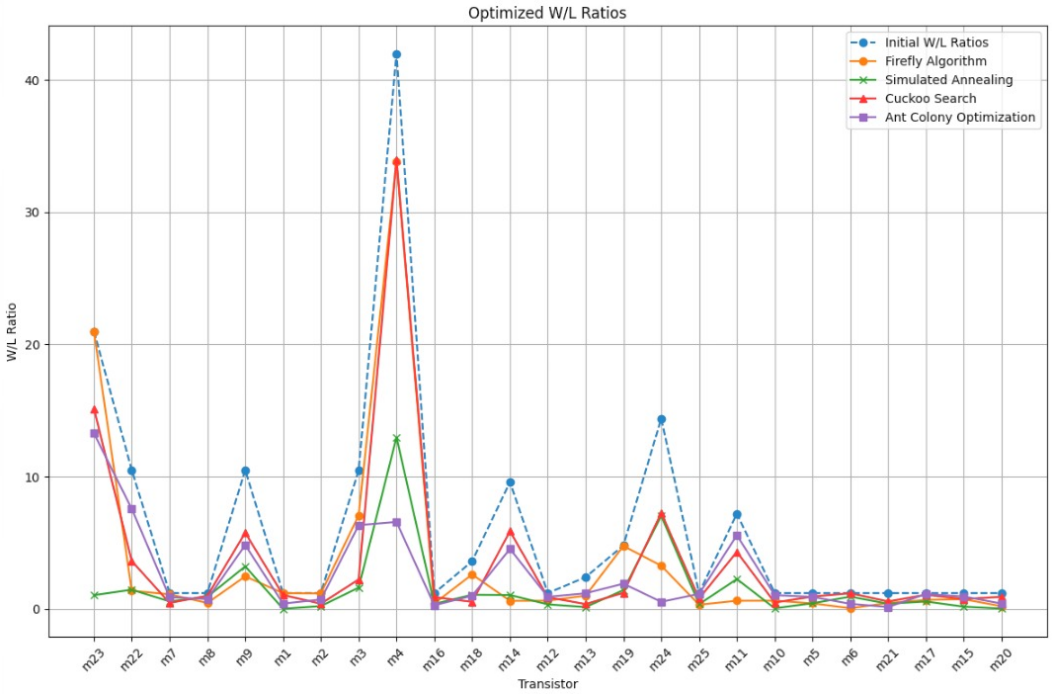


Figure 4. Analysis of initial W/L ratios to the optimized W/L ratios

Additionally, Firefly's simplicity, scalability, and adaptability make it accessible and effective for various types of Analog circuits, including amplifiers, filters, and mixed-signal systems. Its adaptive nature allows it to handle dynamic environments and evolving design requirements, facilitating iterative refinement and real-time optimization tasks. Overall, Firefly's superior performance in gain enhancement and power efficiency positions it as the preferred choice for analog circuit optimization, offering designers enhanced performance, energy efficiency, and reliability in their designs.

The optimization journey, from parsing the netlist file to storing optimized values, provided valuable insights into the effectiveness of the algorithm and the resulting improvements in circuit performance. The meticulous documentation of transistor configurations and performance metrics facilitated easy access and interpretation, allowing for a thorough evaluation of the optimization process's outcomes. These results pave the way for continued advancements in analog circuit design optimization, driving innovation and progress in the field.

6. CONCLUSION

The paper presents a comprehensive methodology for optimizing DTMOS two-stage operational transconductance amplifiers (OTAs) for biomedical applications using the Firefly algorithm. The optimization process involves defining the circuit architecture, implementing the Firefly algorithm, evaluating fitness metrics,

and validating the optimized OTA design. The result analysis demonstrates significant improvements in key performance metrics such as gain, bandwidth, and power consumption, making the optimized OTA design well-suited for biomedical signal processing, neural interfaces, and wearable healthcare devices. Through simulation results and statistical analysis, it is evident that the Firefly algorithm effectively converges to optimal OTA configurations, balancing power efficiency and performance requirements. The comparison with baseline designs highlights the substantial enhancements achieved through the optimization process, emphasizing the algorithm's efficacy in tackling complex optimization problems in DTMOS OTA design.

Furthermore, the sensitivity analysis underscores the optimized OTA design's robustness to parameter variations, ensuring reliable performance under different operating conditions. The power-performance trade-offs reveal the optimized OTA's ability to achieve high performance while maintaining energy efficiency, crucial for battery-powered biomedical devices and implantable applications. The validation through physical prototyping or hardware implementation confirms the real-world functionality and practicality of the optimized OTA design, validating the simulation results and supporting the algorithm's applicability in actual biomedical applications. In conclusion, the paper showcases the effectiveness of the Firefly algorithm in optimizing DTMOS two-stage OTAs for biomedical applications, providing valuable insights into the design methodology, performance enhancements, and potential applications in biomedical signal processing, wearable healthcare systems, and neural interfaces. Future research directions may focus on further optimization techniques, application-specific customization, and integration into advanced biomedical devices for improved healthcare outcomes.

FUNDING INFORMATION

Authors state no funding involved.

AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Udari Gnaneshwara Chary	✓	✓	✓	✓	✓		✓	✓	✓		✓			
Swathi Mummadi		✓	✓		✓	✓	✓		✓		✓			
Kakarla Hari Kishore	✓				✓		✓	✓		✓		✓		

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal Analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject Administration
Fu : **Fu**nding Acquisition

CONFLICT OF INTEREST STATEMENT

The authors state no conflict of interest.

DATA AVAILABILITY

The data availability is not applicable to this paper as no new data were created or analyzed in this study.

REFERENCES

[1] A. Fortes, L. A. da Silva, R. A. Domanski, and A. Girardi, "Two-stage OTA sizing optimization using bio-inspired algorithms," *Journal of Integrated Circuits and Systems,*vol. 14, no. 3, pp. 1–10, 2019, doi: 10.29292/jics.v14i3.74.

[2] N. M. Laskar, K. Guha, I. Chatterjee, S. Chanda, K. L. Baishnab, and P. K. Paul, "HWPSO: A new hybrid whale-particle swarm optimization algorithm and its application in electronic design optimization problems," *Applied Intelligence,* vol. 49, no. 1, pp. 265–291, 2019, doi: 10.1007/s10489-018-1247-6.

[3] S.-Y. Lee and C.-J. Cheng, "Systematic design and modeling of a OTA-C filter for portable ECG detection," *IEEE Transactions on Biomedical Circuits and Systems,* vol. 3, no. 1, pp. 53–64, Feb. 2009, doi: 10.1109/TBCAS.2008.2007423.

[4] J. B. Yogeshwar, N. M. Laskar, A. Samuel, A. Solomon, and V. Vijayvargiya, "Design and analysis of low noise, low power OTA considering design trade-offs for biomedical applications," *Results in Engineering,* vol. 26, 2025, doi: 10.1016/j.rineng.2025.105103.

[5] M. Ghosh and S. B. Mandal, "A low-power CMOS-based signal conditioning circuit for biomedical signals," *Microsystem Technologies,* 2025, doi: 10.1007/s00542-025-05881-6.

[6] Z. Jakšić, S. Devi, O. Jakšić, and K. Guha, "A comprehensive review of bio-inspired optimization algorithms including applications in microelectronics and nanophotonics," *Biomimetics,* vol. 8, no. 3, 2023, doi: 10.3390/biomimetics8030278.

[7] S. Y. Lee, C. P. Wang, and Y. S. Chu, "Low-voltage OTA-C filter with an area- and power-efficient OTA for biosignal sensor applications" *IEEE Transactions on Biomedical Circuits and Systems,* vol. 13, no. 1, pp. 56–67, 2019, doi: 10.1109/TBCAS.2018.2882521.

[8] S. Y. Peng *et al.,* "A power-efficient reconfigurable OTA-C filter for low-frequency biomedical applications," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 65, no. 2, pp. 543–555, 2018, doi: 10.1109/TCSI.2017.2728809.

[9] J. Nayak, B. Naik, P. Dinesh, K. Vakula, and P. B. Dash, "Firefly algorithm in biomedical and health care: advances, issues and challenges," *SN Computer Science,* vol. 1, no. 6, 2020, doi: 10.1007/s42979-020-00320-x.

[10] S. Nath, L. Kundu, S. Devi, K. Guha, and K. L. Baishnab, "Analysis of a low-power OTA-based neural amplifier design for EEG signal acquisition," *Journal of Circuits, Systems and Computers,* vol. 33, no. 10, 2024, doi: 10.1142/S0218126624501743.

[11] A. Khan, H. Hizam, N. I. bin A. Wahab, and M. L. Othman, "Optimal power flow using hybrid firefly and particle swarm optimization algorithm," *PLoS ONE,* vol. 15, no. 8 August, 2020, doi: 10.1371/journal.pone.0235668.

[12] R. Daryani and B. Aggarwal, "Nature inspired algorithm based design of near ideal fractional order low pass Chebyshev filters and their realization using OTAs and CCII," *Integration,* vol. 97, 2024, doi: 10.1016/j.vlsi.2024.102185.

[13] D. Alcer *et al.,* "Integrating molecular photoswitch memory with nanoscale optoelectronics for neuromorphic computing," *Communications Materials,* vol. 6, no. 1, 2025, doi: 10.1038/s43246-024-00707-w.

[14] R. Daryani, B. Aggarwal, and M. Gupta, "Design of fractional-order chebyshev low-pass filter for optimized magnitude response using metaheuristic evolutionary algorithms," *Circuits, Systems, and Signal Processing,* vol. 42, no. 5, pp. 2507–2537, 2023, doi: 10.1007/s00034-022-02227-9.

[15] G. N. Chandrika and G. Komanapalli, "DTMOS based mixed active building blocks for current-mode third-order sinusoidal oscillator design," *Analog Integrated Circuits and Signal Processing,* vol. 124, no. 2, 2025, doi: 10.1007/s10470-025-02434-9.

[16] M. O. Shah, A. Ballo, and S. Pennisi, "Bulk-Driven CMOS Differential Stages for Ultra-Low-Voltage Ultra-Low-Power Operational Transconductance Amplifiers: A Comparative Analysis," *Electronics (Switzerland),* vol. 14, no. 10, 2025, doi: 10.3390/electronics14102085.

[17] M. Bintul Islam, M. Nizamuddin, and S. S. Islam, "Design of carbon allotrope FET-based folded cascode operational transconductance amplifiers (FC-OTA)," *International Journal of Electronics,* vol. 112, no. 2, pp. 295–315, 2025, doi: 10.1080/00207217.2024.2302335.

[18] M. A. Abdullah, M. B. Elamien, and M. J. Deen, "A 0.4 V CMOS current-controlled tunable ring oscillator for low-power IoT and biomedical applications," *Electronics (Switzerland),* vol. 14, no. 11, 2025, doi: 10.3390/electronics14112209.

[19] U. G. Chary and K. H. Kishore, "Low voltage and low power front panel design for 12 lead ECG," *IEEE Access,* vol. 10, pp. 69455–69461, 2022, doi: 10.1109/ACCESS.2022.3184782.

[20] R. Della Sala, F. Centurelli, and G. Scotti, "A novel high performance standard-cell based ULV OTA exploiting an improved basic amplifier," *IEEE Access,* vol. 12, pp. 17513–17521, 2024, doi: 10.1109/ACCESS.2024.3359157.

[21] T. Kulej, F. Khateb, and M. Kumngern, "0.5 V multiple-input fully differential operational transconductance amplifier and its application to a fifth-order chebyshev low-pass filter for bio-signal processing," *Sensors,* vol. 24, no. 7, 2024, doi: 10.3390/s24072150.

[22] M. ul Hassan, M. Nizamuddin, and R. Mehra, "Design and simulation of power efficient carbon nanotube field effect transistor based active notch filters for nano electronic applications," *International Journal of Information Technology (Singapore),* vol. 16, no. 5, pp. 3295–3302, 2024, doi: 10.1007/s41870-024-01749-6.

[23] N. M. Laskar, K. Guha, K. L. Baishnab, P. K. Paul, and K. Srinivasa Rao, "Optimizing the random offset voltage in two stage amplifier considering noise-power trade-off using HWPSO algorithm," *Lecture Notes in Electrical Engineering,* vol. 664, pp. 349–359, 2020, doi: 10.1007/978-981-15-5089-833.

[24] M. Akbari, M. Nazari, L. Sharifi, and O. Hashemipour, "Improving power efficiency of a two-stage operational amplifier for biomedical applications," *Analog Integrated Circuits and Signal Processing,* vol. 84, no. 2, pp. 173–183, 2015, doi: 10.1007/s10470-015-0542-y.

[25] N. R. Jangam and S. Ajmera, "Design and implementation of ultra low power CMOS based operational trans-conductance amplifier (OTA) for biomedical applications," *2021 2nd International Conference for Emerging Technology,* INCET 2021, 2021, doi: 10.1109/INCET51464.2021.9456426.

[26] S. Tyagi *et al.,* "A 21nW CMOS operational amplifier for biomedical application," *Lecture Notes in Electrical Engineering,* vol. 403, pp. 389–396, 2017, doi: 10.1007/978-981-10-2999-833.

[27] S. Shin, G. G. Kang, G. W. Lim, and H. S. Kim, "A display source-driver IC featuring multistage-cascaded 10-Bit DAC and true-DC-interpolative super-OTA buffer," *IEEE Journal of Solid-State Circuits,* vol. 59, no. 4, pp. 1050–1066, 2024, doi: 10.1109/JSSC.2024.3350240.

[28] J. Shailaja and V. S. V. Prabhakar, "A programmable gain amplifier based on a two-level CNTFET op amp with optimized trans-conductance to drain current ratio," *Analog Integrated Circuits and Signal Processing,* vol. 118, no. 2, pp. 355–369, 2024, doi: 10.1007/s10470-023-02239-8.

[29] F. Khateb, T. Kulej, M. Akbari, and K. T. Tang, "A 0.5-V multiple-input bulk-driven OTA in 0.18 μ CMOS," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 30, no. 11, pp. 1739–1747, 2022, doi: 10.1109/TVLSI.2022.3203148.

[30] M. Kumngern, T. Kulej, V. Stopjakova, and F. Khateb, "0.5 V sixth-order Chebyshev band-pass filter based on multiple-input bulk-driven OTA," *AEU–International Journal of Electronics and Communications,* vol. 111, 2019, doi:

10.1016/j.aeue.2019.152930.
[31] G. D. Colletta, L. H. C. Ferreira, and T. C. Pimenta, "A 0.25-V 22-nS symmetrical bulk-driven OTA for low-frequency G-m-C applications in 130-nm digital CMOS process," *Analog Integrated Circuits and Signal Processing,* vol. 81, no. 2, pp. 377–383, 2014, doi: 10.1007/s10470-014-0385-y.
[32] P. S. Sushma, S. Gaonkar, K. S. Gurumurthy, and A. Fathima, "Design of high gain bulk-driven miller OTA using 180nm CMOS technology," *2016 IEEE International Conference on Recent Trends in Electronics, Information and Communication Technology, RTEICT 2016 - Proceedings,* pp. 1774–1777, 2017, doi: 10.1109/RTEICT.2016.7808139.
[33] A. Namdari, O. Aiello, and D. D. Caviglia, "0.5 V 32nW inverter-based Gm-C filter for bio-signal processing," in *2024 IEEE International Symposium on Circuits and Systems (ISCAS),* IEEE, May 2024, pp. 1–5, doi: 10.1109/ISCAS58744.2024.10558655.
[34] A. Namdari, O. Aiello, and D. D. Caviglia, "A 0.5 V, 32 nW compact inverter-based all-filtering response modes Gm-C filter for bio-signal processing," *Journal of Low Power Electronics and Applications,* vol. 14, no. 3, 2024, doi: 10.3390/jlpea14030040.
[35] R. Della Sala, F. Centurelli, and G. Scotti, "An ultra-low-voltage approach to accurately set the quiescent current of digital standard cells used for analog design and its application on an inverter-based operational transconductance amplifier," *Journal of Low Power Electronics and Applications,* vol. 14, no. 3, 2024, doi: 10.3390/jlpea14030039.

BIOGRAPHIES OF AUTHORS

Udari Gnaneshwara Chary received his Master's degree in 2009 in VLSI systems design from Jawaharlal Nehru Technological University Hyderabad. He works as an Assistant Professor at the B. V. Raju Institute of Technology, Narsapur. He is pursuing a Ph.D. at Koneru Lakshmaiah University (KLEF). He had 15+ years of teaching experience. His research interests include CMOS Analog design, VLSI system design, quantum VLSI architectures, and quantum computing. He has published over 20 papers in reputable journals, core conferences, and book chapters, and has served as a reviewer for SCI-indexed journals and major conferences. He can be contacted at email: gnaneshwarchary@gmail.com.

Dr. Swathi Mummadi is currently an Associate Professor in the Department of Computer Science and Engineering at B V Raju Institute of Technology (BVRIT), Narsapur, and also serves as a Post-Doctoral Researcher at Universiti Malaysia Perlis (UniMAP), Malaysia. She holds a Ph.D. in Quantum Computing and Cryptography from the Department of Information Technology, National Institute of Technology Karnataka (NITK), Surathkal, India. Her B.Tech. and M.Tech. degrees in Computer Science and Engineering were earned from Jawaharlal Nehru Technological University (JNTU), Hyderabad. She has published over 25+ articles in reputed journals, core conferences, and book chapters. Additionally, she has been honored with the Young Researcher Award for her contributions to Quantum Computing, Quantum Excellence Badge, and Quantum Challenge Achievement from IBM, Gold medal in KPIT Shodh Awards 2025, Finalist of Rising Quantum Star Award at Quantum Innovation Summit, Dubai, Teaching Excellence Award and Gold Medal for outstanding performance in faculty colloquium, Merit certificate from IIT Roorkee, and C-DAC India for the QSim course. She also qualified for UGC-NET. She is also a recipient of funding from MeitY, India, for a Quantum Machine Learning Project and served as a reviewer for 100+ SCI Journal papers and core conferences. Her research interests span a variety of topics, including quantum computing, quantum cryptography, quantum machine learning, quantum information, quantum key distribution, quantum cost optimization, blockchain technology, security, algorithms, and future internet architectures. She can be contacted at email: mummadiswathi@gmail.com.

Dr. Kakarla Hari Kishore was born in Vijayawada, Andhra Pradesh, India. He received a B.Tech. (ECE) from JNTUH, M.Tech. from SK University, A.P., India. He received his Ph.D. in VLSI from Koneru Lakshmaiah Education Foundation. He received his postdoctoral fellowship (PDF) in Malaysia. At present, he is working as a Professor in ECE. He has published three papers in IEEE Transactions and more than 121 research articles in International Journals/Conferences, with an H-index of 33. He has filed and published 7 patents and 3 textbooks. He is an editorial board member/reviewer for several international journals/conferences. His research interests include VLSI design, fault tolerance and digital testing, IOT, communications, and signal processing. He is a life member of ISTE and IE. He can be contacted at email: kakarla.harikishore@kluniversity.in.