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Seventeen-level cascaded switched-capacitor multilevel inverter for grid-connected photovoltaic systems

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ABSTRACT

This paper proposes a single-phase photovoltaic (PV) multi-array single DC bus seventeen-level cascaded switched capacitor multi-level inverter (CSC-MLI). Two boost converters are employed to extract maximum power, one for each PV string, and the output of each boost converter is connected to a single DC bus collector. A new 17-level CSC-MLI topology has been proposed to produce seventeen output voltage levels with a boosting ability of 2 times and the capability of limiting the capacitors' inrush current during the capacitors' charging mode. The topology offers a lower total standing voltage (TSV) of 16.5 as well as utilizes a lower number of components compared to conventional inverters. A total harmonic distortion (THD) of only 8.12% is present in the output voltage waveform, which yields a high-quality injected grid current through a simple filter with a THD of 1.18%. This design utilizes the switched-capacitor technique and has a self-voltage balancing feature. A novel hybrid-PWM technique has been implemented on CSC-MLI with a switching frequency of 2.5 kHz. The topology of the 3 kW single-phase 17-level inverter demonstrated commendable steady-state and dynamic performance across a range of test conditions by using MATLAB/Simulink software.

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1. INTRODUCTION

Recently, solar photovoltaic (PV) energy has emerged as a feasible substitute for traditional energy sources. Power converters are essential for converting solar energy into electrical energy [1]. Compared to two-level inverters, multilevel inverters (MLIs) are especially preferred for their enhanced waveform quality, reduced filtering requirements, lowered total harmonic distortion (THD), lower voltage stress across the switches, and low electromagnetic interference (EMI) propagation issue [2], [3]. This leads to lowering the size and expense of MLIs by enabling the use of devices with lower ratings [4]. For grid-connected MLIs, it is important that the output voltage THD meets existing IEEE standards [5]. To do this, an elevate in voltage levels is usually needed, resulting in a corresponding rise in the switches number and components. However, the rise in device count introduces complexity, expenses, and losses, especially when aiming for elevated voltage levels [6]. The neutral point clamped (NPC), flying capacitors (FC), and cascaded H-bridge (CHB) are the most conventional MLI topologies and have been exclusively used and implemented for varied applications [7]. NPC and FC experience issues with DC-link voltage unbalancing and a high count of semiconductor components, especially when the voltage levels are increased [8]. The main limitation of the CHB is the need for a large number of power semiconductor switches and isolated DC sources [9]. Switched capacitor multilevel inverters (SC-MLIs) provide innovative configurations that serve as a superior alternative to conventional

multilevel inverters in terms of overcoming the limitations of existing designs. SC-MLIs have shown promise for PV applications due to their ability to generate a greater number of output voltage levels with fewer power supplies, achieve high voltage gain without the use of inductors or bulky transformers, reduce the components count, and minimize the voltage stress across switches. In recent years, many attempts have been undertaken to devise SC-based MLIs with higher voltage levels to produce a superior staircase counterfeited sinusoidal output voltage waveform with the minimal count of components required. In the context of grid-connected photovoltaic systems, A unique 7-level structure has been proposed that mitigates voltage stress and decreases the switches number [10]. In spite of this, the output voltage of this design has a THD of 16.66%, making it essential to use bigger filters to fulfil the IEEE requirements. A variety of 17-level inverters have been investigated in the literature to achieve a compromise between minimizing switch count and reducing the total harmonic distortion in the output voltage. Various inverter topologies that have been proposed are presented in [11]–[13]. However, these designs suffer from high voltage stress. Traditional approaches to designing a 17-level inverter, such as employing CHB units, necessitate a minimum of eight units connected in series with 32 switches and eight isolated input DC sources, making the system expensive, bulky, and complicated. Alternative 17-level topology that utilizes four bidirectional switches, ten unidirectional switches, four capacitors, and four diodes to produce 17-level output voltage in [14]. This design required an isolated flyback converter to produce two identical isolated DC sources for supplying the proposed inverter. In this modified inverter, the component-to-level ratio is very high, which affects the size, cost, and efficiency of the inverter. On the basis of improved series-parallel conversion, a novel cascaded SCMLI is suggested in [15]. Only 10 switches are needed to generate 17 output levels, but two separate DC sources are needed. Similarly, [16] presents a new 17L inverter with four isolated DC sources. With just one DC supply, 12 switches, five diodes, and four capacitors, the 17-level topology shown in [17] achieved an 8-voltage gain. This structure mitigates voltage stress on devices and has the ability to restrict the high inrush current by employing the quasi-soft charge method. However, it is important to observe that the total standing voltage (TSV) is relatively high. Another 17-L based SCMLI is illustrated in [18], tailored for renewable energy applications. By using fewer switches, capacitors, and drivers, the design simplifies the system while reducing costs. The inverter structure has the ability to self-balance capacitor voltage levels and an inherent voltage-boosting capability with four DC supplies. The configuration in [19] can generate 17 levels of voltage with a single source configuration. It uses five capacitors with five diodes and 10 switches, and it is able to boost the input voltage up to 8 times. While in [20], the inverter has the ability to boost the input voltage up to 4 times by using just 12 switches and 3 capacitors. With ten switches and four isolated DC sources, the topology in [21] presented a novel single-phase MLI based on a cascade connection to produce an output voltage with 17 levels. Additionally, it offers the potential to extend to higher voltage levels by using a cascade connection.

This paper successfully extended a pre-existing nine-level multilevel inverter [22] to a 17-level topology for grid-connected photovoltaic systems with lower THD and the ability to limit the capacitor inrush current. This paper proposed a single-phase 17-level cascaded switched capacitor MLI (CSC-MLI) topology connected to a single DC bus bar collector for a multi-array photovoltaic system with grid integration. The primary objectives of this paper are: i) To achieve a balance between the device count and the output voltage THD with less count of power supplies, addressing a research gap; ii) To generate seventeen output voltage levels with a boosting ability of 2 times using minimum numbers of switches; iii) To minimize the subjected voltage stress and rated current on switches; iv) To achieve self-voltage balancing of capacitors without using auxiliary circuits; and v) To minimize the filtering needs.

This paper is organized as follows: i) Section 2 presents the configuration description of the proposed 17-level CSC-MLI with a single DC bus; ii) The single-phase control methodology is illustrated in section 3; iii) The theoretical analysis of the proposed CSC-MLI is explained in section 4; iv) A comparative study is presented in section 5; v) The results and discussion are shown in section 6; vi) Finally, section 7 presents the conclusion.

2. CONFIGURATION DESCRIPTION

Single-phase photovoltaic multi-array single DC bus bar collector CSC-MLI inverter is illustrated in Figure 1. The configuration depicted in Figure 1 includes independent photovoltaic arrays linked to a single DC bus bar via DC-DC boost converters performing maximum power point tracking (MPPT) independently for each photovoltaic array. The DC bus is then connected to the proposed cascaded switched capacitor multilevel inverter (CSC-MLI). To ensure proper operation of the CSC-MLI, an isolated source must feed each cell of the CSC-MLI. So, flyback DC-DC converters with a turn ratio of 1:1 are put between the DC bus and the individual CSC-MLI cells due to their simplicity, affordability, and buck-boost capability which increases the system's flexibility and operating range. This structure offers the benefit of evenly distributed output power across the cells of CSC-MLI. This configuration is proposed in order to eliminate the drawback of the cascaded structure when the PV arrays suffer from partial shading or non-uniform irradiation, which is the inherent

power imbalance among cells in the case of single-phase systems. And consequently, an imbalance of power among different phases in three-phase systems [23]. This work eliminates the per-cell power imbalance in the CSC-MLI by concentrating all photovoltaic-generated power in a single DC bus. Traditional flyback and boost converters have been used.

2.1. Proposed 17-level CSC-MLI topology description

Figure 1 illustrates CSC-MLI with grid integration for photovoltaic systems. According to this figure, the proposed inverter contains twelve unidirectional switches, six bidirectional switches, four DC-link capacitors $(C_{11}, C_{12}, C_{21}, C_{22})$, four floating capacitors $C_{13}, C_{14}, C_{23}, C_{24}$, four power diodes, and two soft charging inductors (L_{CH_1}, L_{CH_2}) along with freewheeling diodes (D_{f1}, D_{f_2}). The suggested inverter is supplied by two isolated DC sources with a DC-link voltage V_{dc}. In each cell of CSC-MLI, the voltage across each series-connected DC-link capacitor becomes equal to $(V_{dc}/2)$ as they charged to V_{dc}. The strings of floating capacitors are charged to $(V_{dc}/2)$. So, each of them has a voltage equal to $(V_{dc}/4)$, and they remain constant during the operation of the proposed CSC-MLI. The proposed inverter has the ability to limit the capacitor charging current using the soft charging method. In the proposed topology, seventeen distinct levels are generated in the output voltage, involving $\pm 2\,V_{dc}$, $\pm 1.75\,V_{dc}$, $\pm 1.5\,V_{dc}$, $\pm 1.25\,V_{dc}$, $\pm V_{dc}$, $\pm 0.75\,V_{dc}$, $\pm 0.5\,V_{dc}$, $\pm 0.25\,V_{dc}$, and $\pm\,0$ based on the switching states listed in Table 1.

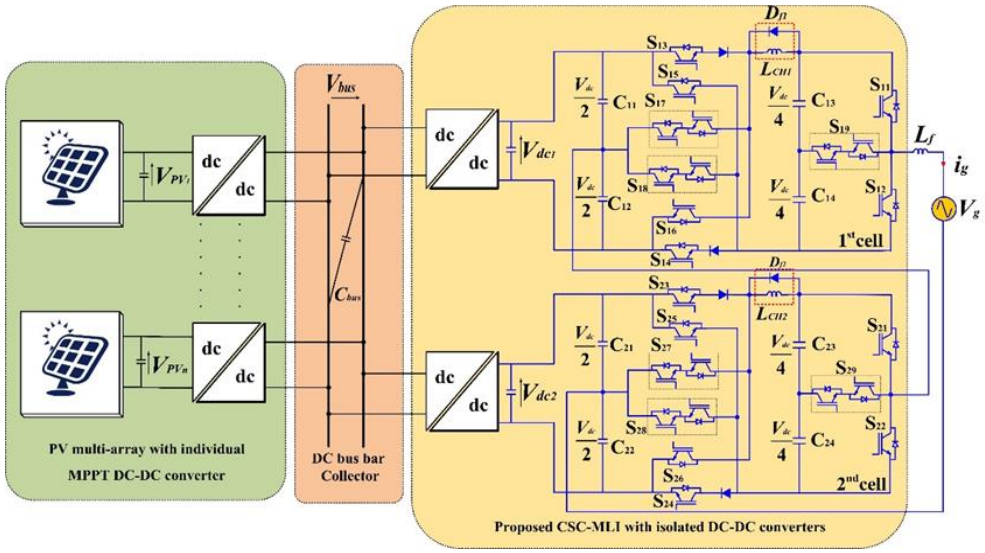

Figure 1. Proposed grid-connected 17-level CSC-MLI

Table 1. Switching states of the proposed 17-level CSC-MLI

Output voltage levels	S_{11}	S_{12}	S_{13}	S_{14}	S_{15}	S_{16}	S_{17}	S_{18}	S_{19}	S_{21}	S_{22}	S_{23}	S_{24}	S_{25}	S_{26}	S_{27}	S_{28}	S_{29}	$V_{C_{13}}$	$V_{C_{14}}$	$V_{C_{23}}$	$V_{C_{24}}$
0	0	1	1	0	0	0	0	1	0	0	1	1	0	0	0	0	1	0	C	C	C	C
$0.25\,V_{dc}$	0	0	1	0	0	0	0	1	1	0	1	1	0	0	0	0	1	0	C	C	C	C
$0.5\,V_{dc}$	1	0	1	0	0	0	0	1	0	0	1	1	0	0	0	0	1	0	C	C	C	C
$0.75\,V_{dc}$	0	0	0	0	1	0	0	0	1	0	1	1	0	0	0	0	1	0	NC	D	C	C
V_{dc}	1	0	0	0	1	0	0	0	0	0	1	1	0	0	0	0	1	0	D	D	C	C
$1.25\,V_{dc}$	1	0	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	C	C	NC	D
$1.5\,V_{dc}$	1	0	0	0	1	0	0	0	0	1	0	1	0	0	0	0	1	0	D	D	C	C
$1.75\,V_{dc}$	0	0	0	0	1	0	0	0	1	1	0	0	0	1	0	0	0	0	NC	D	D	D
$2\,V_{dc}$	1	0	0	0	1	0	0	0	0	1	0	0	0	1	0	0	0	0	D	D	D	D
-0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	C	C	C	C
$-0.25\,V_{dc}$	0	0	0	1	0	0	1	0	1	1	0	0	1	0	0	1	0	0	C	C	C	C
$-0.5\,V_{dc}$	0	1	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	C	C	C	C
$-0.75\,V_{dc}$	0	0	0	0	0	1	0	0	1	1	0	0	1	0	0	1	0	0	D	NC	C	C
$-V_{dc}$	0	1	0	0	0	1	0	0	0	1	0	0	1	0	0	1	0	0	D	D	C	C
$-1.25\,V_{dc}$	0	1	0	1	0	0	1	0	0	0	0	0	0	0	1	0	0	1	C	C	D	NC
$-1.5\,V_{dc}$	0	1	0	1	0	0	1	0	0	0	1	0	0	0	1	0	0	0	C	C	D	D
$-1.75\,V_{dc}$	0	0	0	0	0	1	0	0	1	0	1	0	0	0	1	0	0	0	D	NC	D	D
$-2\,V_{dc}$	0	1	0	0	0	1	0	0	0	0	1	0	0	0	1	0	0	0	D	D	D	D

C = charging, D = discharging, and NC = not change

2.2. Soft charging method

One of the major disadvantages of the switched capacitor-based topologies is the capacitor inrush current during the capacitor's charging mode. So, the current stress on the switches will increase. To solve this issue, a soft charging method has been employed to decrease the capacitor spike current. A soft charging inductor (L_{CH}) in parallel with a freewheeling diode (D_f) is employed in the capacitor charging path to restrict the spike current. The smallest size for the charging inductor is figured out by (1) where C_F represent the floating capacitors and f_g represent the grid frequency [24].

$$L_{CH} = \frac{1}{(2\pi f_g)^2 C_F} \quad (1)$$

The inductor reduces the inrush current; however, it leads to voltage spikes. As a result, diodes (D_{f1}, D_{f_2}) are placed parallel to the inductors to mitigate this overvoltage issue.

2.3. PWM control for proposed 17-level CSC-MLI

To produce the gate pulses for the proposed CSC-MLI, the carrier-based unipolar sine PWM technique has been considered according to the logic circuit given in Figure 2. A single sinusoidal reference signal featuring an inverted negative half-cycle is used alongside eight triangular carrier signals in order to reduce the number of required carrier signals to the half as compared with the noninverted one. Hence, only eight carrier signals rather than 16 are used to compare with the reference signal to produce switching gate pulses for the proposed inverter. Each of the carrier signals has a 2.5 kHz frequency. In this paper, a new hybrid pulse width modulation has been proposed based on a combination of phase-shifted pulse width modulation (PS-PWM) and level-shifted pulse width modulation (LS-PWM).

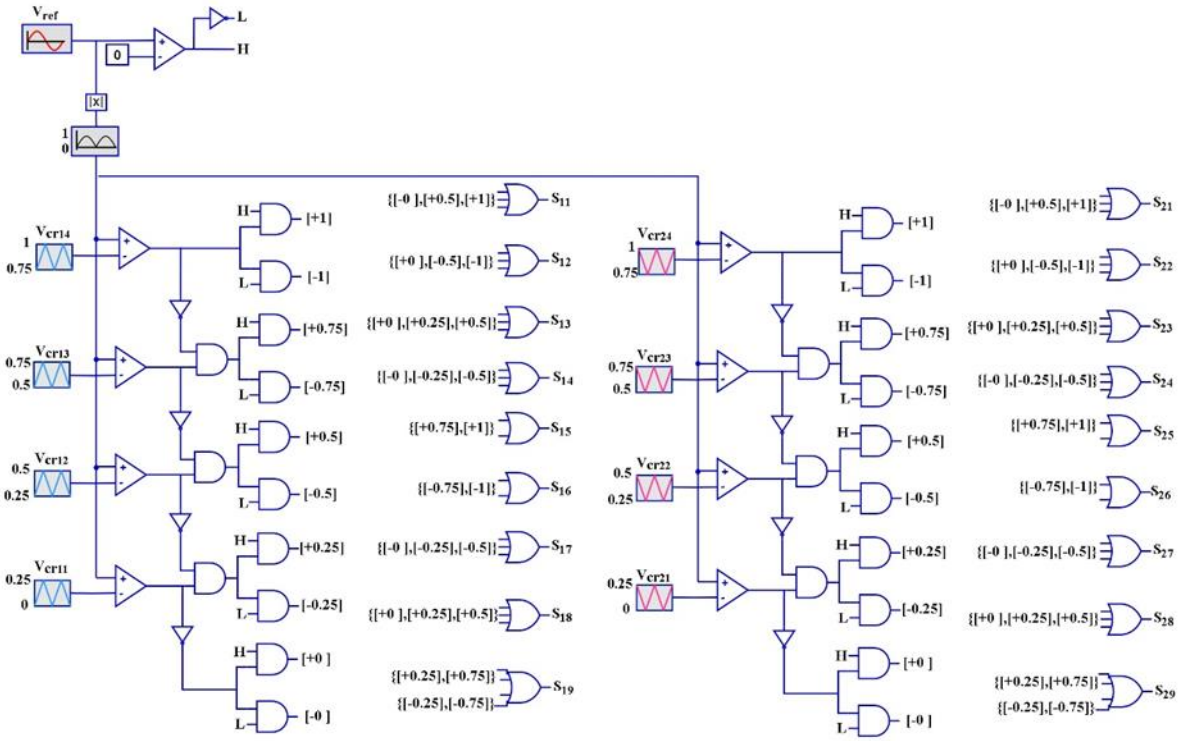

Figure 2. Hybrid-PWM logic circuit for the proposed 17-level CSC-MLI

As shown in Figure 2, the level-shifted carriers ($V_{cr_{11}}, V_{cr_{12}}, V_{cr_{13}}, V_{cr_{14}}$) have the same phase, which is compared with the absolute value of the reference signal to produce the gate pulses for the first cell of CSC-MLI. Similarly, the phase-shifted carrier signals ($V_{cr_{21}}, V_{cr_{22}}, V_{cr_{23}}, V_{cr_{24}}$) whose opposed to level-shifted carriers of the first cell are contrasted with a reference signal to produce the switching pulses for the second cell of CSC-MLI. The comparison between the carrier and reference signals and the produced 17-L inverter output voltage waveform is presented in Figure 3. The modulation index m_a can be calculated as (2).

$$m_a = \frac{\hat{V}_{ref}}{(4\hat{V}_{cr})} \quad (2)$$

Here $\hat{V}_{ref}, and\ \hat{V}_{cr}$ are the peak values of the reference signal and each carrier signal, respectively.

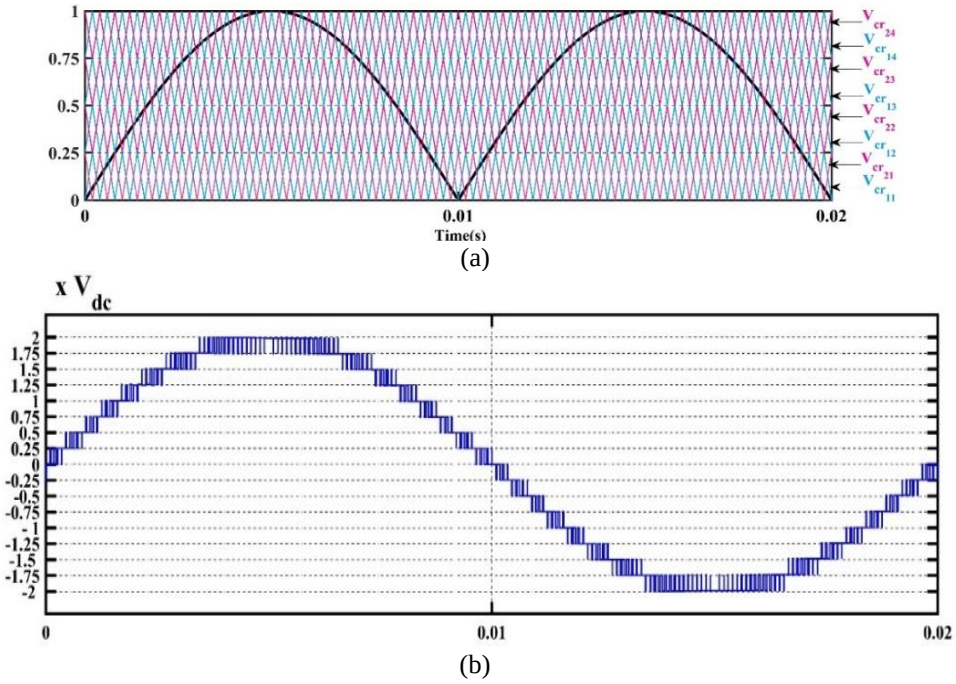

Figure 3. Hybrid-PWM scheme for the proposed CSC-MLI: (a) reference and carrier signals and (b) 17-level CSC-MLI output voltage waveform

3. CONTROL SCHEME

One of the advantages of the presented single-phase photovoltaic multi-array single DC-bus bar CSC-MLI inverter is that the control system can be effectively segmented among the converters utilizing conventional control methodologies. The control scheme of each converter stage is described in the following sections. The MPPT boost converters perform a perturb and observe (P&O) technique by controlling the PV voltages as shown in Figure 4. The P&O MPPT is used due to its simple structure and easy implementation and its algorithm presented in [25]. The reference voltage ($V^*_{pv_k}$) is generated by sensing the PV voltage (V_{pv_k}) and current (I_{pv_k}) for each PV array and used it to perform the MPPT, which is then compared with (V_{pv_k}) and the error is entered into the PI controller for the purpose of providing the required duty cycle for PWM to generate the gate pulses for the boost converter. The input voltage V_{dc} of each CSC-MLI cell is kept constant by adjusting the duty ratio of the flyback switch using PWM based on the output of the PI controller.

The THD level is a significant power quality index for grid-connected photovoltaic inverters. According to both the IEEE and IEC standards, the THD for injected grid current should be less than 5% to minimize negative effects on other users and the grid [26]. So, the current controller must be designed carefully to satisfy this requirement. The CSC-MLI that appears in the third block of Figure 4 is used to control the grid current (i_g) and the single DC bus bar voltage (V_{bus}). In this block, the DC bus voltage (V_{bus}) is compared with the bus reference voltages (V^*_{bus}) and the error is applied to a PI controller with gains K_p = 0.2 and K_i = 1.5. The controller output determines the reference grid current (I^*_g). Then, a phase-locked loop (PLL) technology is employed to synchronize the control system for the purpose of generating the grid reference current (i^*_g) [27]. The grid current (i_g) then is compared with the reference value (i^*_g) and the resulting error signal is applied to a proportional-resonant (PR) current controller with gains K_p = 0.3 and K_r = 15, which is employed rather than a PI controller to get rid of frequencies other than 50 Hz from the current waveform [28]. Finally, the PR controller output is used as the reference voltage and is applied to the hybrid-PWM block.

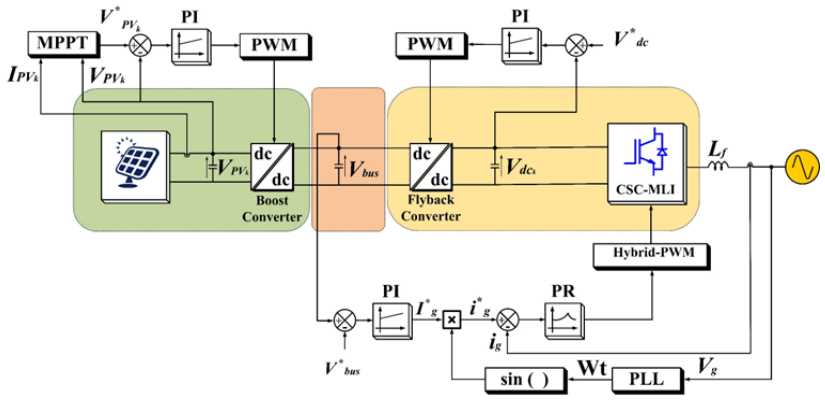

Figure 4. Control block diagram of the proposed CSC-MLI with grid integration for PV system

4. THEORETICAL ANALYSIS

4.1. Voltage and current stress on switching devices

The maximum voltage stress across the switches of the proposed CSC-MLI can be expressed as (3) to (6).

$$V_{S_{19}} = V_{S_{29}} = \frac{V_{dc}}{4} \tag{3}$$

$$V_{S_{11}} = V_{S_{12}} = V_{S_{21}} = V_{S_{22}} = \frac{V_{dc}}{2} \tag{4}$$

$$V_{S_{13}} = V_{S_{14}} = V_{S_{17}} = V_{S_{18}} = V_{S_{23}} = V_{S_{24}} = V_{S_{27}} = V_{S_{28}} = V_{dc} \tag{5}$$

$$V_{S_{15}} = V_{S_{16}} = V_{S_{25}} = V_{S_{26}} = 1.5\, V_{dc} \tag{6}$$

In the proposed CSC-MLI, the charging current (i_c) which has high amplitude flows through the switches (S_{13}, S_{14}, S_{17}, and S_{18}) in the first cell of CSC-MLI and through the switches (S_{23}, S_{24}, S_{27}, and S_{28}) in the second cell. So, the current stress of these switches is high. But the remaining switches carry only the grid current (i_g). The maximum rated current on each switch of CSC-MLI can be mathematically represented as (7) and (8).

$$i_{S_{11}} = i_{S_{12}} = i_{S_{15}} = i_{S_{16}} = i_{S_{19}} = i_{S_{21}} = i_{S_{22}} = i_{S_{25}} = i_{S_{26}} = i_{S_{29}} = i_g \tag{7}$$

$$i_{S_{13}} = i_{S_{14}} = i_{S_{17}} = i_{S_{18}} = i_{S_{23}} = i_{S_{24}} = i_{S_{27}} = i_{S_{28}} = (i_g + i_c) \tag{8}$$

4.2. DC-link and floating capacitance design

The calculation of equivalent DC-link capacitance is (9) [22].

$$C_{Dc-link} = \frac{P_g}{4\pi\, f_g\, V_{dc}\, \Delta V_{dc}} \tag{9}$$

As the DC-link capacitors of each cell are connected in series (10).

$$C_{11} = C_{12} = C_{21} = C_{22} = 2C_{Dc-link} \tag{10}$$

Where P_g represent the injected power to the grid, f_g represent the grid frequency and ΔV_{dc} represent the ripple voltage (5–10% of V_{dc}). The calculation of floating capacitance is (11) [22].

$$C_F = \frac{I_{g,max}}{\Delta V_c\, f_{sw}} \tag{11}$$

As the floating capacitors of each cell are connected in series (12).

$$C_{13} = C_{14} = C_{23} = C_{24} = 2C_F \tag{12}$$

Where $i_{g,max}$ is the maximum magnitude of grid current and ΔV_c is acceptable voltage ripple (2–5% of $\frac{V_{dc}}{4}$) in the floating capacitors.

5. COMPARATIVE STUDY

To demonstrate the effectiveness of the suggested 17-level CSC-MLI, a comparison between the proposed inverter and other existing 17L-MLIs is illustrated in Table 2. The comparison is made in terms of the number of voltage levels (N_{level}), input DC source (N_{dc}), switches (N_{sw}), diodes (N_{dio}), and capacitors (N_{cap}) are taken into account. Additionally, the limitation of capacitor's inrush current capability, connection to the grid and TSV have been included in the comparison. The term TSV is calculated as (13).

$$TSV_{sw} = \sum_{ij=11}^{N_{sw}} V_{S_{ij}} \quad (13)$$

Where the N_{sw} is the switch number and $V_{S_{ij}}$ is the voltage across the switch. TSV is an essential factor in analyzing the feasibility of a topology, as it is an indirect indicator of the switches' ratings.

The higher the TSV, the higher the rating and cost of the used IGBT. Among the presented 17-level topologies, the proposed topology has a superior TSV, which it has a value of 16.5. In [30], topology has a low value of TSV, but it requires a higher number of DC sources. While in [12], [24], TSV value is quite high. Common CHB, NPC, and FC configurations necessitate numerous components to produce 17 voltage levels. This limitation makes them uneconomical for several applications. In [16], [18], [21] 17-level topologies are invented with a lower number of switches but the large number of input DC sources is a drawback of these topologies. Further MLI topologies with a single DC source for 17-level are explored in [12], [14], [17], [20], [32], [33], these designs suffer from high voltage stress. Many presented inverters have a higher gain factor than the proposed one, but they suffer from very high voltage stress across switches, making them unsuitable for high-voltage applications. In comparison to the other structures presented in Table 2, the proposed CSC-MLI demonstrates a notable ability to limit the charging spike current. As mentioned in the above table, it was observed that only the structures presented in [12], [14], [17], [24], [33], can provide this significant feature. In summary, whatever the complexity of the switch arrangements, the number of DC sources, or the high voltage stress, each topology presents its own challenges.

Table 2. Comparison of the proposed topology in relation to other 17-level topologies

Topology	N_{level}	N_{dc}	N_{sw}	N_{dio}	N_{cap}	TSV ($\times V_{dc}$)	Current % THD	Gain factor	Limitation of inrush current	Grid connected
CHB	17	8	32	0	0	32	-	-	-	-
FC	17	2	32	32	16	32	-	-	-	-
NPC	17	2	32	32	16	32	-	-	-	-
[12]	17	1	14	4	4	82	-	8	Yes	No
[14]	17	1	14	4	4	24	-	2	Yes	Yes
[16]	17	4	14	0	4	44	-	4	No	No
[17]	17	1	12	5	4	34	1.6	8	Yes	Yes
[18]	17	4	14	0	2	48	1.62	8	No	No
[20]	17	1	12	2	3	25	2.47	4	No	No
[21]	17	4	10	0	0	36	-	2	-	No
[24]	17	1	13	3	3	53	-	8	Yes	No
[29]	17	2	11	1	3	36	-	1.6	No	No
[30]	17	6	9	3	1	20	-	4	No	No
[31]	17	2	14	2	4	40	-	8	No	No
[32]	17	1	13	3	3	40	-	8	No	No
[33]	17	1	11	1	3	28	-	4	Yes	No
Proposed	17	2	18	4	8	16.5	1.18	2	Yes	Yes

6. RESULTS AND DISCUSSION

A proposed 17-level CSC-MLI-based PV-grid system is simulated using the MATLAB/Simulink platform under different environmental conditions. The PV power injection stage, comprising PV arrays and their corresponding MPPT boost converters, has been simulated by linking their outputs to a single DC bus with a capacitor $C_{bus} = 2500$ µF. On the other side, two flyback converters were employed to supply the CSC-MLI cells. The cells of the proposed inverter have been cascaded and connected to the grid through a $L_f =$ 1mH. The proposed inverter parameters for a 3 kW power system are being considered, with peak inverter output voltage V_{inv}= 340 V at a grid frequency f_g= 50 Hz. The input DC-link voltage V_{dc}= 170 V for each cell and operates with a 2.5 kHz switching frequency.

The specifications of the PV modules for each PV array and the main parameters of the simulated system are summarized in Tables 3 and 4, respectively. Initially, to demonstrate the dynamic performance of the proposed grid-tie system control scheme, the system's performance is evaluated under a solar irradiation step change from 700 to 1000 W/m^2 at t = 1 s. A step change in PV power is illustrated in Figure 5(a). As anticipated, the outer voltage loop effectively regulates the bus bar voltage, as can be noted in Figure 5(b) where the bus voltage exhibits

a slight increase at the instant of the power change before returning to its reference level. The decoupling modulation behavior produced by the DC voltage controller is illustrated in Figure 5(c), which shows that the rise in the bus voltage didn't transfer to any cell voltages. In Figure 5(d) the inverter output voltage with seventeen levels can be observed, proving the accurate implementation of the hybrid-PWM scheme. The injected grid current is shown in Figure 5(e), and it is always in phase with the grid voltage.

Table 3. Specifications of the PV module for each PV array

Parameters	Value
No. of series-connected modules per string (N_s)	4
No. of parallel string (N_p)	6
Maximum power of each module (P_{mpp})	65 W
Maximum current at MPP (I_{mpp})	3.69 A
Maximum voltage at MPP (V_{mpp})	17.6 V
Maximum power of each array (P_{PV})	1560 W

Table 4. Specifications for testing the proposed CSC-MLI

Parameters	Value	Unit	Parameters	Value	Unit
V_{bus}	150	V	C_F, $C_{dc-link}$	3750	µF
$V_{dc_1} = V_{dc_2}$	170	V	f_{sw}	2.5	kHz
V_g	220 (rms)	V	f_g	50	Hz
L_f	1	mH	L_{CH}	1	mH
C_{bus}	2500	µF			

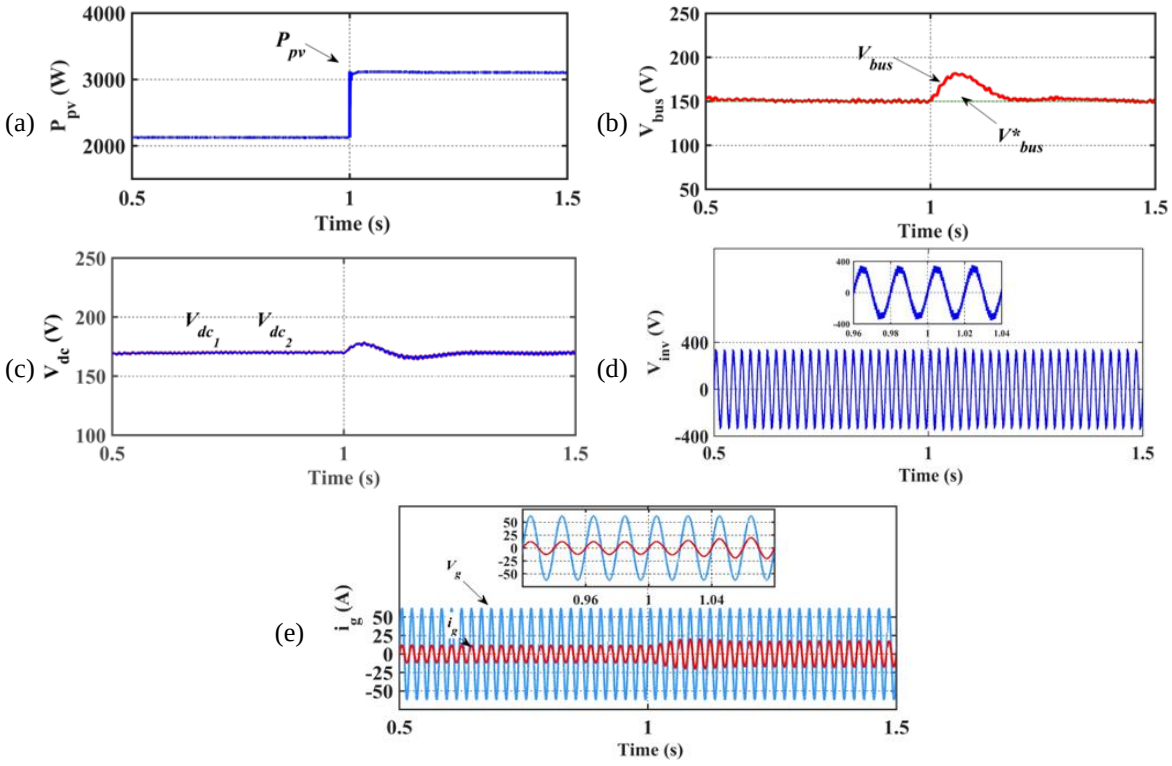

Figure 5. Input power step system results: (a) total PV power, (b) DC bus voltage and reference, (c) per cell DC-link voltage, (d) inverter output voltage, and (e) grid current and scaled grid voltage

A second test, including a step change in the DC bus reference voltage, has been conducted. Figure 6 illustrates the dynamic performance of the CSC-MLI control scheme with grid integration for a reference voltage step from 150 V to 200 V. Figure 6(a) illustrates the increase in DC bus voltage at the instant of the reference step, exhibiting a small overshoot due to a design compromise regarding the controller's speed. In order to get this voltage rise, the reference grid current is reduced slightly for the purpose of using the generated photovoltaic power to charge the DC bus capacitor and then returning to its previous level when the voltage reaches the reference, as seen in Figure 6(b). The input voltage V_{dc} of each CSC-MLI cell exhibits a slight increase at the instant of the DC bus

voltage step before returning to its reference level at 170 V, as noted in Figure 6(c). This is because the voltage loop of flyback converters effectively regulates the input DC-link voltages.

After verifying the proposed inverter control scheme's performance, the proposed grid-tie CSC-MLI for PV systems is tested under varying solar irradiance as shown in Figure 7. An irradiance step from 1000 W/m^2 to 500 W/m^2 is simulated at time 1 s, which is subsequently increased to 1000 W/m^2 at the time of 2 s. Under such varying irradiance conditions, the waveform of PV power P_{pv} is shown in Figure 7(a). The peak magnitudes of total generated PV power P_{pv} of both PV arrays are 3.11 kW and 1.48 kW, corresponding to 1000 $W/m^2$and 500 W/m^2 respectively. It is illustrated in Figure 7(b) that the grid current i_g is decreased as the irradiance decreases. The maximum magnitude of i_g reduces from 18.25 A to 8.25 A when irradiance decreases from 1000 W/m^2 to 500 W/m^2 and it is always in phase with the grid voltage. The voltages across floating capacitors are shown in Figure 7(c). They are always equal and constant to $V_{dc}/4$ and both are balanced despite the changing of the injected grid current. The voltages across C_{13} and C_{14} are maintained at 42.5 V regardless of the changing of solar irradiation, with a voltage peak-to-peak ripple equal to 10 V and 5 V corresponding to 1000 W/m^2 and 500 W/m^2 solar irradiance, respectively. As the CSC-MLI cells are identical, hence voltage waveforms across the floating capacitors of the first cell are considered.

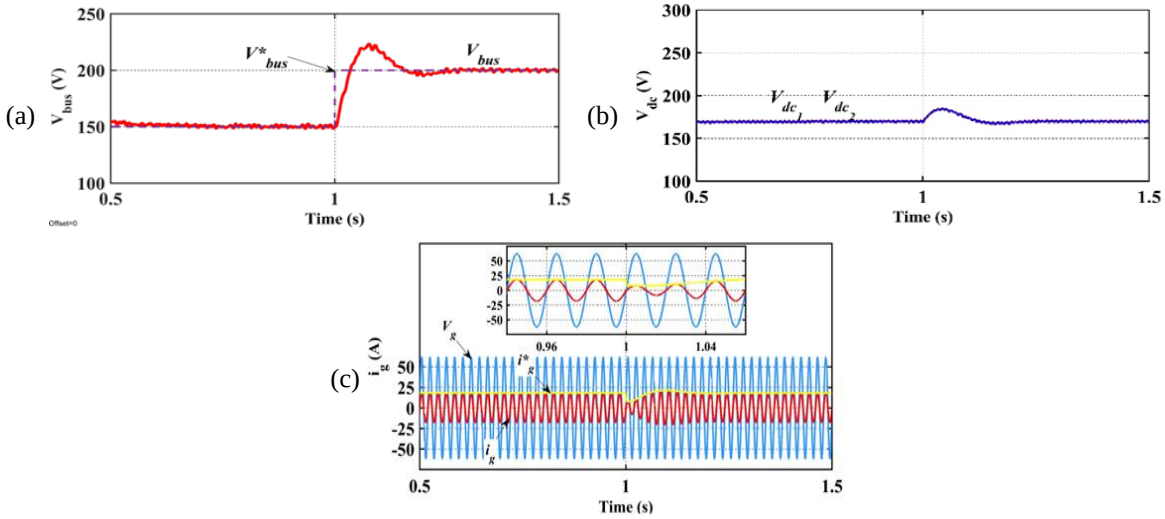

Figure 6. DC bus voltage step system results: (a) bus voltage and reference, (b) per-cell DC-link voltages, and (c) grid current and reference, with scaled grid voltage

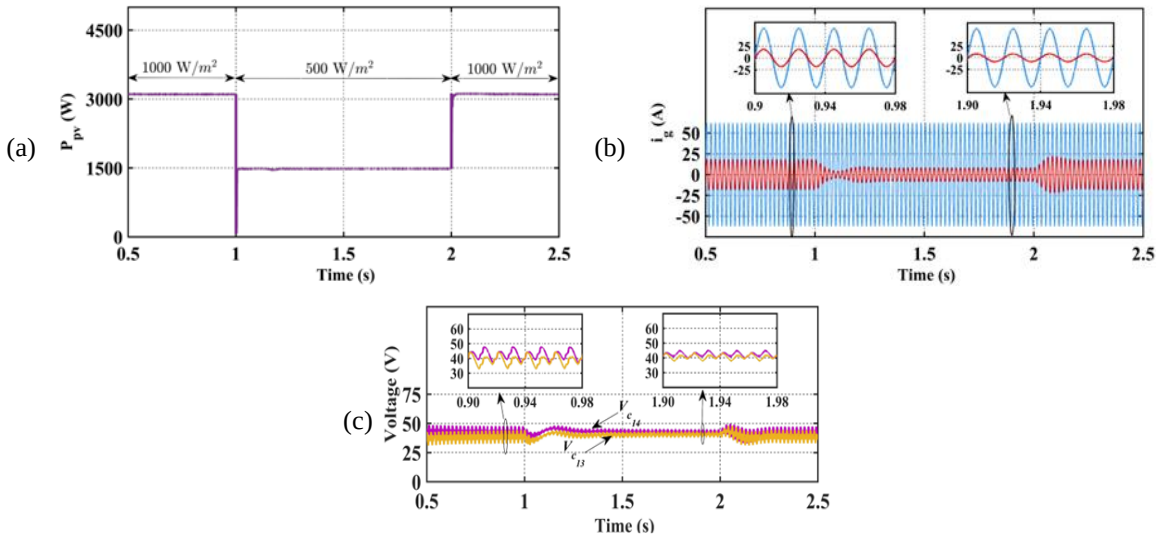

Figure 7. Varying solar irradiance results: (a) total PV power, (b) grid current and scaled grid voltage, and (c) voltage across floating capacitors

The performance of the CSC-MLI with grid integration under steady-state conditions is illustrated in Figure 8. During a steady-state condition, the irradiation is consistently maintained at $1000\ \mathrm{W/m^2}$. The total generated PV power P_{pv} is 3.11 kW and its waveform is shown in Figure 8(a). The inverter output voltage V_{inv} and injected current to the grid with scaled grid voltage are depicted in Figures 8(b) and 8(c), respectively. The peak magnitude of V_{inv} and i_g is 340 V and 18.25 A, respectively. Seventeen voltage levels of equal magnitude are present in the waveform of the V_{inv}, which verifies the correct implementation of the hybrid-PWM scheme. The waveforms of both V_g and i_g is smooth and sinusoidal, and they are always in phase.

As mentioned, one of the most crucial issues of the switched capacitor inverter can be solved by the proposed inverter by employing a soft charging method to restrict the capacitor spike current. As the current waveforms across DC-link capacitors and floating capacitors for both cells are identical, only the first cell is considered in Figures 8(d)-8(e), currents flowing through the DC-link capacitors and the floating capacitors, respectively. Based on these figures, the maximum current through C_{11} and C_{12} is 40 A and 50 A, respectively. While Figure 8(e) displays the current through the capacitor C_{13} and C_{14} with a peak value of 50 A, which verifies the soft charging method. Therefore, the results indicate that the inclusion of the charging inductors in the charging paths has significantly restricted the inrush current. Considering that the grid current is 18.25 A.

Additional investigations of the power quality supplied to the grid have been conducted through THD of the injected grid current, as shown in Figure 9(a). The THD of the inverter output voltage V_{inv} has been shown in Figure 9(b). The %THD content in the injected grid current and the inverter output voltage is measured as 1.18% and 8.12%, respectively, which is according to the IEEE standard, demonstrating the high quality of the current.

The stress voltage across switches of the proposed CSC-MLI is considered for the input DC-link voltage V_{dc}= 170 V. As the cells of the proposed CSC-MLI are identical, from Figures 10(a)-10(c), it has been noticed that the maximal voltage stress across switches of the first cell S_{11}, S_{12}, and S_{19}, is 85 V, 85 V, and 42.5 V, respectively. S_{15} and S_{16}, show a maximum stress of 255 V, and the rest switches have a stress voltage equal to the input DC-link voltage of 170 V. The results indicate that the proposed CSC-MLI operates effectively in both steady-state and dynamic conditions.

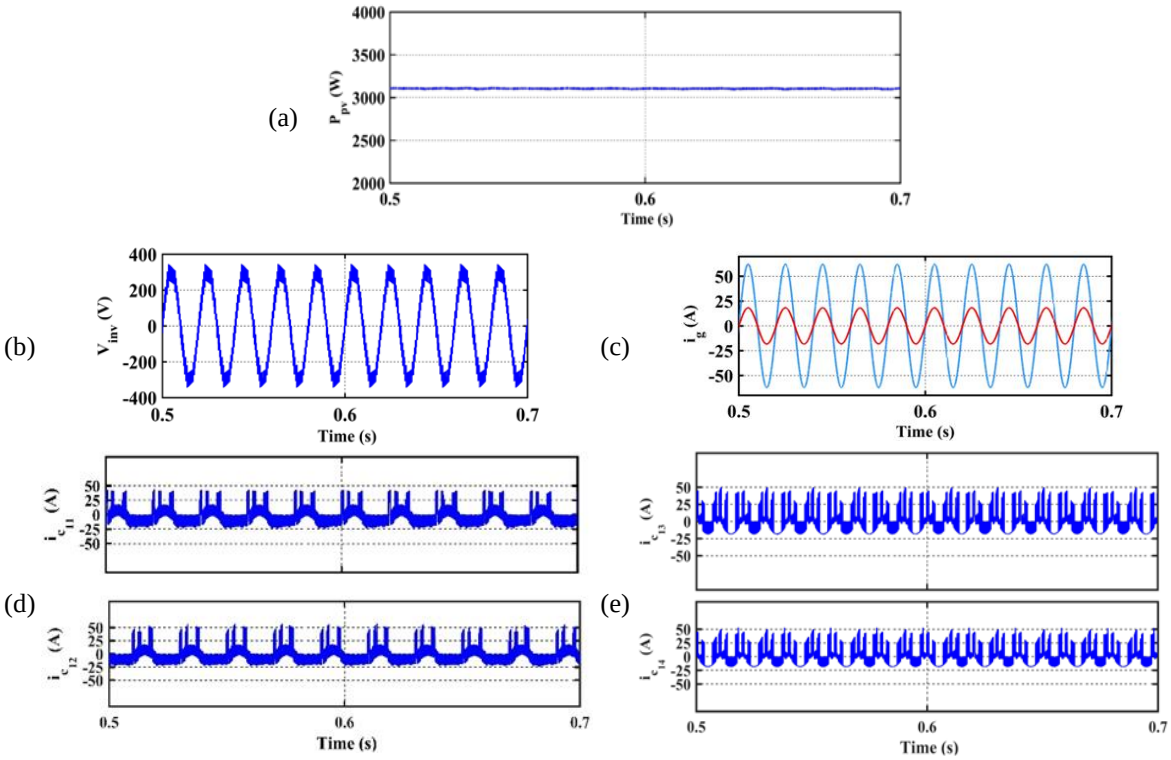

Figure 8. Results under steady-state conditions: (a) total PV power, (b) inverter output voltage, (c) grid current and scaled grid voltage, (d) DC-link capacitors current, and (e) floating capacitors current

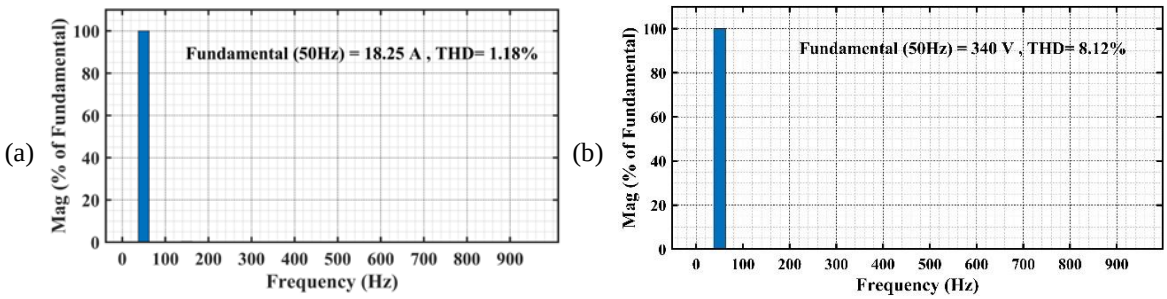

Figure 9. Harmonic spectrum of (a) grid current and (b) inverter output voltage

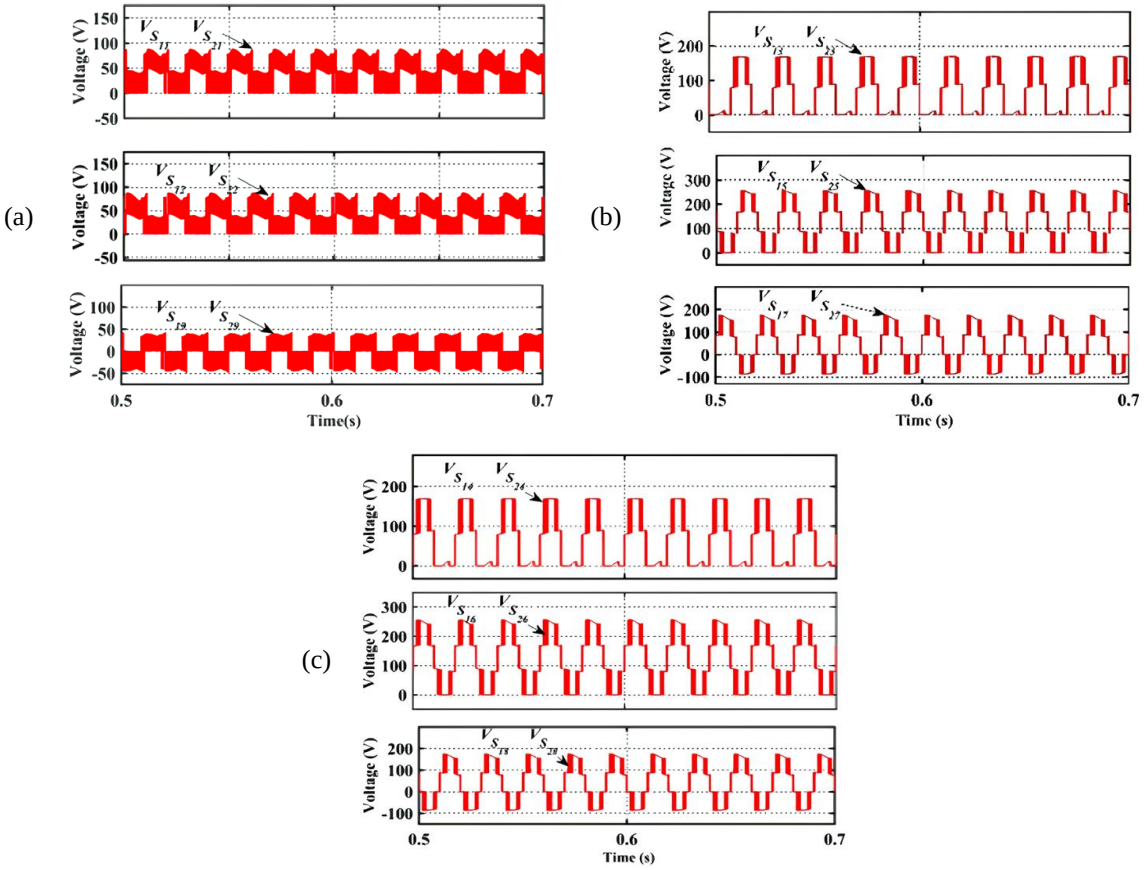

Figure 10. Voltage stress of the proposed inverter across switches (a) S_{11}, S_{21}, S_{12}, S_{22}, S_{19}, and S_{29}; (b) S_{13}, S_{23}, S_{15}, S_{25}, S_{17}, and S_{27}; and (c) S_{14}, S_{24}, S_{16}, S_{26}, S_{18}, and S_{28}

7. CONCLUSION

In conclusion, a new 17-level cascaded switched capacitor multilevel inverter (CSC-MLI) topology has been proposed to comply with IEEE standards for low THD in grid-tied inverters. The new design effectively balances the trade-off between increasing output voltage levels to minimize harmonics and subsequent rise in device count. For the switching scheme, a novel hybrid-PWM is proposed to produce the gate pulses for the proposed CSC-MLI. It has been observed that the proposed structure provides minimum TSV as compared to other structures. Other significant characteristics of the suggested construction include inherent voltage-boosting ability and self-capacitor voltage balancing capacity. In addition, the inrush current during the capacitor charging mode is limited by using a soft charging inductor. The simulation results indicate that the proposed CSC-MLI obtains a THD of 1.18% in its output current that is injected into the grid. The performance of the proposed grid-tied inverter, in both steady-state and dynamic scenarios, is simulated under various environmental conditions using MATLAB/Simulink software.

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AUTHOR CONTRIBUTIONS STATEMENT

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Turki Kahawish Hassan		✓		✓		✓				✓	✓	✓		

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest

DATA AVAILABILITY

The data that support the findings of this study are available on request from the corresponding author, [MJN].

REFERENCES

[1] A. T. Mohsin and I. M. Abdulbaqi, "Analysis of an irrigation pump driver fed by solar PV panel," in *2018 1st International Scientific Conference of Engineering Sciences-3rd Scientific Conference of Engineering Science*, 2018, pp. 92–97. doi: 10.1109/ISCES.2018.8340534.

[2] A. Salem, H. Van Khang, K. G. Robbersmyr, M. Norambuena, and J. Rodriguez, "Voltage Source multilevel inverters with reduced device count: topological review and novel comparative factors," *IEEE Transactions on Power Electronics*, vol. 36, no. 3, pp. 2720–2747, Mar. 2021, doi: 10.1109/TPEL.2020.3011908.

[3] A. K. Hannan and T. K. Hassan, "Hybrid modular multilevel converter for vector-controlled induction motor drive," *Journal of Engineering and Sustainable Development*, vol. 24, no. special, pp. 143–154, Aug. 2020, doi: 10.31272/jeasd.conf.1.16.

[4] S. K. Baksi, U. Ranjan Muduli, R. K. Behera, K. Al Hosani, K. Al Jaafari, and D. Wenzhong Gao, "Reduced switch count three-phase five-level boosted ANPC inverter with unipolar PWM Scheme for electric vehicle propulsion drive," in *IECON 2021 – 47th Annual Conference of the IEEE Industrial Electronics Society*, Oct. 2021, pp. 1–6. doi: 10.1109/IECON48115.2021.9589916.

[5] S. A. Khalid Hailan and R. G. Omar, "Harmonics Compensation for grid connected to PV system using two-step finite set predictive control," in *2022 Iraqi International Conference on Communication and Information Technologies (IICCIT)*, Sep. 2022, pp. 184–189. doi: 10.1109/IICCIT55816.2022.10010543.

[6] P. R. Bana, K. P. Panda, S. Padmanaban, and G. Panda, "Extendable Switched-capacitor multilevel inverter with reduced number of components and self-balancing capacitors," *IEEE Transactions on Industry Applications*, vol. 57, no. 3, pp. 3154–3163, May 2021, doi: 10.1109/TIA.2020.3018422.

[7] S. Kouro *et al.*, "Recent Advances and industrial applications of multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010, doi: 10.1109/TIE.2010.2049719.

[8] J. S. Mohd.Ali and V. Krishnaswamy, "An assessment of recent multilevel inverter topologies with reduced power electronics components for renewable applications," *Renewable and Sustainable Energy Reviews*, vol. 82, pp. 3379–3399, 2018, doi: 10.1016/j.rser.2017.10.052.

[9] X. Sun, B. Wang, Y. Zhou, W. Wang, H. Du, and Z. Lu, "A single DC source cascaded seven-level inverter integrating switched-capacitor techniques," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 11, pp. 7184–7194, Nov. 2016, doi: 10.1109/TIE.2016.2557317.

[10] S. K. Baksi and R. K. Behera, "A Reduced switch count seven-level boost ANPC based grid following inverter topology with photovoltaic integration," *IEEE Transactions on Industry Applications*, vol. 59, no. 4, pp. 4238–4251, Jul. 2023, doi: 10.1109/TIA.2023.3259943.

[11] D. K. Patel, V. P. Pal, K. Baitha, and D. Kumar, "A novel 17-level switched-capacitor multilevel inverter with reduced device count," in *2022 2nd International Conference on Emerging Frontiers in Electrical and Electronic Technologies (ICEFEET)*, Jun. 2022, pp. 1–6. doi: 10.1109/ICEFEET51821.2022.9847689.

[12] J. S. Mohamed Ali, D. J. Almakhles, and M. F. Elmorshedy, "High boost seventeen-level switched capacitor inverter topology with continuous input current," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 3, pp. 2742–2754, Jun. 2023, doi: 10.1109/JESTPE.2022.3230047.

[13] M. A. Rezaei, M. Nayeripour, J. Hu, S. S. Band, A. Mosavi, and M.-H. Khooban, "A New hybrid cascaded switched-capacitor reduced switch multilevel inverter for renewable sources and domestic loads," *IEEE Access*, vol. 10, pp. 14157–14183, 2022, doi: 10.1109/ACCESS.2022.3146256.

[14] M. G. Marangalu, N. V. Kurdkandi, S. H. Hosseini, H. Tarzamni, M. Dahidah, and M. Sarhangzadeh, "A modified switched-capacitor based seventeen-level inverter with reduced capacitor charging spike for RES applications," *IEEE Open Journal of Power Electronics*, vol. 4, pp. 579–602, 2023, doi: 10.1109/OJPEL.2023.3302282.

[15] E. Zamiri, N. Vosoughi, S. H. Hosseini, R. Barzegarkhoo, and M. Sabahi, "A new cascaded switched-capacitor multilevel inverter based on improved series–parallel conversion with less number of components," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 6, pp. 3582–3594, Jun. 2016, doi: 10.1109/TIE.2016.2529563.
[16] C. Dhanamjayulu, D. Prasad, S. Padmanaban, P. K. Maroti, J. B. Holm-Nielsen, and F. Blaabjerg, "Design and implementation of seventeen level inverter with reduced components," *IEEE Access*, vol. 9, pp. 16746–16760, 2021, doi: 10.1109/ACCESS.2021.3054001.
[17] V. Anand *et al.*, "Seventeen level switched capacitor inverters with the capability of high voltage gain and low inrush current," *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, vol. 4, no. 4, pp. 1138–1150, Oct. 2023, doi: 10.1109/JESTIE.2023.3291996.
[18] S. Majhee, T. Roy, A. Chakraborty, and T. N. S. C. Sekhar, "Analysis and development of a novel step-up 17 level switched capacitor multilevel inverter for renewable energy conversion system," in *2019 IEEE International Conference on Electrical, Computer and Communication Technologies (ICECCT)*, Feb. 2019, pp. 1–6. doi: 10.1109/ICECCT.2019.8869420.
[19] S. Deliri, K. Varesi, Y. P. Siwakoti, and F. Blaabjerg, "Generalized diamond-type single DC-source switched-capacitor based multilevel inverter with step-up and natural voltage balancing capabilities," *IET Power Electronics*, vol. 14, no. 6, pp. 1208–1218, May 2021, doi: 10.1049/pel2.12111.
[20] K. Panda, P. Bana, O. Kiselychnyk, J. Wang, and G. Panda, "A single-source switched-capacitor-based step-up multilevel inverter with reduced components," *IEEE Transactions on Industry Applications*, vol. 57, no. 4, pp. 3801–3811, 2021, doi: 10.1109/TIA.2021.3068076.
[21] J. Sathik Mohamed Ali *et al.*, "A New generalized multilevel converter topology based on cascaded connection of basic units," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 4, pp. 2498–2512, 2019, doi: 10.1109/JESTPE.2018.2885209.
[22] S. K. Baksi, R. K. Behera, and U. R. Muduli, "Optimized 9-level switched-capacitor inverter for grid-connected photovoltaic systems," *IEEE Transactions on Industry Applications*, vol. 60, no. 2, pp. 3284–3296, 2024, doi: 10.1109/TIA.2023.3332059.
[23] T. K. Hassan, "Reduction of single DC bus capacitance in photovoltaic cascaded multilevel converter," *International Journal of Power Electronics and Drive Systems (IJPEDS)*, vol. 11, no. 3, p. 1660, Sep. 2020, doi: 10.11591/ijpeds.v11.i3.pp1660-1674.
[24] A. Choudhary, A. K. Singh, R. K. Mandal, and A. K. Saha, "Switched capacitor inverter with reduced inrush current and high boosting gain," *Energies*, vol. 17, no. 13, p. 3064, Jun. 2024, doi: 10.3390/en17133064.
[25] N. Femia, G. Petrone, G. Spagnuolo, and M. Vitelli, "Optimization of perturb and observe maximum power point tracking method," *IEEE Transactions on Power Electronics*, vol. 20, no. 4, pp. 963–973, Jul. 2005, doi: 10.1109/TPEL.2005.850975.
[26] Y. Yang, K. Zhou, and F. Blaabjerg, "Current harmonics from single-phase grid-connected inverters—examination and suppression," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 1, pp. 221–233, doi: 10.1109/JESTPE.2015.2504845.
[27] A. Choudhary and R. K. Mandal, "A Single-stage closed loop control of sc-based inverter," *Electric Power Components and Systems*, vol. 52, no. 5, pp. 811–827, Mar. 2024, doi: 10.1080/15325008.2023.2236095.
[28] D. N. Zmood and D. G. Holmes, "Stationary frame current regulation of PWM inverters with zero steady-state error," *IEEE Transactions on Power Electronics*, vol. 18, no. 3, pp. 814–822, May 2003, doi: 10.1109/TPEL.2003.810852.
[29] M. S. Bin Arif *et al.*, "An improved asymmetrical multi-level inverter topology with boosted output voltage and reduced components count," *IET Power Electronics*, vol. 14, no. 12, pp. 2052–2066, Sep. 2021, doi: 10.1049/pel2.12119.
[30] P. R. Bana, K. P. Panda, and G. Panda, "Power Quality Performance evaluation of multilevel inverter with reduced switching devices and minimum standing voltage," *IEEE Transactions on Industrial Informatics*, vol. 16, no. 8, pp. 5009–5022, Aug. 2020, doi: 10.1109/TII.2019.2953071.
[31] R. Barzegarkhoo, M. Moradzadeh, E. Zamiri, H. Madadi Kojabadi, and F. Blaabjerg, "A new boost switched-capacitor multilevel converter with reduced circuit devices," *IEEE Transactions on Power Electronics*, vol. 33, no. 8, pp. 6738–6754, Aug. 2018, doi: 10.1109/TPEL.2017.2751419.
[32] M. Hosseinpour, M. Noori, and M. Shahparasti, "A 17-level octuple boost switched-capacitor inverter with lower voltage stress on devices," *Scientific Reports*, vol. 14, no. 1, p. 14411, Jun. 2024, doi: 10.1038/s41598-024-65211-0.
[33] M. Hosseinpour, M. Derakhshandeh, A. Seifi, and M. Shahparasti, "A 17-level quadruple boost switched-capacitor inverter with reduced devices and limited charge current," *Scientific Reports*, vol. 14, no. 1, p. 6233, Mar. 2024, doi: 10.1038/s41598-024-56717-8.

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