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# Performance analysis of a cascaded dual full bridges 5, 7, and 9 levels inverter: experimental validation

**Nabil Saidani, Rachid El Bachtiri, Abdelaziz Fri, Karima El Hammoumi**
REEPER Group, Innovative Technology and Computing Laboratory, Higher School of Technology,
Sidi Mohammed Ben Abdellah University (USMBA), Fez, Morocco

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**ABSTRACT**

Cascaded full-bridge inverter is a suitable topology for grid-connected applications due to its ability to generate an output voltage waveform that closely resembles a sine wave, resulting in lower total harmonic distortion (THD) factors. This article proposes the use of the selective harmonic elimination (SHE) technique to produce a 5-level voltage using a symmetrical inverter and 7 and 9-level voltage using an asymmetrical inverter composed of only two full bridges loaded by an RL circuit of 51.4 Ω and 200 mH. The study primarily focuses on analysing the impact of the number of levels on the power quality of the inverter. This includes investigating the effects of the fundamental magnitude on the produced power, as well as measuring losses in the inverter, power factor, THD factor, and fundamental magnitude for each level configuration. The study demonstrates that asymmetrical MLIs lower THD (10.9% vs. 16.7%) and increasing voltage levels enhance waveform quality but slightly reduce the fundamental voltage magnitude, impacting AC power output. The simulation analysis has been conducted using the PSIM environment, and the results have been validated through experimental measurements.



***Corresponding Author:***

Nabil Saidani
REEPER Group, Innovative Technology and Computing Laboratory, Higher School of Technology
Sidi Mohammed Ben Abdellah University (USMBA)
Fez 30000, Morocco
Email: nabil.saidani@usmba.ac.ma

## 1. INTRODUCTION

Multilevel inverters (MLIs) are advanced DC-to-AC converters that generate output voltage waveforms with multiple discrete levels, significantly reducing harmonic distortion and enhancing power quality [1]-[5]. One of the most promising architectures is based on cascaded full-bridge modules, which offer scalability and modularity, enabling high-voltage, high-power applications with improved efficiency and lower THD [6]-[9]. Recent research has extensively explored various MLI topologies, control strategies, and optimization techniques, highlighting their technical advantages and potential for diverse industrial applications [10]-[12].

MLIs are generally classified into two categories: symmetrical and asymmetrical. In a symmetrical MLI, each cascaded full-bridge is supplied by an identical DC voltage source, ensuring uniform voltage steps and a straightforward design [13], [14]. However, this uniformity may limit the achievable number of voltage levels and flexibility in design. In contrast, asymmetrical MLIs utilize different DC voltage levels for each full-bridge module, which allows for the generation of additional voltage steps and can further improve the quality of the output waveform [15], [16]. This approach, while offering enhanced resolution and potentially lower THD, introduces additional complexity in terms of DC source management and control [17].

The control of a multilevel inverter can be achieved through various techniques, one of which is the selective harmonic elimination (SHE) method [18]-[20]. The SHE technique enables the elimination of lower-order harmonics that have significant amplitudes [21]-[23]. Its principle is based on using "n" switching angles to control the amplitude of the fundamental component and cancel out "n-1" harmonics [24], [25]. In our study, we will take advantage of these "n" switching angles to eliminate as many harmonics as possible and investigate how this influences the fundamental component and the overall power quality delivered by the inverter [26].

The main contribution of this work is the practical validation and performance analysis of both symmetrical and asymmetrical MLIs. We conduct a detailed comparative study by evaluating key performance metrics—including total harmonic distortion (THD), switching and conduction losses, and the relationship between AC power, the fundamental voltage magnitude, and power factor, across configurations with 5, 7, and 9 voltage levels. By combining simulation and experimental results, our study bridges the gap between theoretical research and practical implementation, providing valuable insights into the trade-offs and benefits of each MLI configuration for real-world applications.

## 2. DESIGN AND DESCRIPTION

This study focuses on a multilevel inverter that consists of two full-bridge modules (FB1 and FB2) connected in series, as shown in Figure 1. Each full bridge is powered by its own DC voltage source, labelled E1 and E2. In this section, we explain how we determine the DC voltage values for each full bridge, and outline the process for finding the switching angles using the SHE technique to generate five-, seven-, and nine-level voltage waveforms.

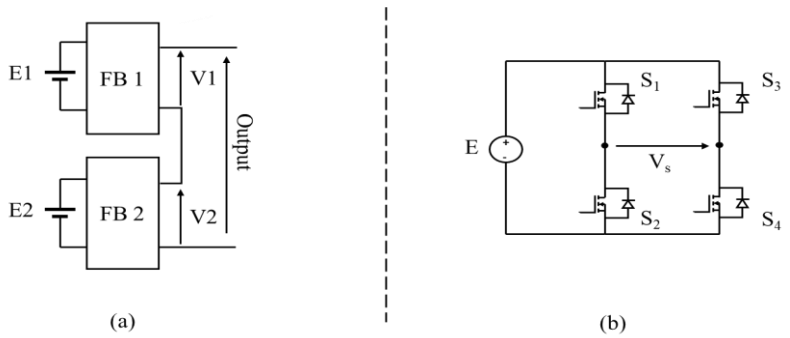



Figure 1. Block diagram of the multilevel inverter: (a) cascaded full bridges and (b) circuit diagram of the full bridge

### 2.1. Determination of the DC source value of each configuration

a. Design constraints
   - Step voltage: Identical voltage steps between consecutive levels to ensure harmonic reduction.
   - Maximum output voltage: Fixed at $E_{max}$=31.1 V, scaled down by a factor of 10 from the nominal grid peak voltage (311 V for a 220 $V_{RMS}$ system).

   For each case, we use a pair of equations derived from the level expressions.

b. Symmetrical configuration (5-level): For the symmetrical case (E1=E2=E), the output voltage levels are −2E, −E, 0, E, 2E as shown in Figure 2. The DC source voltages are derived using (1).

$$\begin{cases} E1 + E2 = E_{max} = 31.1V \\ E1 = \frac{E_{max}}{2} = 15.55V \end{cases} \quad \Rightarrow \quad E1 = E2 = 15{,}55V \tag{1}$$

c. Asymmetrical configuration (7-level): For seven-level, an asymmetrical configuration (E2>E1) generates additional voltage levels: −E1−E2, −E2, −E1, 0, E1, E2, E1+E2 (Figure 3). The DC sources are determined by solving (2).

$$\begin{cases} E1 + E2 = \mathrm{E}_{max} = 31.1V \\ E1 = \frac{\mathrm{E}_{max}}{3} = 10.3V \end{cases} \quad \Rightarrow \quad \begin{cases} E1 = 10.3V \\ E2 = 20.7V \end{cases} \tag{2}$$

d. Asymmetrical configuration (9-Level): To achieve nine levels as shown in Figure 4(−E1−E2, −E2, E1−E2, −E1, 0, E1, E2−E1, E2, E1+E2). The DC sources are calculated using (3).

$$\begin{cases} E1 + E2 = E_{max} = 31.1V \\ E2 - E1 = \frac{E_{max}}{2} = 15.5V \end{cases} \Rightarrow \begin{cases} E1 = 7.7V \\ E2 = 23.3V \end{cases} \quad (3)$$

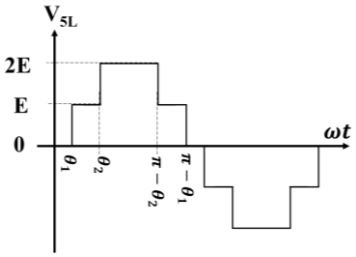



Figure 2. Five-level output voltage waveform

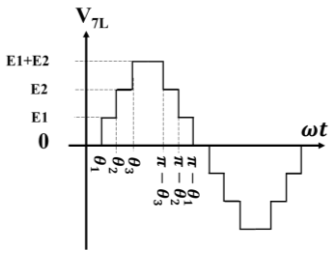



Figure 3. Seven-level output voltage waveform

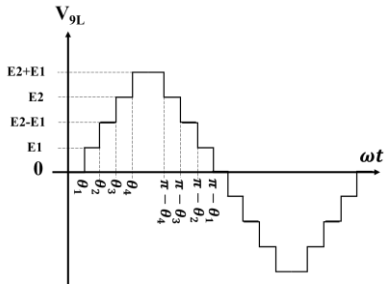



Figure 4. Seven-level output voltage waveform

### 2.2. Determination of the switching angles

The selective harmonic elimination technique involves decomposing the output voltage waveform into a Fourier series and determining the appropriate switching angles to eliminate specific harmonics. The technique becomes more effective as the number of switching angles increases, enabling the elimination of a greater number of harmonics. The fourier series decomposition (FSD) of the inverter's output voltage can be derived by following the steps below. First, we consider that the output voltage waveform of the inverter is composed of a sum of distinct rectangular pulses, as illustrated in Figure 5.

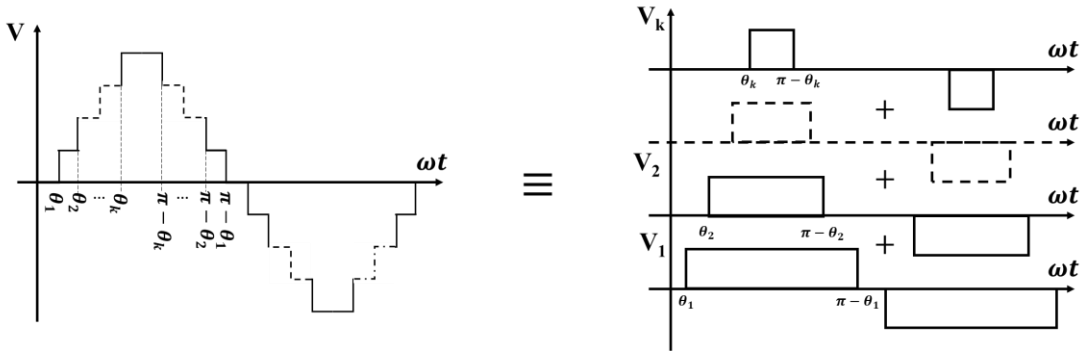



Figure 5. Output voltage expressed as a sum of partial waveforms Vi

From this observation, the output voltage $V$ (4) can be expressed as the sum of elementary voltage $V_i$:

$$V = V_1 + V_2 + \cdots + V_k \quad (4)$$

Each component $V_i$ corresponds to a voltage segment (Figure 6) defined by a specific switching angle $\theta_i$, and each of them has odd symmetry. Therefore, their Fourier Series decomposition (5) contains only sine terms and can be written as (5):

$$V_i(t) = \sum_{n=1}^{+\infty} b_n^i . sin\ (n\omega_0 t) \quad (5)$$

where $b_n^i$ are the Fourier coefficients for the $i$-th segment and are given by (6).

$$b_n^i = \frac{4}{2\pi} \int_{\theta_i}^{\pi-\theta_i} V_{max} . sin(n\omega_0 t)\, . dt \quad (6)$$

The (7) represents the solution of (6).

$$b_n^i = \frac{2V_{max}}{n\pi}\left(cos(n\theta_i) - cos\left(n(\pi - \theta_i)\right)\right) \quad (7)$$

This means the total output voltage $V(t)$ becomes (8).

$$V(t) = \sum_{i=1}^{k} V_i = \sum_{i=1}^{k}\left(\sum_{n=1}^{+\infty} b_n^i . sin(n\omega_0 t)\right) \quad (8)$$

We can rearrange (8) to (9).

$$V(t) = \sum_{n=1}^{+\infty}\left(\sum_{i=1}^{k} b_n^i\right) sin(n\omega_0 t) \quad (9)$$

Thus, the $n$-th harmonic component of the output voltage is given by (10) and (11).

$$V_n(t) = \left(\sum_{i=1}^{k} b_n^i\right) sin(n\omega_0 t) \quad (10)$$

$$V_n(t) = \frac{2V_{max}}{n\pi} . \left(\sum_{i=1}^{k}\left(cos(n\theta_i) - cos\left(n(\pi - \theta_i)\right)\right)\right) sin(n\omega_0 t) \quad (11)$$

The amplitude of the n[th] harmonic, noted Bn, is (12).

$$Bn = \left(\sum_{i=1}^{k} b_n^i\right) = \frac{2V_{max}}{n\pi} . \left(\sum_{i=1}^{k}\left(cos(n\theta_i) - cos\left(n(\pi - \theta_i)\right)\right)\right) \quad (12)$$

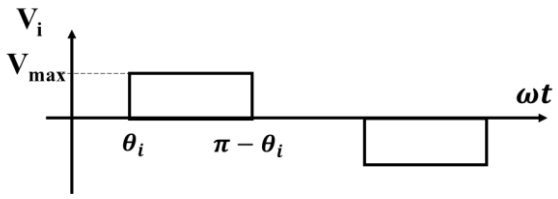



Figure 6. Illustration of the partial waveform Vi

To eliminate a specific harmonic $V_n$, it is sufficient to set $Bn = 0$. Finally, the system of equations used in the SHE technique is solved using MATLAB's fsolve function. The initial guess vector for fsolve is computed based on (13).

$$\theta_0^x = \frac{\pi}{2k} . \left(x - \frac{1}{2}\right) \quad where\ x = 1,2 \ldots k \ \ and\ k\ the\ number\ of\ switching\ angles \quad (13)$$

a. Symmetrical MLI five levels: In the five-level wave form shown in Figure 2, we have two switching angles (14), which means two harmonics to eliminate n=3 and n=5 (3[rd] and 5[th] harmonic).

$$\begin{cases} \sum_{i=1}^{2} cos(3\theta_i) - cos\left(3(\pi - \theta_i)\right) = 0 \\ \sum_{i=1}^{2} cos(5\theta_i) - cos\left(5(\pi - \theta_i)\right) = 0 \end{cases} \Rightarrow \begin{cases} \theta_1 = 12.00° \\ \theta_2 = 48.00° \end{cases} \quad (14)$$

b. Asymmetrical MLI seven levels: The output voltage of the seven-level waveform shown in Figure 3 possessed three switching angles (15), which make it possible to eliminate three harmonics n=3, n=5, and n=7.

$$\begin{cases} \sum_{i=1}^{3} \cos(3\theta_i) - \cos\left(3(\pi - \theta_i)\right) = 0 \\ \sum_{i=1}^{3} \cos(5\theta_i) - \cos\left(5(\pi - \theta_i)\right) = 0 \\ \sum_{i=1}^{3} \cos(7\theta_i) - \cos\left(7(\pi - \theta_i)\right) = 0 \end{cases} \Rightarrow \begin{cases} \theta_1 = 11.67° \\ \theta_2 = 26.93° \\ \theta_3 = 56.05° \end{cases} \quad (15)$$

c. Asymmetrical MLI nine levels: The number of switching angles in the nine-level waveform in Figure 4 is four, as indicated by (16), which allows to elimination of four harmonics, n = 3, n = 5, n = 7, and n = 9.

$$\begin{cases} \sum_{i=1}^{4}\cos(3\theta_i) - \cos\big(3(\pi-\theta_i)\big) = 0 \\ \sum_{i=1}^{4}\cos(5\theta_i) - \cos\big(5(\pi-\theta_i)\big) = 0 \\ \sum_{i=1}^{4}\cos(7\theta_i) - \cos\big(7(\pi-\theta_i)\big) = 0 \\ \sum_{i=1}^{4}\cos(9\theta_i) - \cos\big(9(\pi-\theta_i)\big) = 0 \end{cases} \Rightarrow \begin{cases} \theta_1 = 0.85° \\ \theta_2 = 24.85° \\ \theta_3 = 35.14° \\ \theta_4 = 60.85° \end{cases} \quad (16)$$

## 3. SIMULATION

The PSIM simulation was conducted using the schematic diagram presented in Figure 7. Figure 7 depicts the configuration of the MLI, which consists of two full bridges connected in series, with four switches each. The output voltage is the sum of the full bridge outputs, and the number of levels can be varied from 5 to 9 according to the switches control and the DC input value, as explained earlier in this article.

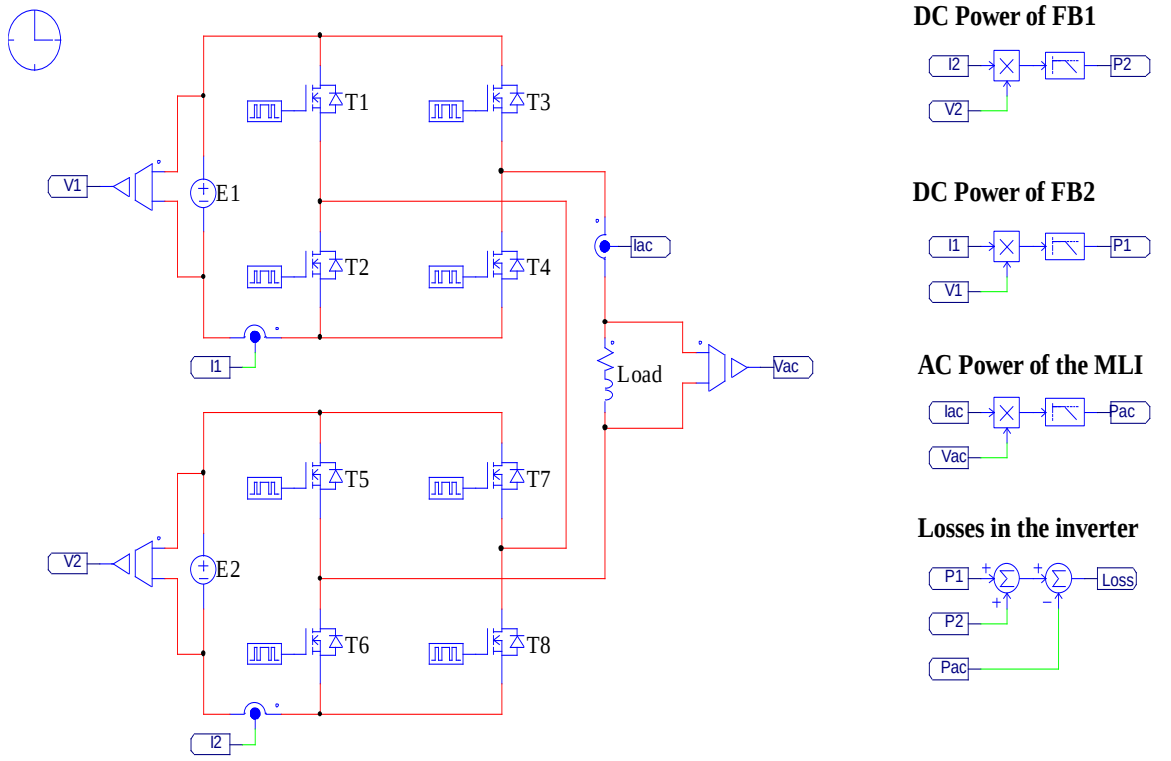


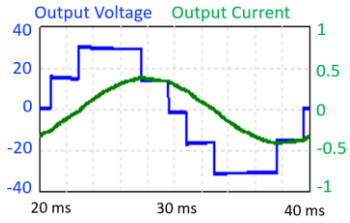
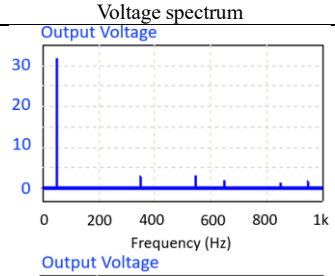
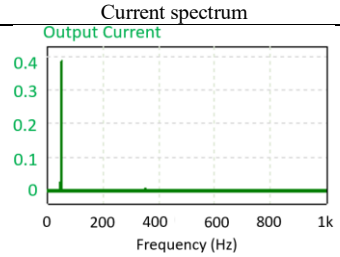
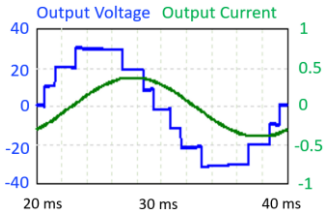
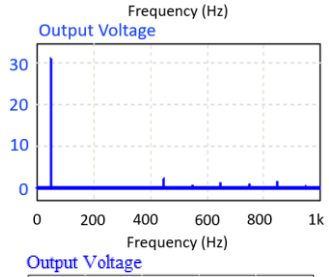
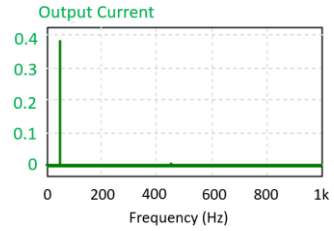
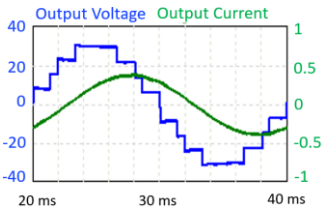
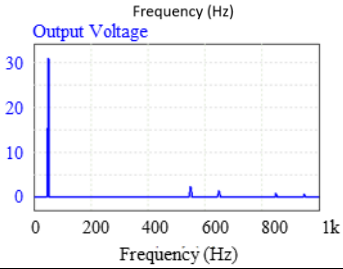
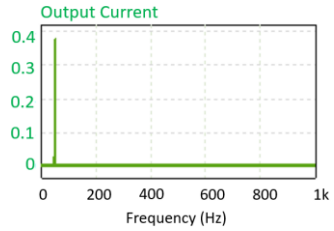

Figure 7. Schematic diagram of the PSIM environment

The inverter is connected to an RL circuit (R = 51.4 Ω and L = 200 mH) that acts as a low-pass filter to remove high-frequency components from the inverter's output voltage. In order to measure the power absorbed by each full bridge in the inverter, it is necessary to measure the input current and voltage. By multiplying these instantaneous values, the instantaneous power can be obtained. This product is then filtered using a low-pass filter to obtain the average value, which represents the real power consumed by the full bridge. The same procedure is applied to measure the power consumed by the load.

By performing these measurements, it becomes possible to determine the losses in the inverter. This is achieved by subtracting the power at the input of the inverter, which is the sum of the power at the input of each full bridge, from the power at the output of the inverter, which represents the power absorbed by the load. This subtraction allows for the calculation of the losses incurred within the inverter system.

Table 1 shows the output voltage, spectrum analysis of the output voltage, and the current waveform of each case. The spectrum analysis of the output voltage confirms the effectiveness of the Selective Harmonic Elimination (SHE) technique in eliminating specific harmonics. As the number of levels in the inverter increases, more harmonics can be effectively eliminated.

Table 1. Simulation waveforms and spectrum analysis of the inverter output voltage and current were performed on the PSIM environment

| Level | Waveforme | Voltage spectrum | Current spectrum |
|---|---|---|---|
| 5L |  |  |  |
| 7L |  |  |  |
| 9L |  |  |  |



## 4. EXPERIMENTAL VALIDATION

To practically validate the simulation results presented in the previous section, a test bench setup (Figure 8) was used. This experimental setup consists primarily of measurement instruments—including a voltmeter, ammeter, and power quality analyser—as well as the inverter with its drivers and isolation interface feeding an RL load.

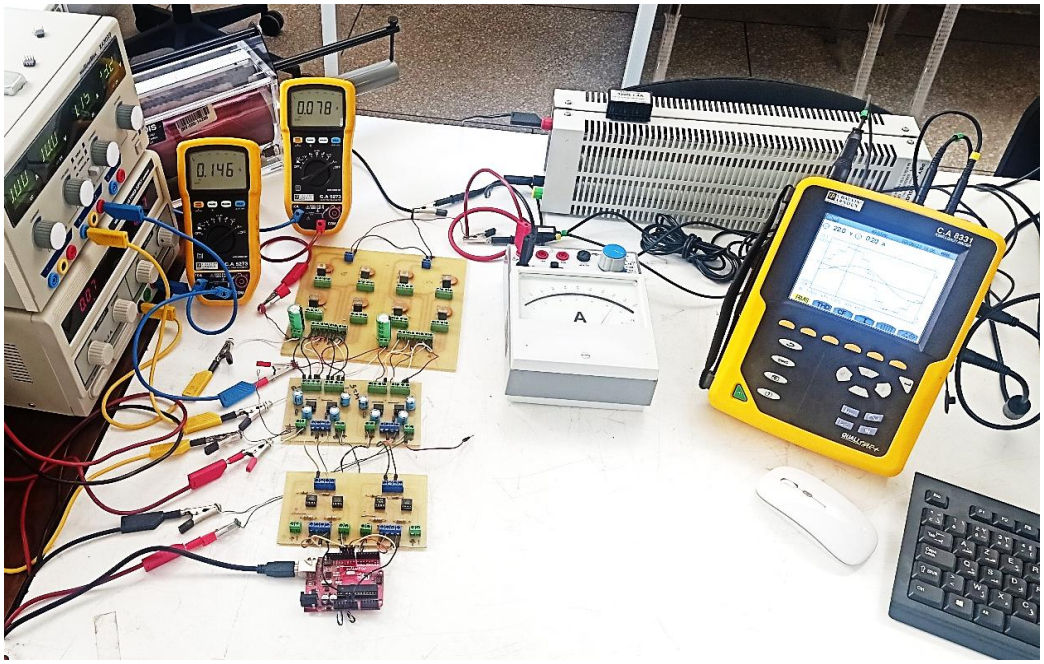


Figure 8. Experimental bench

To compare the inverter's performance between simulation and experimental testing, and due to the limited precision of the power quality analyzer, it was necessary to calculate the power on both sides of the inverter using the measured parameters and then deduce the power losses. Additionally, the apparent power was calculated to enable comparison between the power factor and the cosine of the phase angle of the load (cos φ), which provides insight into the impact of harmonic distortion.

Figure 9 presents a simplified schematic diagram of the test bench to aid understanding. The system consists of several key components (Figures 8 and 9):

- Command circuit: An Arduino UNO generates command signals that control the operation of the inverter.
- Optocoupler: It serves as a means to separate the command circuit from the power circuit. It ensures electrical isolation and protection between the two circuits.
- Drivers: These components are responsible for applying the required voltage between the gate and the source of the transistors in the inverter.
- Full bridges: These bridge circuits generate the corresponding voltage output based on the commands received from the command circuit. They convert the DC input into the desired AC output voltage

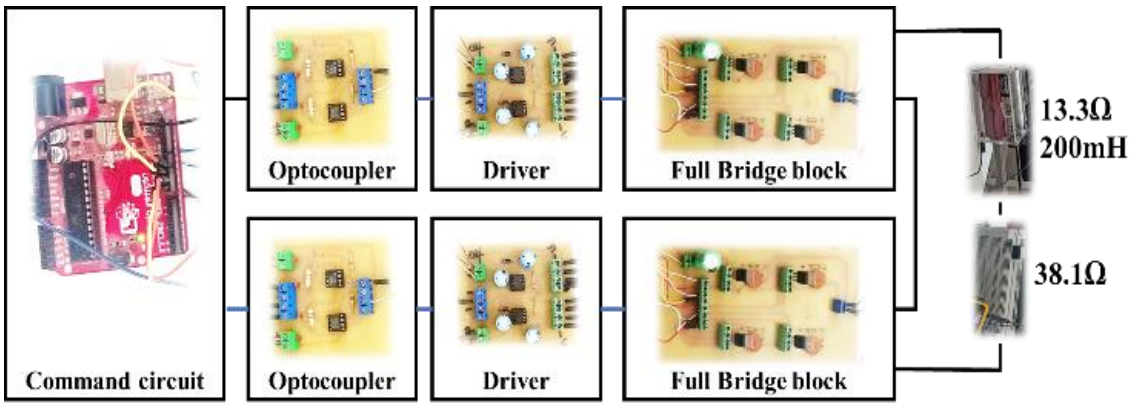



Figure 9. Schematic block of experimental setup

The experimental validation involved measuring various parameters to compare the simulation results with practical results. The following measurements were taken:

- Average voltage (E1, E2) and current ($I_{DC1}$, $I_{DC2}$) at the input of each full bridge.
- $I_{RMS}$ the current RMS value measured at the load (RL circuit).
- $V_{RMS}$ voltage RMS value, as well as voltage Total Harmonic Distortion (THD) and current THD, measured at the output of the inverter using a power quality analyzer.

In addition to these measurements, other parameters were calculated using the following formulas:

- DC power at the input of the inverter is calculated in (17).

$$P_{DC} = E1.I_{DC1} + E2.I_{DC2} \quad (17)$$

- AC power at the output of the inverter is determined by using (18).

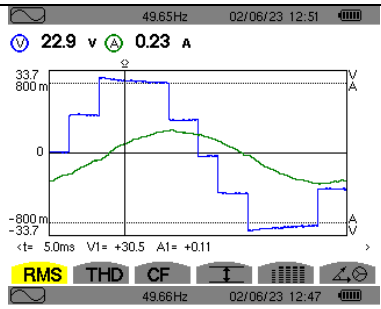
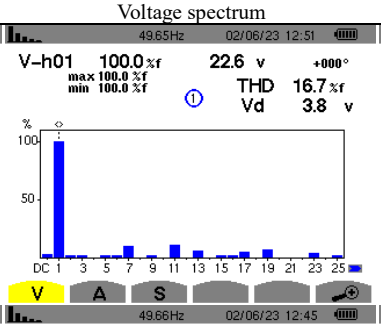
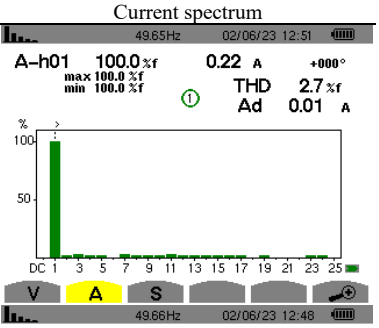
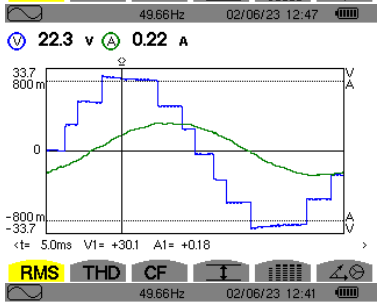
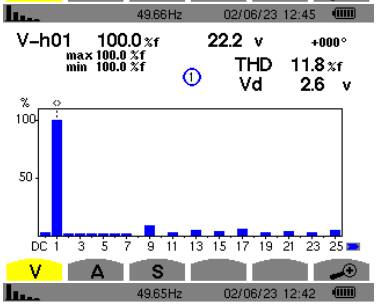
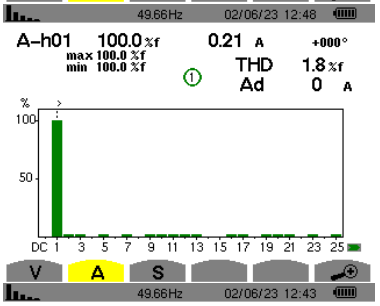
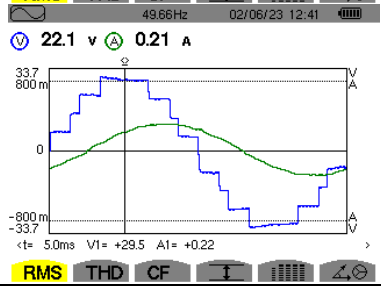
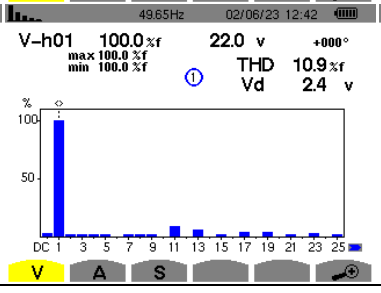
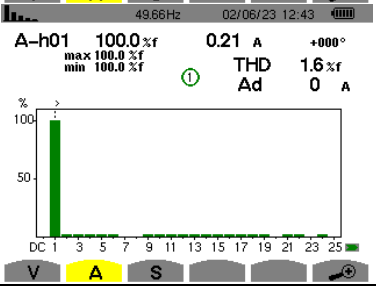
$$P_{AC} = R.I_{RMS}^2 \quad (18)$$

- Losses in the inverter are deduced by the subtraction of (17) and (18) as indicated in (19).

$$Losses = P_{DC} - P_{AC} \quad (19)$$

By measuring and calculating these parameters, a comprehensive understanding of the inverter's performance and efficiency can be obtained, allowing for a comparison between simulation and practical results. Table 2 provides a spectrum analysis and waveform representation for both current and voltage at the output of the inverter, corresponding to different numbers of levels.

Table 2. Practical waveforms and spectrum analysis using power quality analyser C.A 8331

| Level | Waveform | Voltage spectrum | Current spectrum |
|---|---|---|---|
| 5L |  |  |  |
| 7L |  |  |  |
| 9L |  |  |  |

## 5. RESULTS

Simulation and practical results are presented in Table 3. Based on the analysis of Table 3, it is evident that the difference between the results obtained at 7 and 9 levels is relatively small compared to the differences observed between 5 and 7 levels or 5 and 9 levels. This finding reinforces the fact that the elimination of low-order harmonics significantly improves the performance of the inverter. The presence of low-order harmonics, which tend to have significant magnitudes, can adversely impact the quality of the inverter.

Table 3. Simulation and practical results

| Measured and calculated parameters | | Simulation | | | Practical | | |
|---|---|---|---|---|---|---|---|
| | | Sym 5L | Asy. 7L | Asy. 9L | Sym 5L | Asy. 7L | Asy. 9L |
| RMS | Voltage (V) | 22.730 | 22.180 | 21.990 | 22.900 | 22.300 | 22.100 |
| | Current (A) | 0.276 | 0.272 | 0.270 | 0.279 | 0.273 | 0.271 |
| Spectrum analysis | V Fundamental RMS value (V) | 22.373 | 22.076 | 21.899 | 22.600 | 22.200 | 22.000 |
| | THD % | 17.940 | 12.860 | 11.930 | 16.700 | 11.800 | 10.900 |
| | I Fundamental RMS value (A) | 0.276 | 0.272 | 0.269 | 0.270 | 0.270 | 0.260 |
| | THD % | 2.130 | 1.210 | 1.070 | 2.700 | 1.800 | 1.600 |
| Power analysis | $P_{DC}$ (W) | 4.205 | 4.066 | 4.003 | 4.247 | 4.073 | 4.010 |
| | $P_{AC}$ (W) | 3.944 | 3.810 | 3.754 | 4.001 | 3.831 | 3.775 |
| | Apparent power (VA) | 6.273 | 6.033 | 5.937 | 6.389 | 6.088 | 5.989 |
| | Power factor | 0.629 | 0.632 | 0.632 | 0.626 | 0.629 | 0.630 |
| | Losses (W) | 0.261 | 0.256 | 0.249 | 0.246 | 0.242 | 0.235 |
| | Efficiency (%) | 93.793 | 93.704 | 93.780 | 94.208 | 94.060 | 94.134 |

The interpretation of Figure 10 shows a clear correlation between the number of levels and the THD factor. As the number of levels increases, there is a significant reduction in the THD factor. This observation is particularly evident in the transition from 5 levels to 7 levels, where there is a substantial decrease in the THD factor. This reinforces the notion that increasing the number of levels in the inverter leads to a more sinusoidal output waveform with reduced harmonic content, resulting in a lower THD factor.

By analysing Figure 11, it is evident that as the number of levels increases in the inverter, the RMS value of the output voltage and its fundamental component progressively converge and become closer to each other. The analysis of Figure 12 shows that the 5-level voltage configuration allows for a higher power transfer compared to the 7-level and 9-level configurations. This observation can be attributed to Figure 13, which demonstrates that an increase in the RMS value of the fundamental component corresponds to an increase in AC power.

It is evident in Figure 14 that the reduction in losses from 5 levels to 7 levels is smaller compared to the reduction in losses from 7 levels to 9 levels. At the AC side, as the number of levels in the inverter increases, the apparent power decreases (Figure 15). This is primarily due to the harmonics eliminated using the SHE technique, which reduces the distortion power, leading to an improvement in the power factor. From Table 3, it can be observed that the power factor approaches the value of cos(φ)=0.633, where φ represents the angle of the load defined as $\varphi = \arctan\left(\frac{2.\pi.f.L}{R}\right)$.

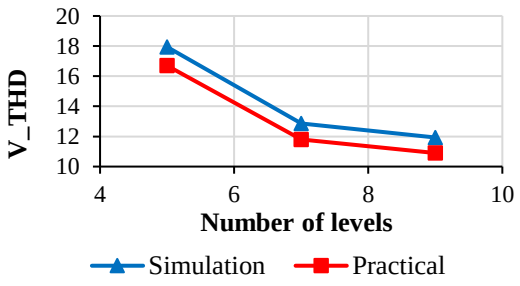



Figure 10. Variation of total harmonic distortion of inverter output voltage with number of levels

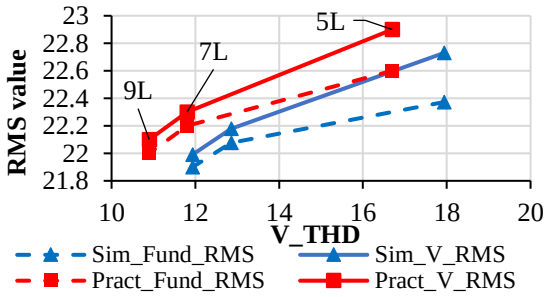



Figure 11. Comparison of simulated and practical RMS values of the output voltage and its fundamental

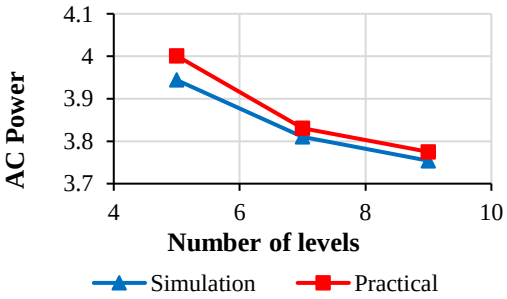



Figure 12. Evolution of the power at the AC side as a function of the number of levels

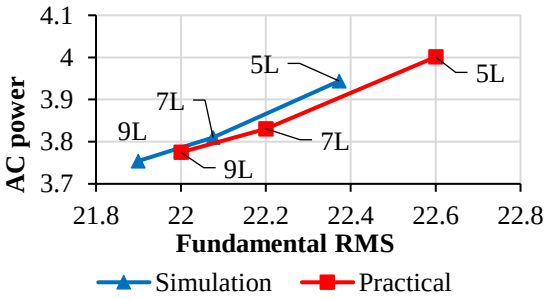



Figure 13. Evolution of the power at the AC side as a function of the fundamental RMS value

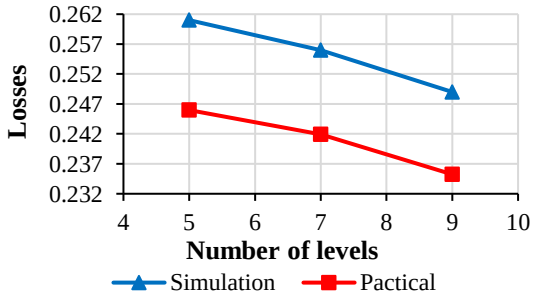



Figure 14. Evolution of the losses in the inverter with the number of levels

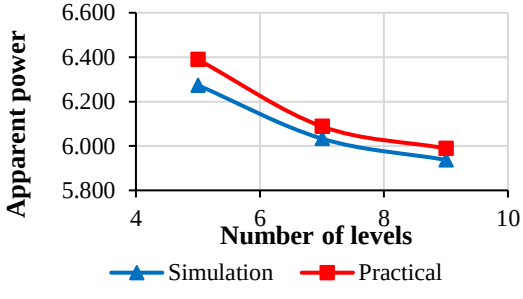



Figure 15. Evolution of the apparent power at the AC side as a function of the number of levels

Generally, the practical results validate the simulation results. It is evident that all the practical curves closely align with their corresponding simulation curves and exhibit similar trends. However, slight differences between the two can be attributed to factors such as temperature effects, the accuracy of the simulation model in representing the physical system, and measurement errors.

## 6. CONCLUSION

In conclusion, the use of MLIs has gained significant popularity in the field of power electronics due to their ability to improve the quality of the output voltage. Asymmetrical MLIs, in particular, offer a higher number of levels compared to symmetrical MLIs, resulting in more sinusoidal voltage waveforms with a low number of switches. Through simulations conducted using the PSIM software and experimental validation, it was demonstrated that increasing the number of levels in the MLI and implementing the SHE technique can effectively reduce the THD factor and losses in the inverter. This leads to improvements in the power factor and overall efficiency of the inverter system. Furthermore, it was observed that as the number of levels in the MLI increases, the magnitude of the fundamental component of the output voltage decreases. This implies that the contribution of the fundamental component to real power production diminishes as more levels are added. Looking ahead, I am eager to explore the application of the asymmetrical configuration for injecting power from photovoltaic (PV) panels. This approach could enhance efficiency and integration of renewable energy sources into the system. Future work will focus on optimizing this setup for real-world PV power delivery.

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## AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

| Name of Author | C | M | So | Va | Fo | I | R | D | O | E | Vi | Su | P | Fu |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Nabil Saidani | ✓ | ✓ | ✓ | ✓ | ✓ | | ✓ | ✓ | ✓ | | | | | |
| Rachid El Bachtiri | ✓ | ✓ | | ✓ | ✓ | ✓ | | ✓ | | ✓ | | | | |
| Abdelaziz Fri | ✓ | | ✓ | ✓ | | ✓ | ✓ | | | ✓ | | | | |
| Karima El Hammoumi | ✓ | | ✓ | ✓ | | | ✓ | | | ✓ | | | | |

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

## CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

## DATA AVAILABILITY

The authors confirm that the data supporting the findings of this study are available within the article.

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## BIOGRAPHIES OF AUTHORS

**Nabil Saidani** was born in Kenitra, Morocco in January 1989, obtained his engineering diploma in Electronics, Electrotechnics and Automatics from the Faculty of Science and Technology of Tangier in 2014. Afterwards, he was able to pass his agrégation in electrical engineering in 2019, allowing him to teach specialized physics in electronics and industrial computing at the BTS centre of Fez. His research area is the advanced control of multilevel inverter to inject photovoltaic power into the grid. He can be contacted at email: nabil.saidani@usmba.ac.ma.

**Rachid El Bachtiri** was born in Midelt, Morocco in November 1964. He received the Electrical engineering diploma from the École Mohammadia d'Ingénieurs, Rabat, Morocco in July 1988, and the Doctorate on applied sciences from the Université Catholique de Louvain, Louvain-la-Neuve, Belgium in January 1997. He is a professor at the higher school of technology, USMBA University, Morocco. Currently, he is a responsible of a group of scientific researchers "Equipe de Recherche en Electrotechnique, Electronique de Puissance et Energies Renouvelables", and Head of electrical engineering and intelligent systems department. His research interests are motor drives, power electronic converters, automatic control systems and renewable energy. Pr. El Bachtiri is expert at CNRST (National Center for Scientific and Technical Research), Rabat, Morocco. He can be contacted at email: rachid.elbachtiri@usmba.ac.ma.

**Abdelaziz Fri** was born in Fez, Morocco. After graduating from the École Normale Supérieure de l'Enseignement Technique (ENSET) in Rabat, Morocco, in 1998, he began his career as a teacher in engineering sciences. He later pursued a Master's degree in Engineering of Industrial Automated Systems from the Faculty of Sciences at Sidi Mohamed Ben Abdellah University in Fez, Morocco. In 2017, Abdelaziz completed his Ph.D. in Renewable Energies and Static Converters. The following year, in 2018, he joined the Higher School of Technology at USMBA University in Fez as an assistant professor. Currently, he is an associate member of the Technologies and Industrial Services Laboratory, and a member of the Research Team in Electrical Engineering, Power Electronics, and Renewable Energies (Équipe de Recherche en Électrotechnique, Électronique de Puissance et Énergies Renouvelables). His research interests include renewable energies and the control of electrical systems. He can be contacted at email: Abdelaziz.fri@usmba.ac.ma.

**Karima El Hammoumi** received the State Engineer diploma in Automatic Control and Industrial Computing in 1985 and the DESA in 'Industrial Process Control' in 2001 from the Mohammadia School of Engineers, Rabat, Morocco. She obtained the Doctorate degree in Renewable Energies from the University sidi Mohamed Ben Abdellah Fez, Morocco in July 2021. Professor EL HAMMOUMI is currently a Professor at the Higher School of Technology, Université Sidi Mohamed Ben Abdellah, Fez, Morocco. His research interests automatic control systems, renewable energy, smart grid and battery storage. She can be contacted at email: karima.elhammoumi@usmba.ac.ma