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THD and spectral performance analysis of two-triangle RPWM for inverter applications

G. Jegadeeswari[1], R. Sundar[2], S. P. Manikandan[3], E. Poovannan[4], C. Rajarajachozhan[5], M. Batumalay[6], Sukumar Kalpana[7]
[1]Department of Electrical and Electronics Engineering, Saveetha Engineering College, Chennai, India
[2]Department of Marine Engineering, AMET Deemed to be University, Chennai, India
[3]Electronics and Communication Engineering, Saveetha Engineering College, Chennai, India
[4]Computer Science Engineering, Saveetha Engineering College, Chennai, India
[5]Electronics and Communication Engineering, University College of Engineering, Kancheepuram, India
[6]Centre for Data Science and Sustainable Technologies & Faculty of Data Science and Information Technology, INTI International University, Nilai, Malaysia
[7]Department of Physics, Saveetha Engineering College, Chennai, India

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ABSTRACT

Pulse width modulation (PWM) is essential for voltage source inverters (VSI) to generate high-quality voltage outputs. Conventional deterministic PWM generates predictable harmonics, causing clusters that increase acoustic noise. Random PWM (RPWM) disperses harmonic power over a wider frequency range, reducing noise and electromagnetic interference. Many RPWM techniques improve inverter quality, but only partially suppress dominant harmonics and lack effective harmonic spreading. Most studies focus on simulations with limited FPGA implementation or hardware validation. The use of digital tools like VHDL, ModelSim, and MATLAB co-simulation remains underutilized. This paper proposes two-triangle RPWM strategies to enhance harmonic dispersion and reduce total harmonic distortion (THD). Co-simulation results are shown for both SPWM and RPWM, along with comparisons of fundamental voltages, THD, and HSF across different modulation indexes. Additionally, synthesis data for the Xilinx XC3S500E FPGA processor is supplied. The last section offers a comparative analysis and experimental validation of SPWM and RPWM. These techniques enable enhanced inverter performance, lower acoustic noise, and process innovations in power electronic systems.

Corresponding Author:

G. Jegadeeswari
Department of Electrical and Electronics Engineering, Saveetha Engineering College
Chennai, India
Email: jegadeeswari.dharan@gmail.com

1. INTRODUCTION

The two main kinds of inverters are current source inverters and voltage source inverters. Out of which voltage source inverters (VSI) is one of the most used circuits among contemporary power electronics converters with power ratings ranging from kilowatts to many megawatts. By converting a constant DC voltage level into a 3ϕ AC voltage, a VSI allows for frequency and magnitude modifications [1]. A typical layout of a field-programmable gate array (FPGA) based 3ϕ voltage source inverter is shown in Figure 1. PWM-VSIs are utilized in a variety of applications, such as static VAR compensators, regenerative drive applications, and applications involving uninterruptible power supplies [2]. In all the applications, the power

flow is controlled by switching of the devices, i.e., by having proper pulse width modulation (PWM) for the devices used in the inverters. The present work concentrates on the PWM-based drive applications.

An inverter's function is to convert a DC source into an AC voltage with a frequency and amplitude that may be adjusted. PWM techniques have gained prominence in recent decades and are the primary means of obtaining the VSI's quality-controllable outputs [3], [4]. For a variety of applications, numerous PWM schemes have been created and successfully applied.

Many PWM techniques have different goals and guiding principles, but both have been accomplished and used [5]. The sinusoidal PWM (SPWM) method is the backbone of the PWM field [6]. It generates the PWM signal by comparing a high-frequency (easily filtered) carrier waveform with an output (fundamental) frequency sinusoidal waveform [7].

Furthermore, the SVPWM is a digital method that pre-calculates the switching timings and instants for different target output sections. It offers choices for where to place the active vectors within each sampling interval [8], [9]. Additionally, there are a few other popular PWM schemes that are worth considering, such as amplitude modulated triangular carrier PWM [10], selective harmonic elimination PWM [11], discontinuous PWM [12], third harmonic injection PWM [13], and triplet harmonic injection PWM [14]. The output voltage's harmonic spectrum provides a clear understanding of the performance variations between them.

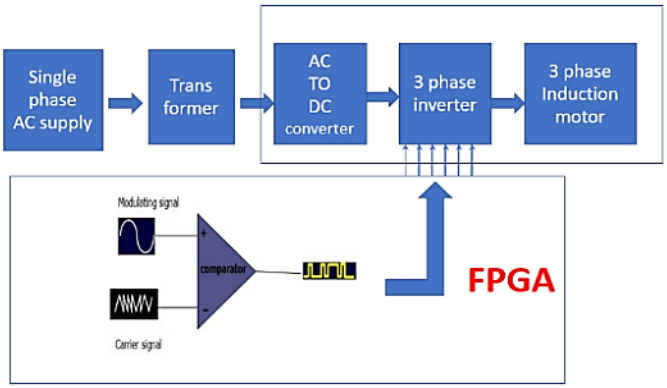


Figure 1. FPGA-based three-phase voltage source inverter

The harmonic profile acquired for a certain control structure and input results in a distinct classification even when PWM approaches are categorized using different scales [15]. Although an inductive load or filter can readily filter these high-frequency harmonics, their presence contributes to acoustic noise and electromagnetic interference (EMI) [16]. The current study was conducted on non-deterministic PWM, also called random pulse width modulation, which is the second class of PWM [17].

Acoustic noise and vibration are two of the main issues with modern drives. Therefore, the PWM methods employed in inverters and the motor's structural design are the main reasons for acoustic noise issues. According to Rodriguez *et al.* [18], PWM inverters with predictable switching frequencies cause mechanical vibrations in the motor, which produce an unpleasant auditory switching noise. In RPWM, there are more harmonics with no distinct harmonics and an undesirable magnitude rather than a small number of dominantly sized harmonics.

Even while the SPWM and SVPWM patterns meet the primary requirements of the motor and theoretically work with recent speed control techniques, it is not desired for harmonics to cluster around a specific frequency [19]. Since 1987, RPWM techniques have drawn users as a way to address the aforementioned issue [20]. The duty cycle of a typical RPWM is determined by comparing the random two-triangular waves with a reference sinusoidal wave with opposing phases but the same fixed frequency [21].

Microprocessor-based PWM schemes have been prevalent in recent years, and they can be tuned to minimize motor torque and/or harmonics in driving applications [22]. Field programmable gate arrays have gained popularity since their introduction in 1984, and now, this is the most popular technique in the digital circuit world [23], [24]. The secret to FPGA success is the programmability, which allows any circuit to be built quickly by suitably programming an FPGA [25].

Although various RPWM techniques exist to reduce acoustic noise and improve inverter output quality, they often only partially suppress dominant harmonics and lack effective harmonic dispersion. Most prior work focuses on simulations, with limited practical FPGA implementation or hardware validation. The

integration of digital tools like VHDL, ModelSim, and MATLAB co-simulation remains underexplored. This study addresses these gaps by developing efficient digital RPWM schemes to enhance harmonic distribution and inverter performance in VSI-fed induction motor drives.

The following are this paper's primary goals:

- To analyze different RPWM randomization levels in terms of harmonic magnitudes and harmonic spread factor (HSF).
- To confirm the FPGA performance using the Xilinx Project Navigator tool, and to confirm the functionality using the ModelSimSE 6.3f digital simulator.
- Co-simulation approach, which combines Modelsim and MATLAB simulation, is used to confirm the inverter's operation.
- PWM performance is compared using the output voltage, THD, and HSF fundamental component values.
- The overall goal of this study is to determine a formulaic, sensible, digital implementation of RPWM schemes that are appropriate to VSI drives and to improve their performance.

2. METHOD

The developed co-simulation delivers a time-saving technique for addressing mixed simulations. This method deploys a synthesizer and two simulators. MATLAB/Simulink is used for 3ϕ inverter modeling, FFT-PowerGUI analysis tool, and interface tool, while ModelSim SE 6.3f is employed for digital design simulation. To verify the functionality, an RTL-based test bench is incorporated with ModelSim-VHDL-design. All VHDL modules use a 50 MHz system clock, and a system deactivation is achieved by an active-high reset. The workspace is the area where the data between the two simulators are exchanges. Figure 2 illustrates how HDL co-simulation serves as a powerful tool between the analysis environment and design. The feasibility of real-time implementation is evaluated using the Xilinx Project Navigator tool, which incorporates behavior and synthesis analysis. The ratio between the distorted current/voltage and its fundamental is known as THD, and it is estimated by:

$$\% \text{ THD} = (\sqrt{(V_2^2 + V_3^2 + ... + V_n^2)}) / V_1 * 100\%$$

where, V_1 = RMS value of the fundamental component;

V_2, V_3, $V_4 \ldots V_n$ = RMS values of the 2nd, 3rd, 4^{th} harmonic components

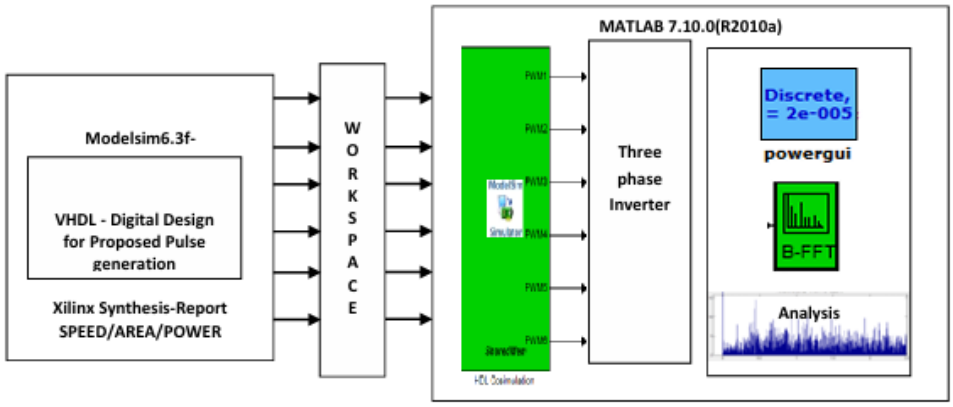
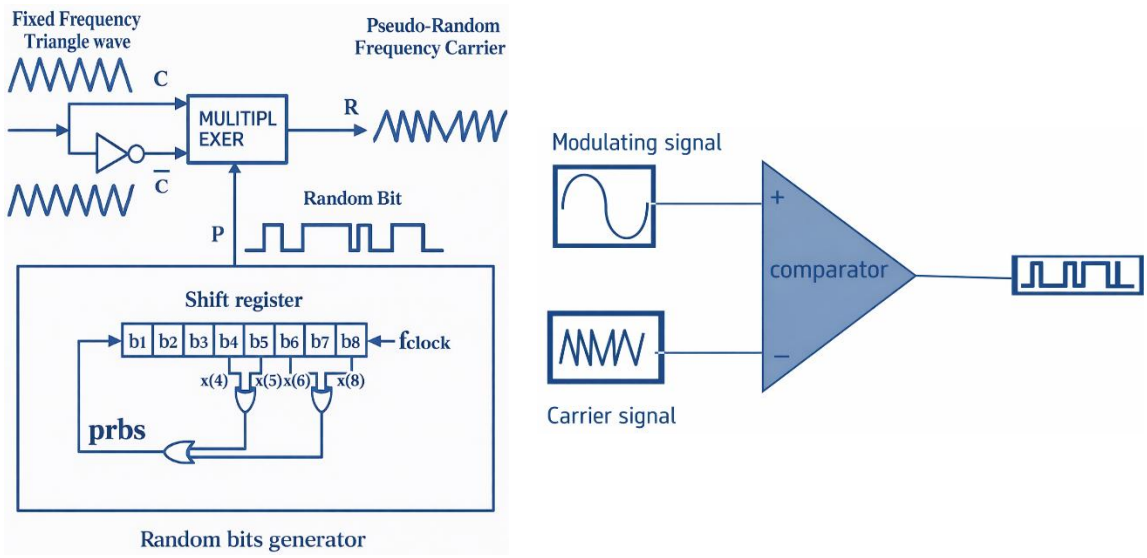


Figure 2. Co-simulation environment

2.1. Random pulse width modulation generation

By combining two triangular carrier signals of the same frequency, a random carrier signal is generated that is 180 degrees out of phase with each other. Figure 3(a) illustrates the process of generating the random pulse. These two carrier signals with fixed frequency and provides the multiplexer of 2:1. Figure 3(b) illustrates the comparator circuit of RPWM generation with a switching frequency of 3 kHz.



(a) (b)

Figure 3. RPWM: (a) generation of a random bit and (b) RPWM generation

3. DISCUSSION ON SIMULATION AND EXPERIMENTAL RESULTS

Figure 4 shows the MATLAB Simulink model of RPWM based three phase inverter design. The RPWM-based three-phase inverters are modeled using MATLAB 7.10.0 without the use of internal filters. Figures 5(a) and 5(b) show the Sine reference wave generation output at fm = 50 Hz and the output of random carrier generation at Fs = 3 kHz. In Figure 5(c). presents all switching pulses generation with the corresponding reference and carrier wave.

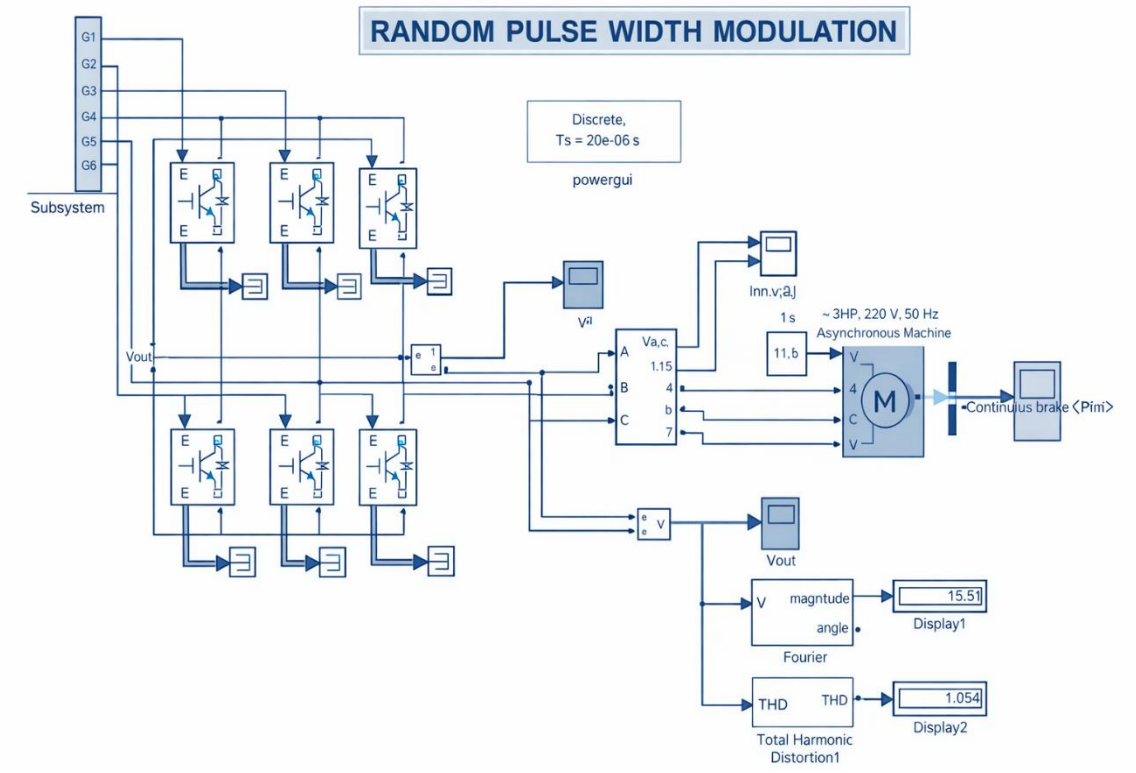


Figure 4. Simulink model of RPWM-based three-phase inverters

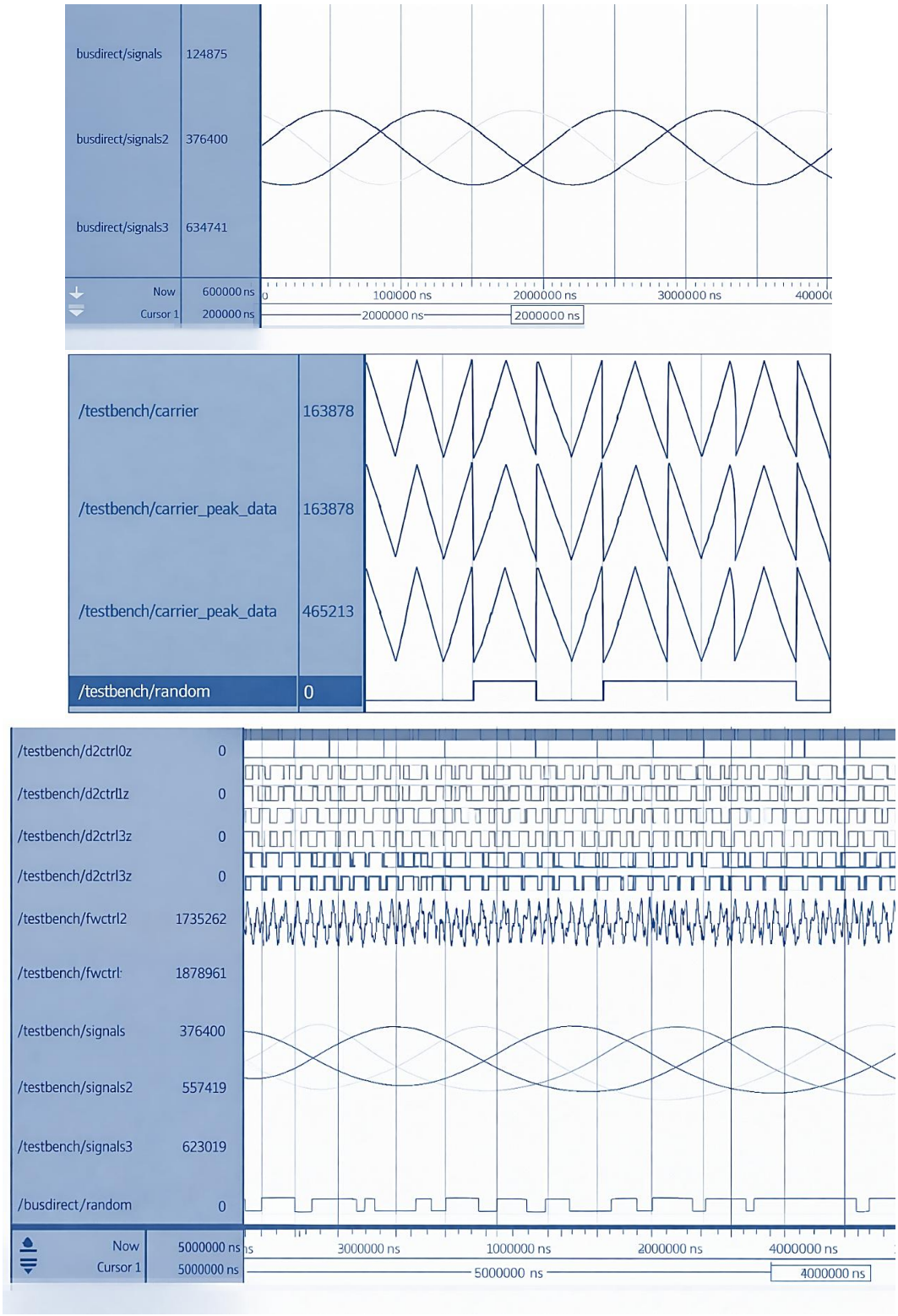


Figure 5. Generation of RPWM using ModelSim 6.3f: (a) generation of sinusoidal reference, (b) generation of a random carrier bit, and (c) generation of a random carrier bit

The simulation results show mean ± SD for THD of 125.95 % ± 73.17 % for SPWM and 127.14 % ± 71.19 % for RPWM. Figures 6(a)-6(d) show the THD analysis of both SPWM and RPWM for 1 and 1.2 m_a. The obtained THD values for the proposed inverter using simulation study of SPWM and RPWM

techniques in Table 1 were compared with values reported in previous literature. In this study, the minimum THD achieved was 58.24% for SPWM and 60.10% for RPWM at a modulation index of 1.2. Similar studies have reported THD values ranging between 60–75% for comparable operating conditions and switching frequencies [6]. The present work, therefore, demonstrates a notable improvement in harmonic performance, maintaining THD within the acceptable limits. Compared with conventional SPWM-based inverters, the proposed approach achieves a smoother harmonic spectrum and reduced low-order harmonic dominance. Overall, the results validate that the developed modulation strategy offers competitive or superior THD performance relative to published benchmark studies.

Table 1. Simulation results comparison

m_a	SPWM			RPWM		
	Output Voltage	%THD	HSF	Output voltage	%THD	HSF
0.2	38	254	10.7	39.8	250.1	9.23
0.4	77.20	161.9	6.56	79.3	164.2	5.18
0.6	113.6	121.8	4.94	116.7	125.1	4.37
0.8	152.5	90.8	3.64	158	92.13	3.1
1.0	190.4	68.99	2.94	196.8	71.23	2.12
1.2	210.3	58.24	2.34	217.5	60.10	1.82

The methods have been tested with the designed setup consisting of a FPGA based PWM inverter circuit. The arrangement includes a DSO, an FPGA board, an autotransformer, an inverter with driver circuits, and an induction motor. A Yokogawa Digital Storage oscilloscope was used for measuring all inverter outputs. The hardware implementation of FPGA-based speed control of an induction motor with three-phase VSI is shown in Figure 7, and the setup specification is listed in Table 2. A 220 V DC is fed into the inverter with the help of an autotransformer and a rectifier circuit. A dead time of 2.9 µs is given to each leg of the inverter for a smooth switching operation. For an inverter, a frequency of 50 Hz is set as a fundamental frequency for both conventional and proposed methods. The experimental results were analyzed over a modulation index of 0.2 to 1.2.

SPWM and two-triangle random pulse width modulation schemes are implemented by using FPGA-based three-phase inverters. The switching frequency of the fixed switching triangular frequency is about 3 kHz. The experimental measurement window of both SPWM and RPWM is depicted in Figures 8(a) and 8(b). The obtained THD values for the proposed inverter using experimental study of SPWM and RPWM techniques are shown in Table 3. In this study, the minimum THD achieved was 15.76 % for SPWM and 15.5% for RPWM at a modulation index of 1.2. Similar studies have reported THD values ranging between 40–50% for comparable operating conditions and switching frequencies [6]. The present work, therefore, demonstrates a notable improvement in harmonic performance, maintaining THD within the acceptable limits. Compared with conventional SPWM-based inverters, the proposed approach achieves a smoother harmonic spectrum and reduced low-order harmonic dominance. Figures 9(a)-9(c) display the harmonic spectra for SPWM and RPWM with the m_a varying from 0.2 to 1.2 with $m_f = 50$, which were acquired from the ModelSim digital environment using co-simulation approaches.

Table 2. System specification used in hardware setup

Type of inverter	Two-level inverter
Switch	IGBT
Source voltage	220 Volt
Load	3 Phase induction motor
M_a	0.8
Dead time	2.9 µs
Controller	Open loop
Filter usage	No

Table 3. Experimental results comparison

Ma	SPWM			RPWM		
	Output voltage	THD %	HSF	Output voltage	THD %	HSF
0.2	36.5	60.67	3.545	40.2	61	3.275
0.4	74.6	45.81	4.765	78.3	47	4.435
0.6	112.5	30.21	5.355	120.5	32	4.755
0.8	151.2	24.01	5.465	163.04	22	4.535
1.0	186.6	18.66	4.465	185	17.2	3.805
1.2	208.2	15.76	4.056	221.7	15.5	3.421

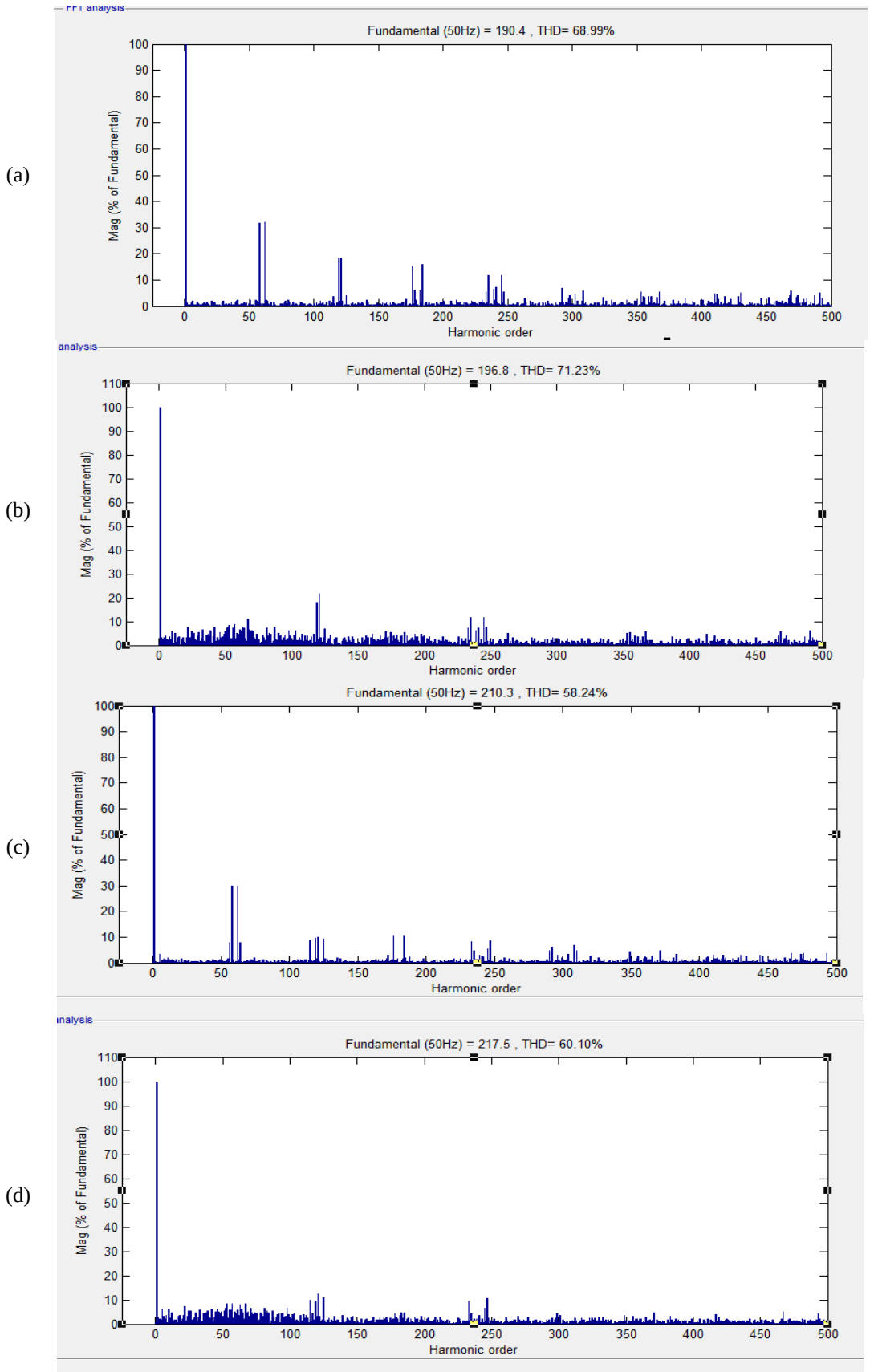


Figure 6. THD analysis: (a) SPWM for 1 m_a, (b) RPWM for 1 m_a, (c) SPWM for 1.2 m_a, and (d) RPWM for 1.2 m_a

Figure 7. Experimental setup

(a)

(b)

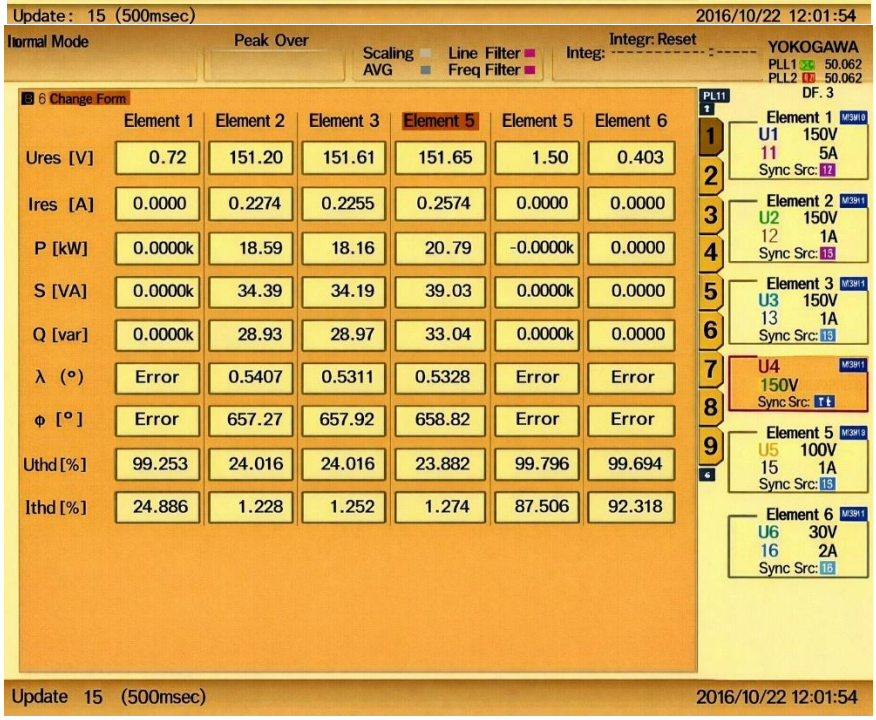


Figure 8. Measurement window for ma = 0.8: (a) SPWM and (b) RPWM

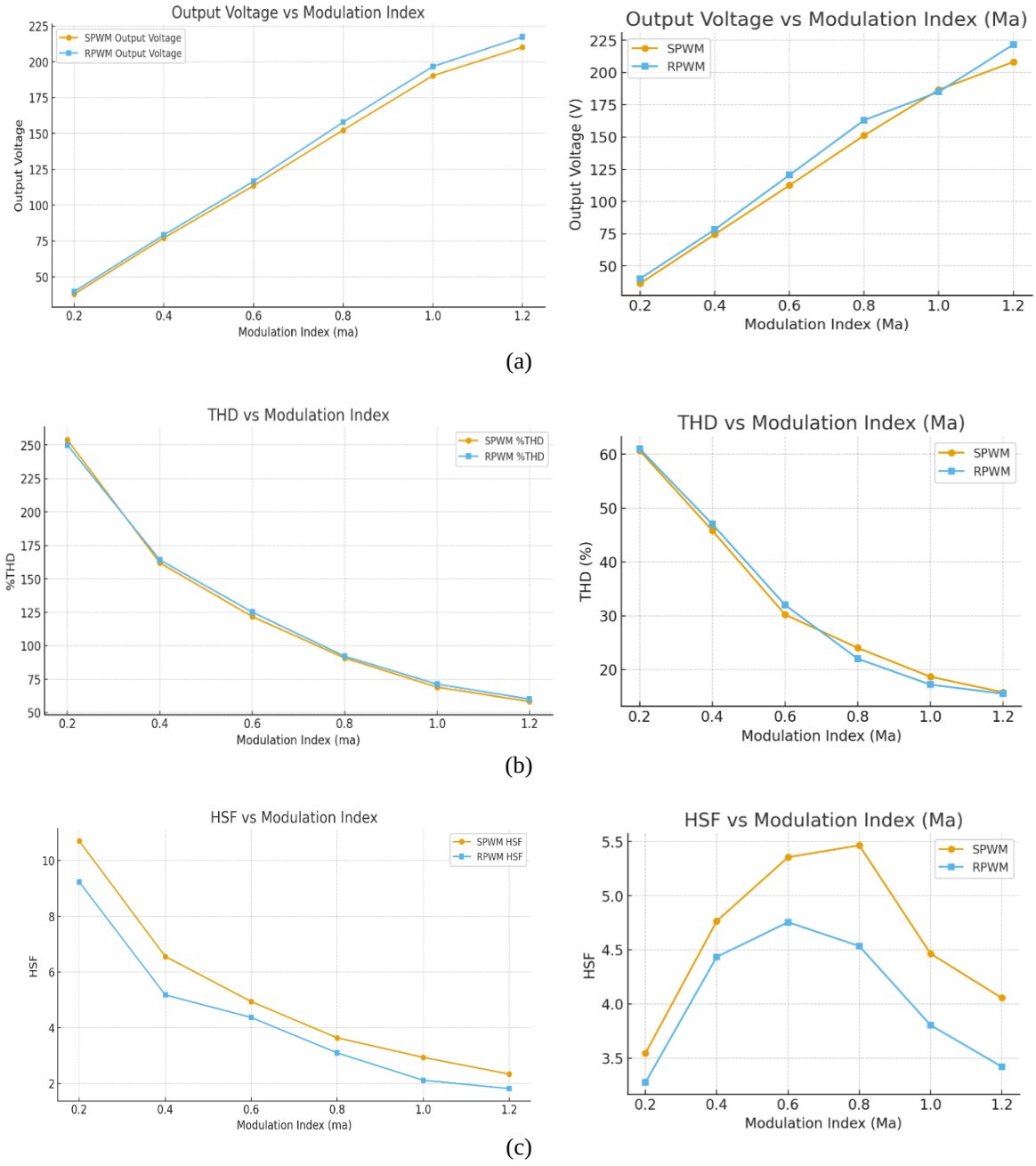


Figure 9. Harmonic spectra for SPWM and RPWM: (a) output voltage vs modulation index (ma), (b) total harmonic distortion (%THD) vs modulation index (ma), and (c) harmonic spread factor (HSF) vs modulation index (ma)

4. CONCLUSION

The usefulness of RPWM techniques in improving the three-phase VSIs' capacity to disperse harmonic power has been covered in this study. In contrast to conventional PWM techniques, which provide predictable harmonic shapes, RPWM exhibits unpredictability throughout the modulation process, resulting in a larger harmonic energy distribution. This feature addresses all the power quality concerns by notably reducing acoustic noise in the motor drive applications, which reduces the electromagnetic interference, too. The implementation of carrier-based RPWM methods on a digital platform based on an FPGA has shown to be practical and efficient. The proposed model of the RPWM method improves harmonic performance and increases its efficiency, but also increases its computational difficulty and usage of resources in the FPGA

when compared to traditional techniques. This may give us a challenge in employing the hardware setup at varying switching frequencies due to its constraints and time delay.

When compared to conventional PWM, the proposed RPWM model boosts its efficiency and improves the harmonic performance, but it also uses more resources on the FPGA and is more complex in computation. Because of its restrictions and delay time, this might make it tough for us to install the hardware at different switching frequencies. Future work should also focus on experimental validation in large-scale power applications to assess the long-term reliability and efficiency of the proposed RPWM strategies.

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AUTHOR CONTRIBUTIONS STATEMENT

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Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
G. Jegadeeswari	✓	✓	✓	✓	✓	✓		✓	✓	✓			✓	
R. Sundar		✓				✓		✓	✓		✓	✓		
S.P. Manikandan	✓		✓	✓	✓		✓			✓	✓		✓	
E. Poovannan	✓		✓		✓	✓		✓		✓			✓	
C. Rajarajachozhan	✓		✓	✓	✓		✓			✓	✓		✓	
M. Batumalay	✓	✓		✓	✓			✓	✓				✓	
Sukumar Kalpana	✓		✓	✓	✓			✓		✓			✓	

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors state no conflict of interest.

DATA AVAILABILITY

No new data were generated or analyzed in this study.

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BIOGRAPHIES OF AUTHORS

Dr. G. Jegadeeswari is an assistant professor in the Electrical and Electronics Engineering Department, Saveetha Engineering College (Autonomous), Chennai, since 2024. She received the B.Tech. degree in electrical and electronics engineering and the M.Tech. degree in power electronics and drives, both from Pondicherry University, in 2007 and 2012, respectively; and Ph.D. degree in Faculty of Electrical and Electronics Engineering from AMET University, Chennai, in 2024. With over 13 years of teaching experience and 6 years of research expertise, she has published more than 100 research articles, with 30 indexed in Scopus. She is a member of professional organizations such as IEEE and ISOR and holds 3 national and international patents. Additionally, she has authored 3 textbooks, 1 Editor Book, and contributed 8 book chapters to renowned publishers such as IGI Global, CRC Press, Bentham Science, and Wiley. She has organized over 70 workshops, faculty development programs (FDP), seminars, and conferences at both department and university levels. She has submitted research proposals to prestigious bodies like TNSCST, AICTE, DST, NCW, and SERB and secured an ATAL FDP grant of ₹2,70,000. Her contributions to academia have earned her several accolades, including best teacher and best paper awards from various institutions. She is also a reviewer and editorial board member for several international journals. Her research interests encompass power electronics and drives, special machines, and renewable energy. She can be contacted at email: jegadeeswari.dharan@gmail.com.

Dr. R. Sundar is currently working as an associate professor in marine engineering at AMET Deemed to be University. He received his Doctor of Philosophy (Ph.D.) in Engineering and Technology, specializing in renewable energy, from AMET University. He received a master's degree in power electronics and drives from SPIHER Electronics from the Madras Institute of Technology (MIT) Campus, Anna University. He received his Bachelor of Engineering degree in Electrical and Electronics Engineering from the University of Madras. He has 22 years of teaching experience, with areas of specialization including marine automation and control systems, marine electrical technology, electrical machines, renewable energy systems, IoT, and power electronics. He has published more than 25 papers in reputed journals, including Scopus, SCI-indexed journals, and Elsevier publications. He has presented 35 papers at various international conferences. He is also the author of the textbook Design of Electrical Machines, Control Systems, and Electric and Hybrid Vehicles. He has been a lifetime member of the Institute of Research Engineers and Doctors (IRED) and the International Association of Engineers (IAENG). He has been a member of the Academic Council, IQAC Core team, NDLI Club President, Marine Technology Society (MTS) Student Chapter Coordinator, and served on several committees, including the Library Committee. He can be contacted at email: mrsundarkrishna@gmail.com.

Dr. S. P. Manikandan holds a B.E. degree in Electronics and Communication Engineering from PSN College of Engineering & Technology, Affiliated Anna University. Following his undergraduate studies, he completed his M.E. in Embedded Systems and Technologies from Sri Ram Engineering College, Affiliated Anna University. He is Completed Ph.D. at Dr. M.G.R. Educational and Research Institute. Now he is working in Saveetha Engineering College, Thandalam, Chennai. He specializes in key subjects such as digital electronics, circuits and devices, and linear integrated circuits. With over 15 years of teaching experience, he has actively enhanced his academic knowledge through participation in various NPTEL and SWAYAM courses. He has made significant contributions to research and innovation, having published patents and books. He has also presented papers at numerous national and international conferences and published his research in reputed Scopus-indexed journals. He can be contacted at email: drmanikandansp@gmail.com.

Dr. E. Poovannan holds a Ph.D. in Electronics and Communication Engineering from SRM Institute of Science and Technology, Vadapalani Campus, Chennai, completed in March 2024. He has over 14 years of experience in academia and research. His area of specialization is VLSI Design, with a focus on low-power and high-speed digital systems. He began his academic career as a faculty member in SRM Institute of Science and Technology, Ramapuram Campus, Chennai, where he served as an assistant professor in the Department of Electronics and Communication Engineering from June 2010 to June 2020. Currently, he has been working as an assistant professor in the Department of ECE, Saveetha Engineering College (Autonomous), Chennai, since June 2024. He completed his M.Tech. in VLSI Design from Sathyabama University, Chennai, in 2010 and received his B.E. in Electronics and Communication Engineering from Thangavelu Engineering College, affiliated with Anna University, in 2005. He has actively participated in faculty development programs, workshops, and conferences, and has a keen interest in digital electronics, CMOS design, and low-power VLSI systems. He is proficient in using industry-standard tools such as Cadence, Xilinx, ModelSim, and MATLAB. He also holds certifications like CCNA and is committed to promoting excellence in engineering education and research. He can be contacted at email: epoovannan28@gmail.com.

Dr. C. Rajarajachozhan received the B.E. degree in electronics and communication engineering, M.E. degree in communication systems, and Ph.D. degree from Anna University, Chennai in the year of 2007, 2010, and 2020, respectively. Presently, he is working as an assistant professor in the Electronics and Communication Engineering Department at University College of Engineering, Kancheepuram.. His research interests include Semiconductor Device Modelling and technology. He can be contacted at email: chozhanacademic@gmail.com.

Dr. M. Batumalay earned her master's degree in engineering from the University of Malaya, Malaysia, and subsequently pursued her Ph.D. in photonics engineering at the same institution. Her research focuses on lasers, fiber optics, and fiber sensors. Previously, she invented fiber optics into sensors capable of detecting changes in relative humidity and chemical solutions. She collaborates with both local and international researchers to delve deeper into the behavior and characteristics of fiber optics sensors and plasmonic sensors, resulting in numerous high-quality publications in relevant journals. Additionally, she actively serves as a reviewer for several journals and holds a committee position in the Optical Society of Malaysia (OSM), where she contributes to activities involving young researchers. Furthermore, she is also registered as a professional engineer with the Board of Engineers Malaysia (BEM) and as a Chartered Engineer with The Institution of Engineering and Technology (IET). Presently associated with a prestigious private university in Malaysia, renowned for its expertise in communication, networking, and cloud computing, she holds pivotal leadership positions. As the director of the Center for Data Science and Sustainable Technologies, the Chair of the University Research Committee, and the Chief Internal Auditor for Malaysia Research Assessment, she epitomizes academic excellence. She is actively contributing as a managing editor for the Journal of Innovation and Technology (JOIT). Her fervent aspiration is to engage with emerging talents and prospective research candidates, thereby enhancing the academic landscape. She can be contacted at email: malathy.batumalay@newinti.edu.my.

Dr. Sukumar Kalpana is a professor in the Department of Physics with 24 years of teaching and 11 years of research experience. She has published 57 research papers and holds nearly 30 patents, of which 4 have been granted. With extensive expertise in teaching, research, and academic administration, she has actively organized multiple academic and professional events. Her commitment lies in leveraging her knowledge and experience to contribute to institutional growth while advancing her career in research and education. She can be contacted at email: kalpanarajan30@gmail.com.