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Design and DSP-based validation of a cascaded DSOGI-PLL for mitigating grid disturbances

Ilias En-Naoui, Abdelhadi Radouane, Azeddine Mouhsen, Hamid Yantour
Laboratory of Energy-Matter-Instrumentation and Telecoms (EMIT), Faculty of Sciences and Techniques, Hassan First University, Settat, Morocco

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ABSTRACT

Ensuring a smooth power injection into an electric grid in the presence of imperfections, such as phase disturbances, voltage imbalance, frequency variations, harmonics, and DC offsets, requires fast and robust phase-locked loop (PLL) techniques. Among these, the double second-order generalized integrator (DSOGI)-based PLL is widely used due to its strong performance in challenging grid conditions. However, conventional DSOGI-PLL has limitations in handling DC offsets and harmonic disturbances. To address these challenges, this paper introduces the design of a cascaded DSOGI-PLL that enhances attenuation of DC components and low-order harmonics while maintaining computational simplicity for DSP-based implementation. Experimental validation on a TMS320F28379D DSP platform demonstrates that the proposed scheme achieves synchronization settling within 48 ms even under severely polluted grid conditions, while reducing output unit-vector THD to 0.5% when the input voltage contains 22% THD. These results confirm the cascaded DSOGI-PLL as a significant improvement over conventional PLLs.

Corresponding Author:

Ilias En-Naoui
Laboratory of Energy-Matter-Instrumentation and Telecoms (EMIT)
Faculty of Sciences and Technology, Hassan First University
BP: 577, Route de Casablanca. Settat, Morocco
Email: i.ennaoui@uhp.ac.ma

1. INTRODUCTION

Power electronic converters play a critical role in the integration of renewable energy sources [1], and their effective control relies on robust synchronization algorithms with the grid as described in Figure 1. These algorithms must accurately estimate key grid voltage parameters, such as phase, amplitude, and frequency, to ensure grid stability and reliable power transfer. Among these algorithms, phase-locked loops (PLLs) serve as a fundamental component for achieving synchronization and implementing closed-loop control strategies in grid-connected power converters.

A wide range of three-phase PLLs has been reported in the literature. The conventional synchronous reference frame PLL (SRF-PLL) [2], [3] is simple and effective under balanced and clean grid conditions, but its performance degrades severely in the presence of voltage imbalance or harmonics. To mitigate these issues, enhanced schemes such as decoupled double synchronous reference frame PLL (DDSRF-PLL) [3], [4] have been developed, improving accuracy under imbalance. Other advanced PLLs for single-phase and three-phase systems [5]-[8] exist, but their high computational burden often limits their applicability on low-end digital controllers.

The double second-order generalized integrator PLL (DSOGI-PLL) [9], [10] has emerged as a promising alternative due to its ability to attenuate harmonics and handle voltage unbalance. It relies on two SOGI adaptive filters to generate orthogonal signals, which are then processed by an embedded SRF-PLL. However, despite its robustness, the DSOGI-PLL still faces challenges. First, the SOGI structure is not inherently designed to reject DC offsets, which may arise from grid asymmetries, control imperfections in renewable inverters, or measurement hardware such as transducers and ADCs [11]-[15]. The presence of such offsets leads to DC components in the PLL output unit vectors, violating grid interconnection standards like IEEE 1547-2018 [16], [17]. Second, DSOGI-PLL shows limited rejection capability against low-order harmonics, which are common in grids with nonlinear loads, photovoltaic inverters, or transformer saturation [18]-[20]. These harmonics distort the input voltage and degrade the phase and frequency estimation accuracy [21]. Table 1 summarizes the Strengths and points of weakness of each structure mentioned above against grid's disturbances.

These limitations highlight the need for improved synchronization schemes that remain accurate under DC offsets, low-order harmonics, and grid voltage imbalance. In this paper, we propose a cascaded DSOGI-PLL, a three-phase PLL structure designed to overcome the aforementioned issues while maintaining computational simplicity suitable for digital controllers in renewable energy converters. The proposed scheme cascades two DSOGI stages to enhance attenuation of low-order harmonics and DC components, thus ensuring accurate synchronization even under distorted or unbalanced grid conditions.

The novelty of this work lies in i) introducing a cascaded DSOGI architecture explicitly designed for DC offset and low-order harmonic rejection, ii) providing a complete discretization for real-time deployment, and iii) demonstrating an experimental validation on a DSP-based implementation using the TMS320F28379D platform. This approach is particularly relevant for grid-connected inverters in renewable energy systems, where fast and reliable synchronization under practical disturbances is essential.

This paper is organized as follows: The first section provides an analysis of the DSOGI structure to identify its weaknesses, followed by the design of the cascaded DSOGI-PLL and its discretization process to enable implementation on a digital processor. The second section discusses the experimental results, where the PLL is implemented on the TMS320F28379D DSP board, and its performance is validated under various real-world grid scenarios using a grid emulator developed in our laboratory. Finally, the last section provides a conclusion summarizing the key contributions of the work and potential future research directions.

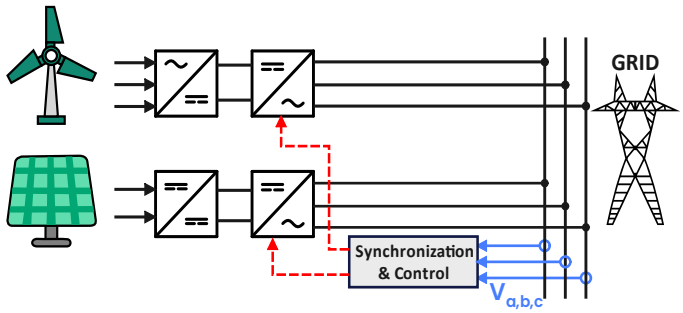


Figure 1. General architecture of the grid synchronization system for renewable energy converters

Table 1. Strengths and weaknesses of three-phase PLLs against grid's imperfections

PLL method	Balance	Imbalance	Frequency variation	High order harmonics	Low order harmonics	DC offset
SRF-PLL	✓	✖	✓	✖	✖	✖
DDSRF-PLL	✓	✓	✓	✖	✖	✖
DSOGI-PLL	✓	✓	✓	✓	✖	✖

2. METHODS

This section initially describes the limitations of the DSOGI-PLL under non-ideal grid conditions. Following this analysis, we present the design of a cascaded DSOGI-PLL to overcome these limitations.

2.1. Conventional DSOGI-PLL

The DSOGI-PLL illustrated in Figure 2, employs two SOGI quadrature signal generators (SOGI) to filter out voltage harmonics, a positive sequence calculator (PSC) to calculate positive's voltage sequence

during imbalance using (1) and (2), and a synchronous reference frame PLL (SRF-PLL) to estimate the grid frequency, phase angle, and the positive voltage sequence. The estimated frequency is then fed back to the DSOGI, ensuring frequency adaptability under varying grid conditions.

$$V_{\alpha}^{+} = \frac{1}{2} \cdot (V_{\alpha} - qV_{\beta}) \quad (1)$$

$$V_{\beta}^{+} = \frac{1}{2} \cdot (qV_{\alpha} + V_{\beta}) \quad (2)$$

The DSOGI-PLL converts the measured grid voltages through an ADC. Then, it transforms these voltages into the stationary reference frame using the Clarke transformation, resulting in the V_{α} and V_{β} components. Each of these signals is then processed by an SOGI block, which consists of a second-order generalized integrator, as illustrated in Figure 3(a). The SOGI bloc generates two outputs for each input signal: the direct component v and the quadrature component qv'. These outputs are related to the input through D(s) and Q(s) transfer functions, as defined in (3) and (4), respectively.

$$D(s) = \frac{v'}{v_{in}} = \frac{k.\omega_n.s}{s^2 + k.\omega_n.s + {\omega_n}^2} \quad (3)$$

$$Q(s) = \frac{qv'}{v_{in}} = \frac{k.{\omega_n}^2}{s^2 + k.\omega_n.s + {\omega_n}^2} \quad (4)$$

The bode diagrams in Figure 3(b) is plotted using ω_n=2π×50 and $k = \sqrt{2}$ which provides the minimum response time while ensuring an optimal overshoot of 4%. It is evident that at the frequency ω_n, the gain of both transfer functions is unity. From (3) and (4) and their bode plots, it is evident that these represent two second-order filters, where D(s) exhibits a band-pass filtering characteristic, while Q(s) is a low-pass filter. Both D(s) and Q(s) are effective in attenuating high-frequency harmonics; however, their filtering effect is less pronounced when dealing with low-order harmonics. Also, the two transfer functions exhibit a phase shift of 90° between them at the frequency ω_n, regardless of the value of k, which means that v' and qv' will be in quadrature, and v' is in phase with the signal v_{in} at this frequency. Additionally, an issue arises with Q(s) in the presence of a DC offset. From bode plots, Q(s) is incapable of eliminating the DC component, which will have a detrimental impact on the performance of the PLL [22], [23].

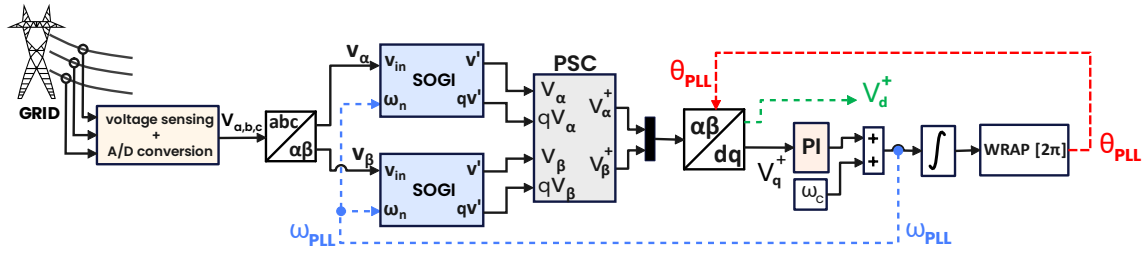
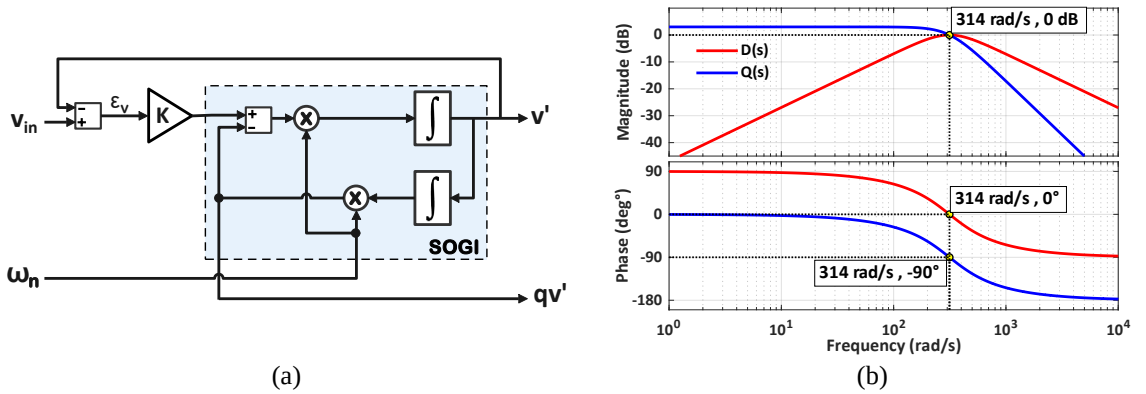


Figure 2. Architecture of a double second-order generalized integrator phase-locked loop



(a) (b)

Figure 3. SOGI model: (a) structure and (b) transfer functions bode plot

2.2. The three-phase cascaded DSOGI PLL

To deal with the problems discussed in the previous section, namely DC offset and low-order harmonics, a design of a cascaded SOGI is proposed. The two SOGI blocks shown in Figure 1 will be replaced with two CSOGI blocks, whose structure is provided in Figure 4. The CSOGI structure is formed by a cascade of two SOGI blocks.

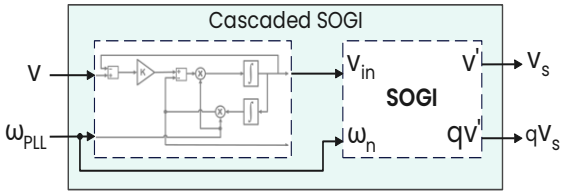


Figure 4. Architecture of a cascaded second-order generalized integrator

In this configuration, the signal v' from the first SOGI block is introduced as the new input for the second SOGI block, since it does not contain any DC component, while the signal qv' will not be considered by the second SOGI block because it allows the DC component to pass through. As a consequence, the second SOGI block processes only the filtered signal v', which is in phase with the original signal v at the frequency ω_{PLL}, as discussed in the previous section.

The second SOGI then performs an additional filtering step on v' and generates quadrature signals v_s and qv_s, both are unaffected by DC offset. The transfer functions $D_{CSOGI}(s)$ and $Q_{CSOGI}(s)$, which relate v_s and qv_s to the input v, are given by (5) and (6), respectively.

$$D_{CSOGI}(s)=\frac{v_s}{v}=\frac{(k.\omega_{PLL}.s)^2}{(s^2+k.\omega_{PLL}.s+{\omega_{PLL}}^2)^2} \quad (5)$$

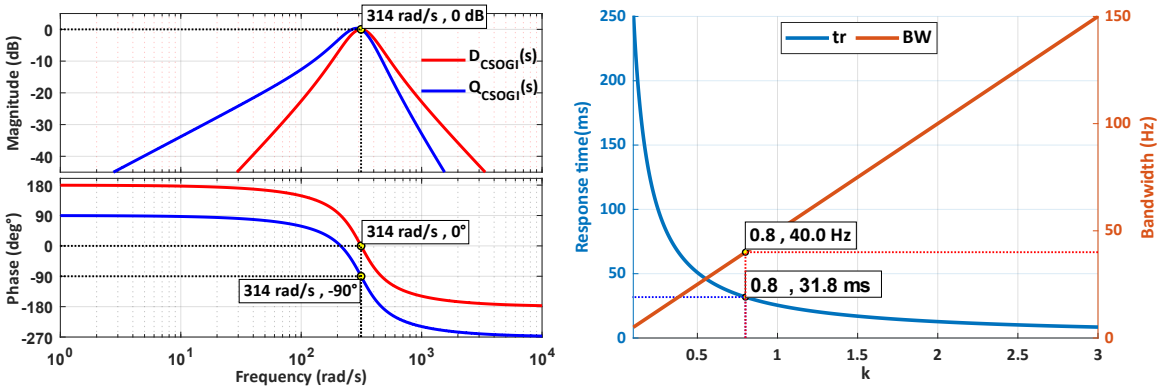
$$Q_{CSOGI}(s)=\frac{qv_s}{v}=\frac{k^2.{\omega_{PLL}}^3.s}{(s^2+k.\omega_{PLL}.s+{\omega_{PLL}}^2)^2} \quad (6)$$

$$t_s=\frac{4}{\xi.\omega_n} \quad (7)$$

$$Bandwidth=\frac{\omega_n.k}{2\pi} \quad (8)$$

As illustrated by the bode diagrams in Figure 5(a) and (5) and (6), the transfer function $D_{CSOGI}(s)$ exhibits a band-pass filtering characteristic, achieving unity gain at the frequency ω_{PLL} and stronger attenuation at frequencies that exceed its passband. It is also notable that the transfer function $D_{CSOGI}(s)$ introduces a phase shift of zero at ω_{PLL}, thereby ensuring that the output signal v_s is in phase with the input signal v and they have the same amplitude at this particular frequency. This configuration provides an additional filtering step, which in turn helps to reduce the impact of low/high-order frequency harmonics. For $Q_{CSOGI}(s)$, unlike the SOGI, it does not allow the DC component to pass through. It achieves a unity gain at the frequency ω_{PLL} and introduces a phase shift of -90° at this frequency. As a result, it generates qv_s, which is a filtered version of the input signal v, with the same amplitude and in quadrature at the frequency ω_{PLL}.

For the design of the cascaded SOGI block, the parameter k is the key factor that determines the dynamics of this block, which will have a significant impact on the response time of the C-SOGI block and its bandwidth, thus affecting its speed and its ability to filter low and high frequencies. To analyze this, we have plotted the evolution of the response time and bandwidth of the C-SOGI as a function of the value of k, using (7) and (8), as illustrated in Figure 5(b). The response time mentioned here refers to the 2% settling. It is observed that to achieve a good filtering effect, the value of k must be small. However, this comes at the cost of slower response time, creating a trade-off between the block's response time and its filtering performance. For this reason, a value of k = 0.8 has been chosen, which provides a bandwidth of 40 Hz and a response time of 32 ms. The choice of this bandwidth range [30 Hz, 70 Hz] is justified because it is sufficiently far from low-order harmonic frequencies [3rd, 5th, 7th ...]. At the closest harmonic frequency, which is the 3rd order one, the attenuation is less than -20 dB, whereas for the SOGI block with the same value of k, the attenuation at this frequency is only -10 dB.



(a) (b)

Figure 5. CSOGI model: (a) bode plot and (b) time response vs bandwidth

2.3. Discretization and implementation of the three-phase cascaded DSOGI-PLL

With regard to the integrated SRF-PLL, the parameters K_P and T_i for the PI controller are selected based on its closed-loop model [24], as outlined in (9). The damping ratio ξ is set to $\frac{\sqrt{2}}{2}$, as this value provides an optimal relationship between response time and overshoot in the dynamic response, while the natural frequency ω_n is selected as $2.\pi.55\ rad/s$ to match the desired bandwidth. This choice conforms to the IEEE standard, which allows for a frequency variation f up to $\pm 10\%$ around the nominal 50 Hz frequency in output unit vectors [25]. Using these values, we find $K_P = 345.5752$ and $T_i = 83.7$ ms.

$$\frac{\theta_{PLL}(s)}{\theta(s)} = \frac{K_P.s + \frac{K_p}{T_i}}{s^2 + K_P.s + \frac{K_p}{T_i}} \tag{9}$$

To implement the three-phase cascaded DSOGI PLL on a digital processor, it is necessary to discretize all its blocks. For this purpose, a sampling time of Ts = 100 µs has been chosen. We have selected the Tustin method [26], using (10), which gives a good approximation of an integrator.

$$s \rightarrow \frac{T_s}{2} \cdot \frac{1 - z^{-1}}{1 + z^{-1}} \tag{10}$$

The difference equations for the PI controller and the various integrators within this structure are provided by (11) and (12). The settling time of the SRF-PLL with the chosen values of K_P and T_i is $t_{SRF} = 16\ ms$. In the worst-case scenario for this structure, the total settling time will be the sum of the SRF bloc and the CSOGI blocks' settling time, resulting in $t_{CSOGI} = 48\ ms$ as mentioned in (13), hence, the structure will respond within a maximum of two and a half periods for any transient condition.

$$\text{PI controller: } y(n) = y(n-1) + 345.8 \times u(n) - 345.4 \times u(n-1) \tag{11}$$

$$\text{Integrators: } y(n) = y(n-1) + 5 \cdot 10^{-5} \times (u(n) - u(n-1)) \tag{12}$$

$$\text{Settling time : } t_s = t_{CSOGI} + t_{SRF} \approx 32 + 16 \approx 48\ ms \tag{13}$$

3. DISCUSSIONS OF THE OBTAINED RESULTS

This section presents the setup used to validate the PLL's performance and discusses the obtained results, focusing on its accuracy, time response, and robustness against disturbances.

3.1. The experimental setup

The cascaded DSOGI-PLL structure is validated using the experimental setup shown in Figure 6. In this setup, the cascaded DSOGI-PLL was implemented on the DSP board TMS320F28379D running at 200 MHz, with a sampling time of Ts = 100 µs. The DSP's onboard 12-bit ADC modules were used to acquire the three-phase voltage signals. A grid emulator, developed in our laboratory, was employed to generate test scenarios that emulate real grid conditions. The test signals produced include a 1.5 V DC offset and vary between 0 V and 3 V to match the ADC input range of the DSP board.

3.2. Scenario N°1: balanced grid

In this first test, a balanced grid voltage (V_a, V_b, V_c) of $\sqrt{2}.220$ V amplitude and 50 Hz frequency was applied to the input of the DSP, as illustrated in Figure 7(a). It can be observed that the PLL locks within 20 ms after startup, and the phase angle θ_{PLL} exhibits a linear trend, as shown in Figure 7(b), which represents the evolution of the phase angle generated by the PLL along with the grid voltage V_a. In the steady-state condition, depicted in Figure 7(c), the signal V_{a_PLL}, which represents the unit vector output of the PLL, is in phase with the grid signal V_a. This demonstrates, first and foremost, the ability of this structure to quickly adapt to a balanced grid.

3.3. Scenario N°2: unbalanced grid

Figure 8(a) illustrates the signal applied to the input of the PLL in the case of an unbalanced grid, where the positive sequence is $\sqrt{2}.220$ V and the negative sequence is $\sqrt{2}.50$ V which gives an imbalance rate of 22%. From the transient response shown in Figure 8(b) and the steady-state response depicted in Figure 8(c), it is evident that the PLL is completely insensitive to this type of imperfection. Despite the application of such a disturbance, the PLL remains locked to the grid's fundamental component, and the phase angle maintains its linear curve. Furthermore, the unit vector output V_{a_PLL} remains in phase with the grid signal V_a, confirming the robustness of this structure in maintaining synchronization despite grid imperfections.

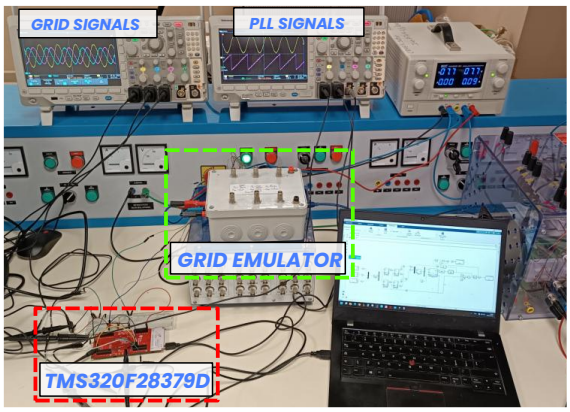


Figure 6. The practical experimental setup

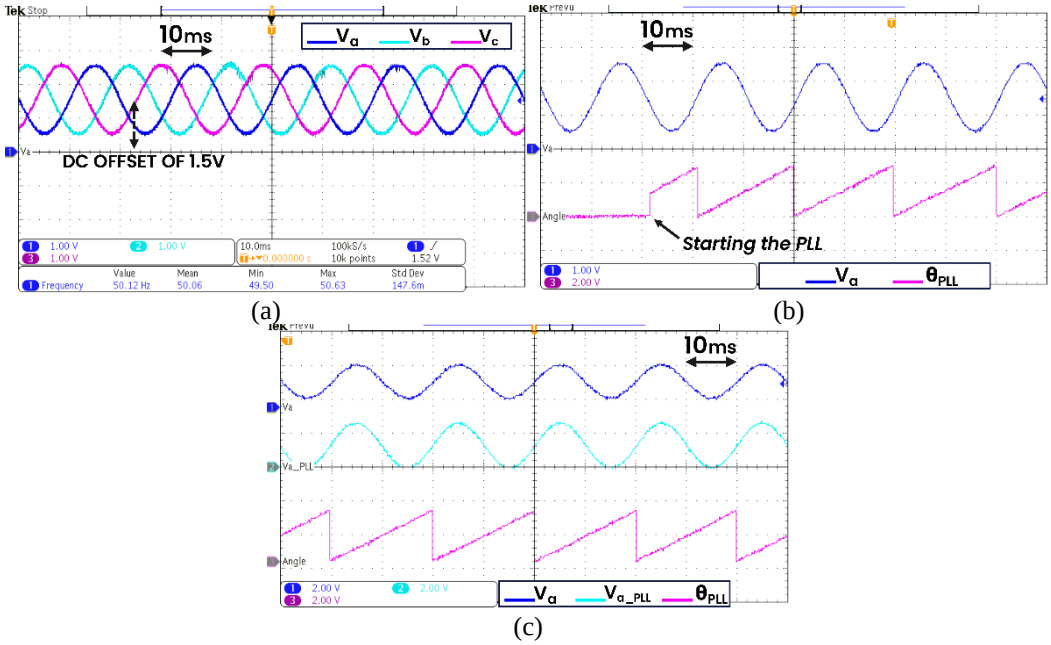


Figure 7. Balanced grid: (a) grid voltage, (b) transient, and (c) steady-state response

3.4. Scenario N°3: frequency variation

In this test, a frequency jump of -5 Hz was applied to the grid, as illustrated in Figure 9(a), resulting in a grid frequency of 45 Hz. From the transient response shown in Figure 9(b), it is observed that the PLL locks within 20 ms, and the unit vector signal V_{a_PLL} aligns perfectly with the grid signal V_a. In addition, Figure 9(c) presents the steady-state response, where the PLL generates a linear phase angle θ_{PLL} that evolves in sync with the grid signal V_a, demonstrating its ability to accurately track and adapt to frequency variations.

3.5. Scenario N°4: presence of harmonics

In this test, the 5th harmonic with an amplitude of $\sqrt{2}.50$ V was injected into the grid signal, while the fundamental component of the grid remained at $\sqrt{2}.220$ V, resulting in a THD of 22%, as illustrated in Figure 10(a). It is clear that, even under such a disturbance, the PLL output remains locked to the grid's fundamental component, as shown in Figure 10(b). The phase angle θ_{PLL} maintains a purely linear trend, and the unit vector signal V_{a_PLL} aligns perfectly with the grid's fundamental. A quantitative analysis shows that the unit vector V_{a_PLL} has very low distortion, with a THD of around 0.5%. This is much lower than the 22% THD present in the input signal. This is further confirmed by the PLL's steady-state response in Figure 10(c), which demonstrates its ability to effectively handle harmonic distortions originating from the grid.

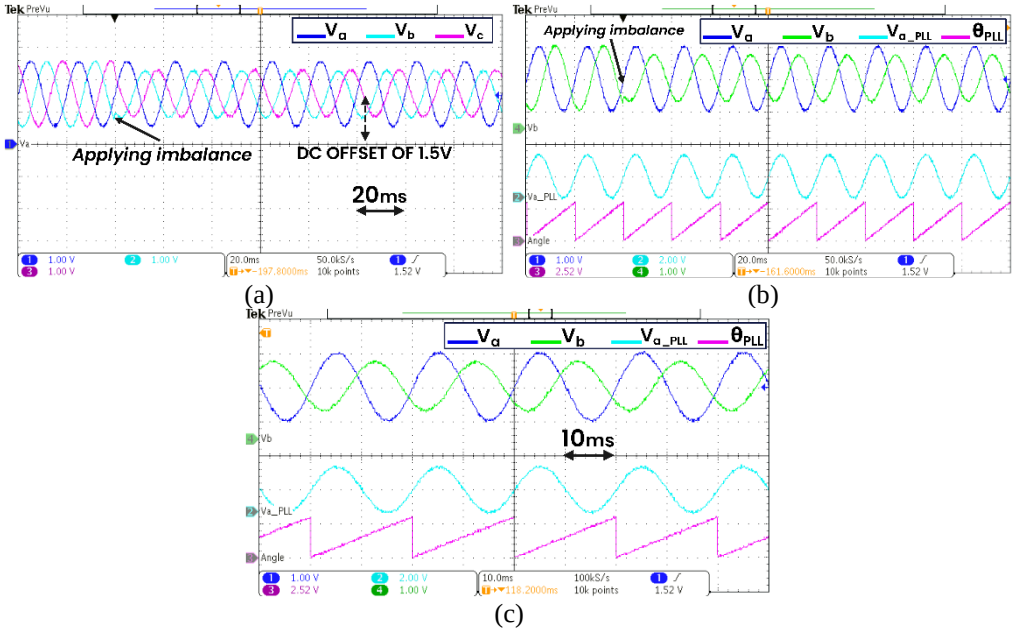


Figure 8. Unbalanced grid: (a) grid voltage, (b) transient, and (c) steady-state response

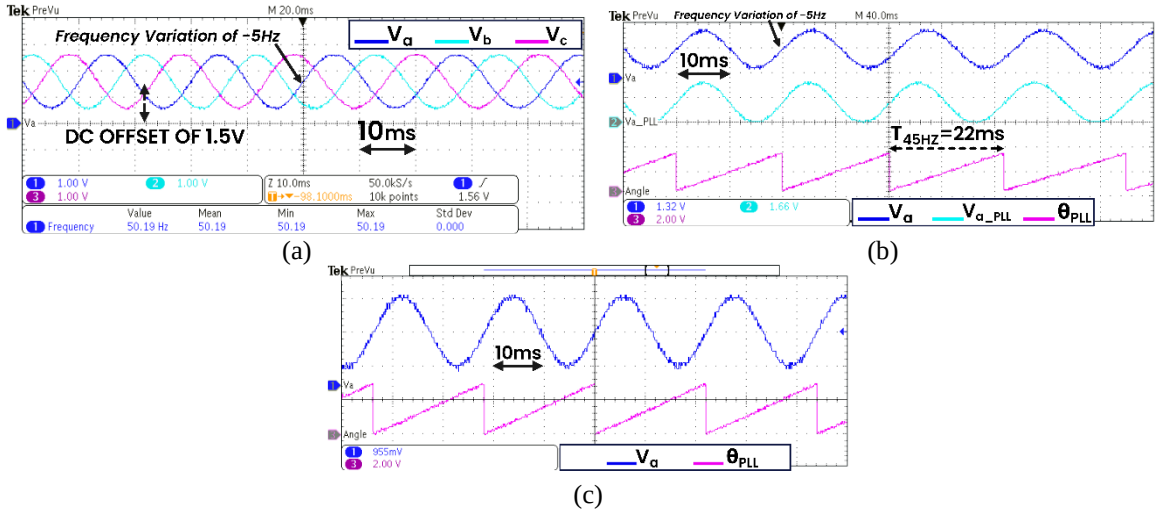


Figure 9. Frequency variation test: (a) grid voltage, (b) transient, and (c) steady-state response

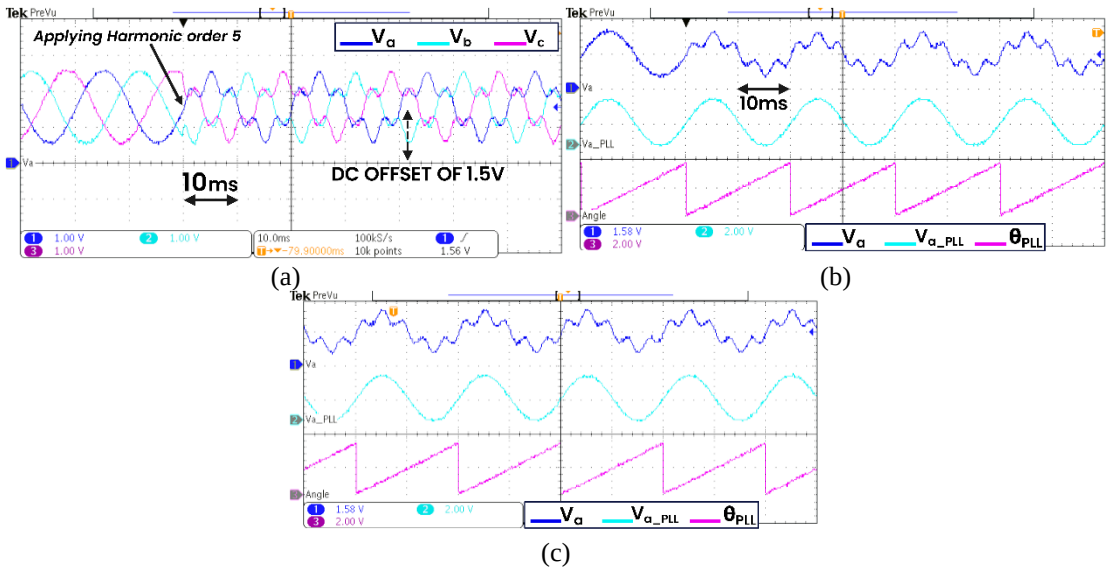


Figure 10. Distorted grid: (a) grid voltage, (b) transient, and (c) steady-state response

3.6. Summary of work and results discussion

Through a series of test scenarios emulating real grid disturbances, the proposed cascaded DSOGI-PLL demonstrated its effectiveness in rejecting these disturbances. Notably, all the grid signals tested contained a DC offset of 1.5 V, but the results confirmed that the PLL had succeeded in eliminating this offset entirely. What's more, during the voltage distortion test, particularly with the 5th harmonic, which is a low-order harmonic, the PLL remained highly resistant. Despite imposing a relatively high THD of 22% on the mains voltage, the PLL reduced the distortion of its unit-vector output to approximately 0.5%, while the phase angle response remained linear, indicating great strength in the face of such disturbances. In terms of response time, the PLL was able to synchronize in the worst case over two and a half cycles of fundamental grid voltage, i.e. around 48 ms, making it ideally suited to applications such as power injection and active power filtering, where fast, precise control actions are crucial. In addition, frequency variation tests confirmed that the PLL's output accurately followed frequency changes, guaranteeing reliable synchronization under dynamic grid conditions. In the case of voltage imbalance, no distortion was observed in the PLL's output, demonstrating once again its ability to cope with a wide range of grid conditions. Lastly, the structure could be further improved by developing an adaptive tuning mechanism for the SOGI blocks, allowing the coefficient "k" to dynamically adjust and achieve an optimal trade-off between PLL response time and bandwidth based on real-time grid conditions.

4. CONCLUSION

This work presents the design, implementation, and validation of a cascaded DSOGI-PLL to enhance synchronization in grid-connected systems under challenging conditions. By overcoming DSOGI-PLL's limitations in handling DC offsets and low-order harmonics, the proposed approach improves phase estimation accuracy and robustness. Experimental results confirm the PLL's performance, demonstrating fast and accurate synchronization across all tested scenarios, making it a reliable solution for synchronization. To further improve performance, future work will focus on developing an adaptive version of the cascaded DSOGI block, improving the trade-off between response time and bandwidth. This step forward will refine the dynamic behaviour of the PLL, guaranteeing even greater adaptability to grid disturbances.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Ilias En-Naoui	✓	✓	✓	✓		✓	✓		✓		✓			
Abdelhadi Radouane		✓		✓	✓					✓	✓	✓		
Azeddine Mouhsen						✓				✓	✓	✓		
Hamid Yantour					✓					✓	✓	✓		

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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BIOGRAPHIES OF AUTHORS

Ilias En-Naoui is a Ph.D. student, received his master's degree in electrical engineering from the Faculty of Science and Technology Settat in 2019, and he is currently a professor of electrical engineering in the agrégation cycle at the Ministry of National Education, Morocco. His research areas include power electronics, renewable energy, and power quality. Laboratory of Radiation-Matter and Instrumentation (RMI), Faculty of Sciences and Technology, Hassan 1st University, Morocco. He can be contacted at email: i.ennaoui@uhp.ac.ma.

Abdelhadi Radouane was born in 1969. He received the Agrégation degree in Electrical Engineering from the ENSET of Rabat, Morocco, in 1996. In 2017, he obtained a Ph.D. in automatic control. Since 2018, he joined the FST Settat, Hassan First University of Settat, Morocco, as an assistant professor. He can be contacted at email: abdelhadi.radouane@uhp.ac.ma.

Azeddine Mouhsen born in 10 July 1967. He has been a professor of physics at Hassan First University, Morocco, since 1996. He holds a Ph.D. from Bordeaux I University (France) in 1995 and a thesis from Moulay Ismail University, Morocco, in 2001. He specializes in instrumentation and measurements, sensors, energy transfer, and radiation-matter interactions. He has taught courses in physical sensors, chemical sensors, instrumentation, systems technology, digital electronics, and industrial data processing. Actually, he is the Director of the Laboratory of Radiation-Matter and Instrumentation. He can be contacted at email: az.mouhsen@gmail.com.

Hamid Yantour born in 1964, received the master's degree in automatic, signal processing, and Industrial Computing (ATSII) from Hassan 1st University, Morocco in 2011. He obtained a Ph.D. in Automatic and Production in 2016. Currently, he is a professor of Electrical Engineering at the Regional Center for Education and Training Professions (CRMEF) in Settat. He can be contacted at email: yantourhamid@gmail.com.