International Journal of Power Electronics and Drive System (IJPEDS)
Vol. 17, No. 1, March 2026, pp. 476~486
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v17.i1.pp476-486

A novel single-switch DC–DC converter using the coupled inductor with ultra-high voltage gain

Kim-Anh Nguyen, Thai Anh Au Tran, Xuan Khanh Ho, Duong Thach Pham
Faculty of Electrical Engineering, The University of Danang - University of Science and Technology, Danang, Vietnam

Article Info

Article history:

Received Mar 30, 2025
Revised Oct 21, 2025
Accepted Dec 11, 2025

Keywords:

DC–DC converter
Coupled inductor
High voltage gain
Single switch
Renewable energy systems

ABSTRACT

This paper presents an extremely high step-up DC–DC converter using a quadratic topology and a coupled inductor (CI). The proposed converter (PC) utilizes a single switch, simplifying the control strategy and reducing switching losses. A passive clamp circuit recycles leakage energy, reducing voltage stress (VS) on the MOSFET and enabling the implementation of a low on-state resistance switch for higher efficiency. Additionally, the quadratic structure and passive clamp circuit contribute to higher voltage gain (VG) and better performance. The converter's operating principles, steady-state analysis, and component selection criteria are discussed in detail. The influence of magnetizing inductance, duty cycle, and parasitic components on the VG is also investigated, along with the system's dynamic response under input voltage and load variations to ensure stable operation. A comparative evaluation with existing converters highlights its advantages. The PC is verified through SIMPLIS simulations, where key performance metrics such as VG and switching stress are analyzed. Furthermore, a hardware prototype with a power rating of 300 W is built to confirm the theory and showcase the converter's performance. Experimental results demonstrate high efficiency, stable operation, and substantial VG, validating the converter's feasibility for renewable energy systems (RES).

Corresponding Author:

Thai Anh Au Tran
Faculty of Electrical Engineering, The University of Danang - University of Science and Technology
54 Nguyen Luong Bang Street, Lien Chieu Ward, Danang 550000, Vietnam
Email: ttaau@dut.udn.vn

1. INTRODUCTION

With the rising global energy demand and increasing environmental concerns, renewable energy sources are considered key to achieving a cleaner and more sustainable future [1]–[3]. Research efforts continue to focus on enhancing these technologies to improve efficiency and reliability in modern energy systems [4], [5]. Nevertheless, photovoltaic panels, fuel cells, wind turbines, and wave energy systems typically generate low and fluctuating output voltages, creating challenges for practical applications [6]. To address this issue, converters with high VG are crucial for increasing voltage levels and maintaining stable power delivery in RES. Conventional boost converters attain high VG by extending the duty cycle. Yet, as the duty cycle approaches unity, parasitic resistances in the inductor, switch, and diode cause significant conduction losses, reducing efficiency and increasing current stress on components [7]. Moreover, extreme duty cycles lead to slow transient response and higher electromagnetic interference (EMI). To overcome these issues, voltage lift and super-lift techniques enhance VG without requiring excessive duty cycles [8]–[12]. Nonetheless, these methods introduce additional passive and active components, leading to increased circuit complexity, higher conduction and switching losses at heavy loads, control challenges due to multiple energy storage elements, greater VS on components, and slower dynamic response. To overcome VG limitations, cascade boost

converters use multiple boost stages in series, reducing the need for extreme duty cycles [13], [14]. However, this increases the number of inductors, capacitors, and switches, making the circuit more complex. Precise control is required to ensure stability, adding design challenges and switching losses. Switched-capacitor techniques achieve high VG without inductors, providing benefits such as high-power density, low EMI, and simplified control [15]–[18]. However, they also have drawbacks, including limited load capacity, increased VS on components, higher switching losses, and a fixed VG, which reduces flexibility for varying input conditions. Switched inductors [19]–[23] boost VG and efficiency by improving energy transfer. Even so, they increase circuit complexity, switching losses, and EMI.

The CI boosts voltage at moderate duty cycles. It efficiently transfers energy by magnetically linking two inductors. A CI is employed for the first time in the published topology to achieve high VG [24]. Nevertheless, this design faces leakage inductance, causing high VS. These voltage spikes can cause excessive VS on the semiconductor components, potentially reducing reliability and efficiency. Clamping circuits, such as diode-capacitor clamping, effectively suppress voltage spikes and reduce stress on switching devices by absorbing and redistributing excess energy [25]–[27]. Nonetheless, they introduce drawbacks such as increased input current ripple, which raises conduction losses and EMI. This can negatively impact overall efficiency and may require additional filtering components, adding to circuit complexity. Voltage multiplier cells help boost voltage efficiently in DC–DC converters by using capacitors and diodes [28]–[30]. They reduce stress on components, improve efficiency, and allow for modular expansion. However, they increase circuit complexity, may cause voltage imbalance, and have limitations in handling high power. Quadratic converters with input inductors cut ripple and boost VG, making them ideal for high-gain applications. A quadratic boost converter featuring reduced VS is proposed [31]. Nevertheless, it experiences significant fluctuations in the input current, limiting its applications. A passive snubber in a converter prevents voltage spikes without energy loss, enhancing efficiency [32], but its VG remains limited. A high VG circuit with smooth input current using a CI is also presented [33]; even so, achieving high VG requires a high turns ratio of the CI and a large number of components. While quadratic converters have significantly improved VG, there is still room for further enhancement.

After evaluating the merits and drawbacks of the discussed converters, a new topology is proposed with the following features: By integrating a boost stage and a CI, a quadratic boost converter attains extremely high VG while ensuring minimal VS of a single switch. The input-side inductor ensures continuous input current with minimal ripple, improving overall performance. Additionally, a passive clamp suppresses switch voltage spikes, lowering conduction losses and achieving higher efficiency.

2. OPERATING PRINCIPLES

The topology of the PC is shown in Figure 1. The circuit comprises inductor L_1, single switch S, six diodes labeled $D_1$to D_6, five capacitors C_1~C_4 and C_0, and a CI. The CI is represented by primary (N_P) and secondary (N_S) windings, with the parameters L_m and L_k indicating the magnetizing and leakage inductances, respectively. The voltage-clamp-circuit made up of D_3 and C_2 helps recycle leakage energy and clamp VS on switch S. For convenient analysis, the circuit operates under the following assumptions:

- All power devices are treated as ideal;
- All capacitors possess high capacitance values, allowing their voltages to remain almost unchanged;
- The CI's winding ratio is given by $n = N_S/N_P$.

The waveforms of the PC, including the control signal (v_{gs}), the magnetizing current (i_{Lm}), the leakage current (i_{Lk}), and the VS of MOSFET (v_{ds}), and the diode currents ($i_{D1} - i_{D6}$), are illustrated in Figure 2. The PC's operating modes are depicted in Figure 3 and are discussed in the next section.

- Mode I ($t_0 - t_1$) **[**Figure 3(a)]: v_{gs} is high, S is ON. D_2 and D_5 are ON, while D_1, D_3, D_4, and D_6 remain OFF. i_{L_k} is greater than i_{L_m}, and both i_{L_k} and i_{L_m} are positive and increasing. V_{in} supplies L_1. V_{in} and C_1 discharge energy to i_{L_k}, i_{L_m}, and also to C_2 and C_4 through the CI. Simultaneously, C_3 transfers energy to C_2 and C_4, while C_0 delivers power to the load. This mode terminates when v_{gs} transitions to low at $t = t_1$.
- Mode II ($t_1 - t_2$) **[**Figure 3(b)]: v_{gs} is low, S is OFF. D_2, D_4, and D_5 are OFF, while D_1, D_3, and D_6 are ON. i_{L_k} is less than i_{L_m}, with i_{L_k} remaining positive. Both i_{L_m} and i_{L_k} decrease. C_1 is energized by L_1. Meanwhile, L_1, V_{in}, L_m, and L_k transfer energy to charge C_2. Additionally, C_0 is powered by L_m, L_1, V_{in}, and C_4. This mode terminates when C_2 is fully charged and D_4 turns on at $t = t_2$.
- Mode III ($t_2 - t_3$) [Figure 3(c)]: v_{gs} is low, S is OFF. D_2 and D_5 are OFF, while the remaining diodes are ON. i_{L_k} is less than i_{L_m}, with i_{L_k} remaining positive. Both i_{L_m} and i_{L_k} decrease. The input voltage V_{in}, along with L_1, L_m, L_k, and C_4, supplies energy to C_3, and together with the energy in C_4, delivers power to the load through diode D_6. The load in conjunction with C_2, effectively recycling the leakage energy. The current i_{D_3} equals i_{L_k} and decreases over time. This mode terminates when i_{D_3} and i_{L_k} reaches zero at $t = t_3$.

- Mode IV ($t_3 - t_4$) [Figure 3(d)]: v_{gs} is low, switch S is OFF. D_2, D_3, and D_5 are OFF, while D_1, D_4, and D_6 are ON. $i_{L_k} = 0$, while i_{L_m} remains positive and decreasing. C_1 continues to be charged by L_1. Meanwhile, C_2 and $V_{\mathrm{Lm}}, V_{\mathrm{in}}$ supply energy to charge C_3. Additionally, C_2, C_4, and $L_{\mathrm{m}}, V_{\mathrm{in}}$ provide power to C_0 and the load. This mode concludes when v_{gs} is high at $t = t_4$.

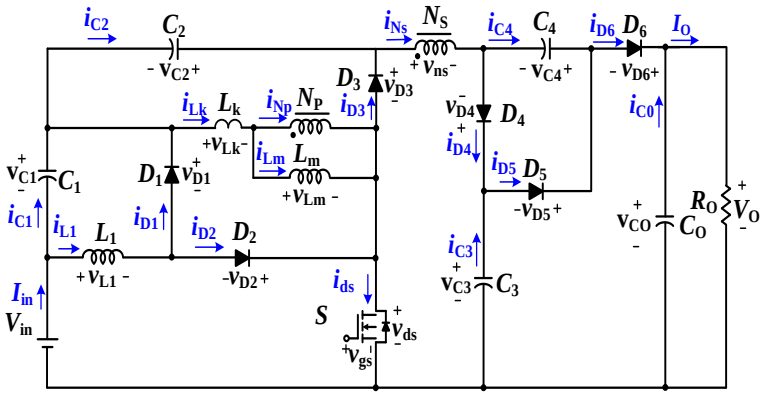


Figure 1. The PC

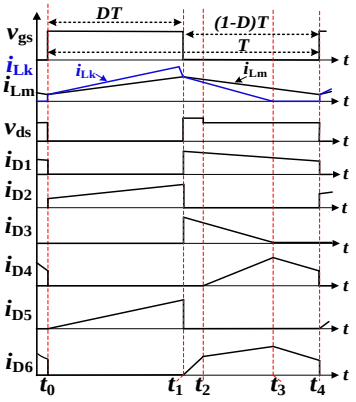


Figure 2. Key operating waveforms of the PC over one switching period

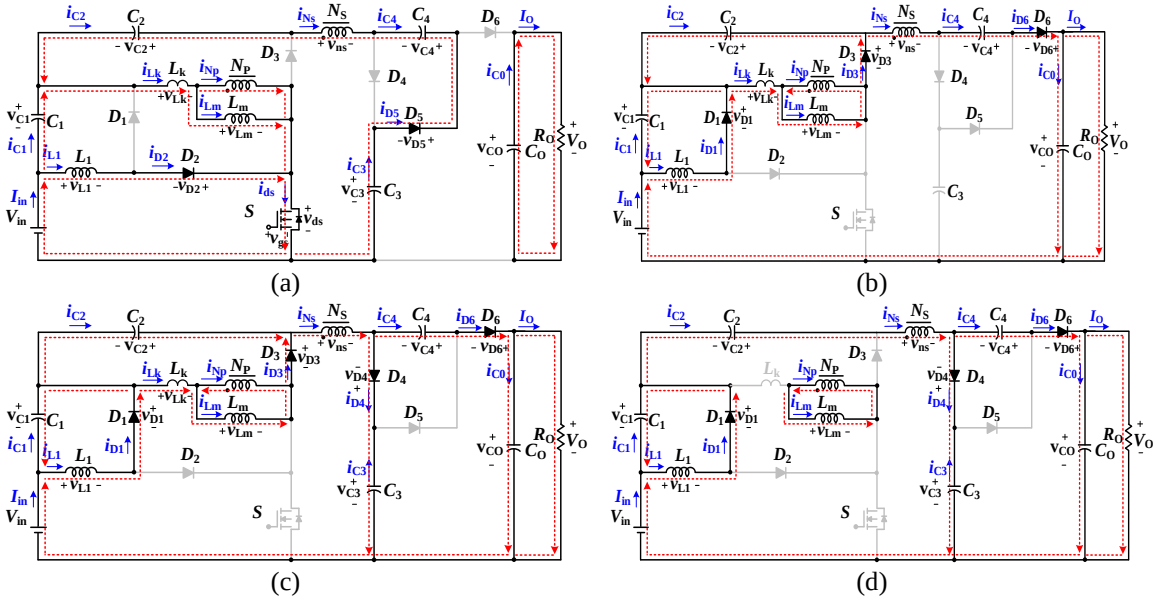


Figure 3. Equivalent circuits of the PC in different operating: (a) mode I, (b) mode II, (c) mode III, and (d) mode IV

3. STEADY-STATE CHARACTERISTICS OF THE PROPOSED CONVERTER

3.1. VG analysis

In this subsection, the analysis is performed based on ideal conditions that all semiconductor devices are ideal (i.e., negligible switch resistance and diode voltage drop), and all passive components (inductors and capacitors) are lossless, having negligible equivalent series resistance (ESR). These assumptions allow a straightforward derivation of the fundamental voltage-gain characteristic, which reflects the intrinsic step-up capability of the PC.

Let the switching period be represented by T, and let D denote the duty ratio of switch S. From Figure 3(a), during the switch-ON interval, $0 < t < DT$, by using Kirchhoff's voltage law, we obtain:

$$v_{L1} = V_{in} \quad (1)$$

$$v_{Lm} = V_{in} + V_{C1} \quad (2)$$

$$V_{C4} + V_{C2} + V_{C1} + V_{in} = V_{C3} + nv_{Lm} \quad (3)$$

From Figure 3(c), during the switch-OFF interval, $DT < t < T$:

$$v_{L1} = -V_{C1} \quad (4)$$

$$v_{Lm} = -V_{C2} \quad (5)$$

$$V_{in} = v_{L1} + (n+1)v_{Lm} + V_{C3} \quad (6)$$

$$V_{C0} = V_{C3} + V_{C4} \quad (7)$$

By enforcing the volt–second balance across L_1 and L_m over one switching period T yields:

$$\int_0^{DT} v_{L1}dt + \int_{DT}^{T} v_{L1}dt = \int_0^{DT} V_{in}dt + \int_{DT}^{T}(-V_{C1})dt = 0 \quad (8)$$

$$\int_0^{DT} v_{Lm}dt + \int_{DT}^{T} v_{Lm}dt = \int_0^{DT}(V_{in} + V_{C1})dt + \int_{DT}^{T}(-V_{C2})dt = 0 \quad (9)$$

From (8), V_{C1} is determined as (10).

$$DV_{in} + (1-D)V_{C1} = 0 \rightarrow V_{C1} = \frac{DV_{in}}{1-D} \quad (10)$$

Based on (9) and (10), V_{C2} is determined:

$$D(V_{in} + V_{C1}) - (1-D)V_{C2} = 0 \rightarrow V_{C2} = \frac{D(V_{in}+V_{C1})}{1-D} = \frac{DV_{in}}{(1-D)^2} \quad (11)$$

Using (4)–(6) and combining the voltage relations for C_1 and C_2 from (10) and (11), V_{C3} is obtained as (12).

$$\begin{aligned} V_{C3} &= V_{in} - v_{L1} - (n+1)v_{Lm} = V_{in} + V_{C1} + (n+1)V_{C2} \\ &= V_{in} + \frac{D}{1-D}V_{in} + (n+1)\frac{D}{(1-D)^2}V_{in} = \frac{1+nD}{(1-D)^2}V_{in} \end{aligned} \quad (12)$$

Based on (1) and (3) and the voltage expressions for C_1–C_3 in (10)–(12), V_{C4} is given by (13).

$$\begin{aligned} V_{C4} &= V_{C3} + nv_{Lm} - V_{C1} - V_{in} - V_{C2} = V_{C3} + n(V_{in} + V_{C1}) - V_{C1} - V_{in} - V_{C2} \\ &= \frac{1+nD}{(1-D)^2}V_{in} + n\left(V_{in} + \frac{D}{1-D}V_{in}\right) - \frac{D}{1-D}V_{in} - V_{in} - \frac{DV_{in}}{(1-D)^2} = \frac{n}{(1-D)^2}V_{in} \end{aligned} \quad (13)$$

Replacing (12) and (13) in (7), The PC's VG is (14).

$$M = \frac{V_O}{V_{in}} = V_{C0} = V_{C3} + V_{C4} = \frac{1+nD}{(1-D)^2}V_{in} + \frac{n}{(1-D)^2}V_{in} = \frac{n+1+nD}{(1-D)^2} \quad (14)$$

3.2. VS analysis

The VSs on power devices are:

$$\begin{cases} V_S = V_{D3} = V_{in} + V_{C1} + V_{C2} = V_{in} + \frac{D\,V_{in}}{1-D} + \frac{DV_{in}}{(1-D)^2} = \frac{1}{(1-D)^2}V_{in} = \frac{1}{n+1+nD}V_O \\ V_{D1} = V_{D2} = V_{in} + V_{C1} = V_{in} + \frac{D}{1-D}V_{in} = \frac{1}{1-D}V_{in} = \frac{1-D}{n+1+nD}V_O \\ V_{D4} = V_{D5} = V_{D6} = V_{C4} = \frac{n}{(1-D)^2}V_{in} = \frac{n}{n+1+nD}V_O \text{ where } V_{D6} = V_{Co} - V_{C3} = V_{C4} \end{cases} \quad (15)$$

3.3. Converter design considerations

Based on Figure 1, applying Kirchhoff's current law (KCL) gives the (16)-(18).

$$\frac{1}{T}\int_0^T i_{D4}\,dt = \frac{1}{T}\int_0^T (I_O - i_{C0} - i_{C3} - i_{C4})\,dt = I_O \quad (16)$$

$$\frac{1}{T}\int_0^T i_{D3}\,dt = \frac{1}{T}\int_0^T (i_{D4} + i_{C4} - i_{C2})\,dt = I_O \quad (17)$$

$$\frac{1}{T}\int_0^T i_{\mathrm{D6}}\,dt = \frac{1}{T}\int_0^T (I_{\mathrm{O}} - i_{\mathrm{C0}})\,dt = I_{\mathrm{O}} \quad (18)$$

During DT ~ T, according to KCL, the subsequent equation is derived:

$$\frac{1}{T}\int_{DT}^T i_{\mathrm{Lm}}dt = \frac{1}{T}\int_{DT}^T n(i_{\mathrm{D4}} + i_{\mathrm{D6}})dt + \frac{1}{T}\int_{DT}^T i_{\mathrm{D3}}\,dt \quad (19)$$

From (16)–(19), the average current of inductor is (20).

$$\frac{1}{T}\int_{DT}^T i_{\mathrm{Lm}}dt = I_{\mathrm{O}}(1+2n) \quad (20)$$

From (20), $i_{\mathrm{Lm\_ave}}$ is deduced as (21).

$$i_{\mathrm{Lm\_ave}} = \frac{(2n+1)I_{\mathrm{O}}}{1-D} \quad (21)$$

The ripple current of the CI is (22).

$$\Delta i_{\mathrm{Lm}} = i_{\mathrm{Lm\_max}} - i_{\mathrm{Lm\_min}} \quad (22)$$

Within $t \in (0 \div DT)$, the voltage across L_{m} can be calculated using the (23).

$$v_{\mathrm{Lm}} = L_{\mathrm{m}}\frac{di_{\mathrm{Lm}}}{dt} \rightarrow \frac{di_{\mathrm{Lm}}}{dt} = \frac{V_{\mathrm{Lm}}}{L_{\mathrm{m}}} \quad (23)$$

Using (22) and (23), the current variation across L_{m} is (24).

$$\Delta i_{\mathrm{Lm}} = \int_0^{DT} i_{\mathrm{Lm}}\,dt = \int_0^{DT}\frac{V_{\mathrm{Lm}}}{L_{\mathrm{m}}}dt = \frac{V_{\mathrm{Lm}}}{L_{\mathrm{m}}}DT \quad (24)$$

Based on the recently calculated (24), we derive:

$$\Delta i_{\mathrm{Lm}} = \frac{V_{\mathrm{in}}+V_{\mathrm{C1}}}{L_{\mathrm{m}}}DT \quad (25)$$

To ensure the circuit operates under continuous conduction mode, half of the ripple current $\Delta i_{\mathrm{Lm}}/2$ of L_{m} must be less than the average current $i_{\mathrm{Lm\_ave}}$. From (21) and (25) , the inductance is designed using (26):

$$L_{\mathrm{m}} = \frac{V_{\mathrm{o}}}{2P_0(2n+1)}DT \quad (26)$$

where, $P_0 = V_{\mathrm{in}}I_{\mathrm{in}}$

In reality, selecting 40% of the load, so the inductor is designed as (27).

$$L_{\mathrm{m\_design}} = \frac{V_{\mathrm{O}}V_{\mathrm{in}}}{2P_0(2n+1)*0.4}DT \quad (27)$$

The average current in L_1 is based on its variation over $t \in (0 \div DT)$:

$$i_{\mathrm{L1\_ave}} = \frac{\Delta i_{\mathrm{L1}}}{2} = \frac{1}{T}\int_0^{DT}\frac{i_{\mathrm{L1}}}{2}dt = \frac{V_{\mathrm{L1}}}{2L_1}DT \quad (28)$$

Based on (28), the design of inductor L_1 is determined according to (29).

$$L_{\mathrm{L1\_design}} = \frac{V_{\mathrm{in}}^2}{2*0.4*P_0}DT \quad (29)$$

The capacitor selection is based on (30):

$$\begin{cases} C_0 = \frac{(1-D)V_{\mathrm{O}}}{f_{\mathrm{s}}R_0\Delta V_0} \\ C_1 = \frac{(1-D)I_{\mathrm{in}}}{f_{\mathrm{s}}\Delta V_{\mathrm{C1}}} \end{cases} \begin{cases} C_{2,4} = \frac{DI_{\mathrm{in}}}{nf_{\mathrm{s}}\Delta V_{\mathrm{C2,4}}} \\ C_3 = \frac{(1-D)I_{\mathrm{in}}}{nf_{\mathrm{s}}\Delta V_{\mathrm{C2,4}}} \end{cases} \quad (30)$$

where, voltage ripple, switching frequency, and load resistor are represented by ΔV_{O}, f_{s}, and R_0, respectively.

4. RESULTS AND DISCUSSION

4.1. Simulation and experimental results

To substantiate the theoretical predictions, a 300 W converter prototype was constructed, simulated in Simplis/Simetrix, based on the specifications of $f_s = 50$ kHz, $V_{in} = 24$ V, $V_O = 400$ V. From (14), the nominal VG and the duty ratio are given by M = 16.67. Based on the prototype specifications and (14), the VG versus duty cycle D for different CI turn ratios: n = 1.5 to 3 is shown in Figure 4. To achieve a suitable turns ratio, n is selected as 2. L_m is calculated by (27) and found to be 82 µH. Using (29), L_1 is designed as 25 µH. The capacitors are selected as (30). Table 1 displays the key parameters of the design prototype.

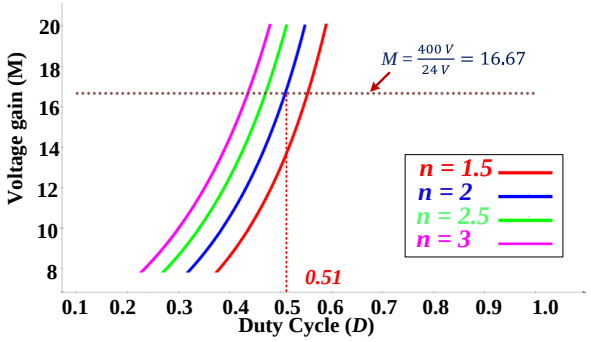


Figure 4. VG curves versus duty cycle at different turn ratios

Table 1. Hardware component specifications of the PC

Devices	Values
D_1 –D_5	DSEP30-06A
D_6	MUR3060PT
S	IRFP250N
C_1	47 µF
C_O	330 µF
$C_2 - C_4$	56 µF
CI	Lm = 82 µH; Lk = 1.8 µH
L_1	25 µH
$N_p : N_s$	1 : 2

Figures 5(a) and 5(b) show the simulated circuit diagram and setup of the PC in Simplis/Simetrix. Figure 6(a) display v_{gs}, i_{Lm} and i_{Lk} of the CI, i_{L1}, v_{ds}, and V_O. The simulation results align well with the analytical theory. The input inductor current remains continuous, ensuring stable operation. The VS on the MOSFET is low and exhibits a waveform consistent with theoretical predictions. V_O is approximately 400 V as designed, with minimal deviation, demonstrating the converter's high accuracy and efficiency. Figure 6(b) presents the diode current profiles. It is evident that the waveforms closely match the analytical theory, further validating the accuracy of the PC model.

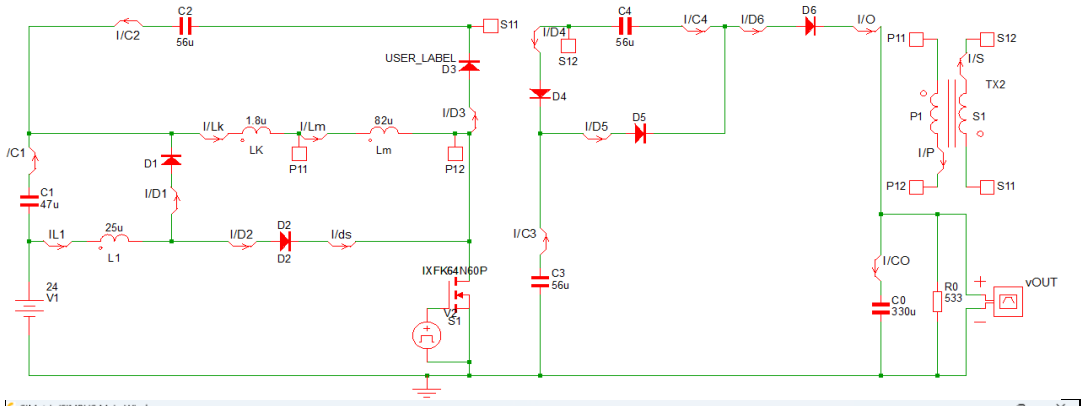
The influence of magnetizing inductance (L_m) tolerance on the output voltage was verified by simulating the proposed circuit with L_m variations of ±5% in Simetrix-SIMPLIS. As shown in Figure 7 for 95%, 100%, and 105% L_m values, a decrease in L_m causes a slight increase in V_O, while increasing L_m slightly reduces. These output voltage fluctuations are, however, minimal and insignificant. This result confirms that the output voltage stays stable, even with typical component tolerances.

To verify the PC performance, a lab prototype was built. The design parameters appear in Table 1. Figure 8 shows the experimental setup of the prototype. The lab setup includes the converter prototype, a control board, a resistive load, and an oscilloscope for waveform measurement, as shown in Figure 8. The prototype of the PC appears in Figure 8(a), while the experimental setup is illustrated in Figure 8(b).

Figure 9(a) presents the hardware waveforms, including v_{gs}, v_{ds}, V_{in}, and V_O. Based on (14) in the revised manuscript, with an output power of P_O = 300 W, V_O = 400 V, V_{in} = 24 V, and n = 2, the theoretical D is calculated to be 50.9%. However, under practical conditions, due to factors such as ESR of capacitors, core losses, diode conduction losses, switching losses, and non-ideal operating conditions, the actual duty cycle implemented in hardware is marginally higher (51.3%) than the theoretical value to achieve V_O = 400 V. As observed, the VS across the MOSFET remains low and consistent with the design analysis, while V_O is stably held at 400 V. The measured peak efficiency of the prototype reaches 93.6%, confirming the good performance of the PC. The output voltage ripple at full-load operation is also seen in Figure 9(a). The measured peak-to-

peak ripple is approximately ΔV_O = 2 V, corresponding to about 0.5% of the rated output voltage, which is within acceptable limits for high VG converters.

(a)



(b)

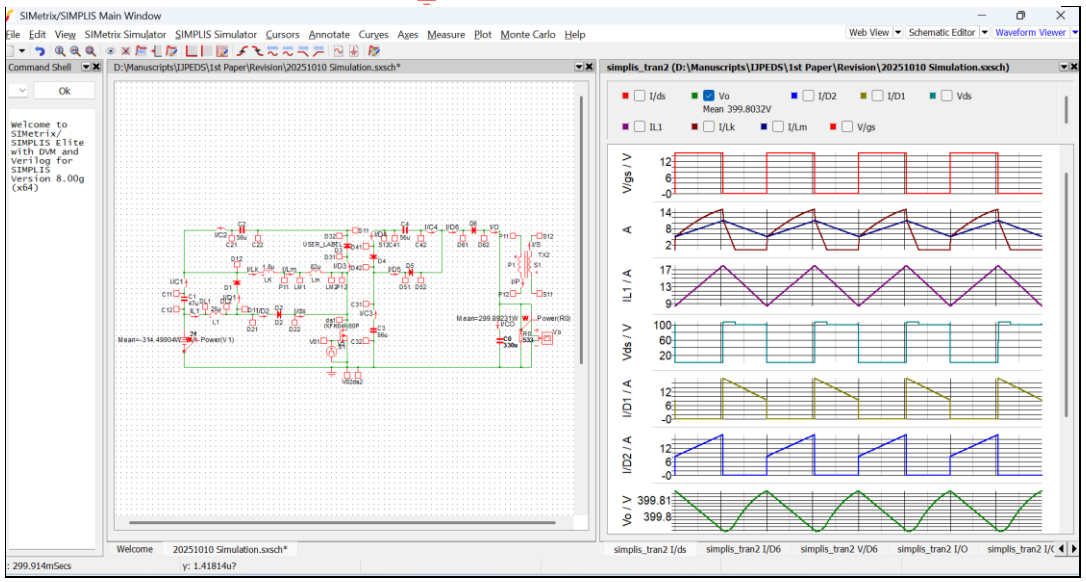


Figure 5. Simulation model and setup of the PC: (a) diagram and (b) setup

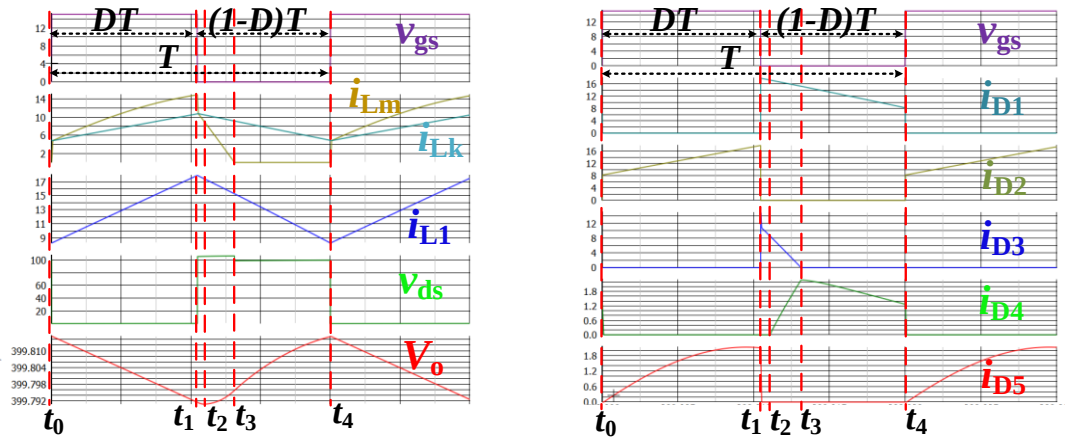


Figure 6. Simulation waveforms: (a) v_{gs}, v_{ds}, i_{L1} and (b) v_{gs}, i_{Lk}, i_{Lm}

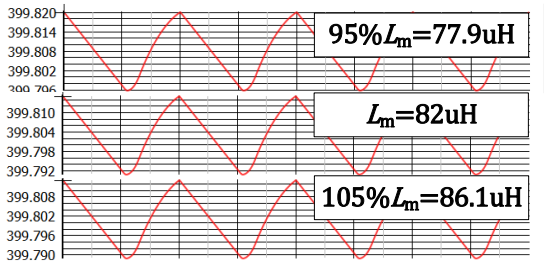
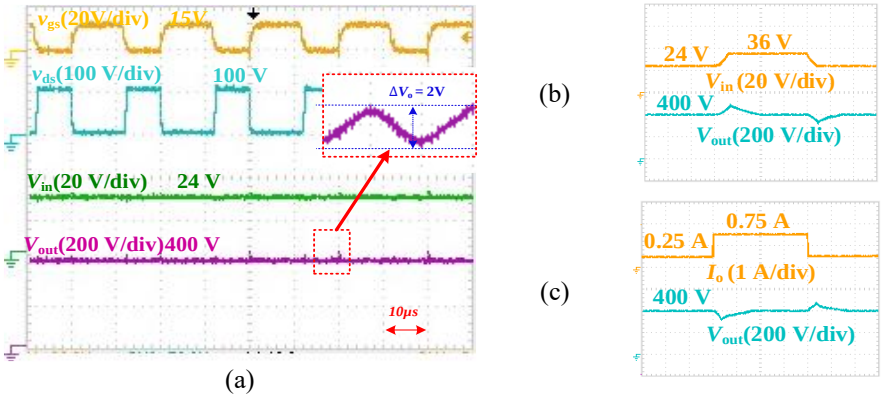


Figure 7. Simulated output voltage under ±5% magnetizing inductance (L_m) variation

(a) (b)

Figure 8. Hardware implementation of the PC: (a) prototype and (b) experimental setup



(a) (b) (c)

Figure 9. Experimental results: (a) waveforms with V_{in} = 24 V, V_O = 400 V, and P_o = 300 W, transient responses under (b) input voltage variation, and (c) load variation

The dynamic performance of the PC was further examined under two conditions:

- Input-voltage variation seen in Figure 9(b): V_{in} was increased from 24 V to 36 V while delivering 300 W. V_O hold steady at 400 V, exhibiting only minor overshoot and a short settling time, demonstrating robust control performance.
- Load variation illustrated in Figure 9(c): the load was step-changed from 33.3% (0.25 A) to 100% (0.75 A) of full load. The PC maintained V_O near 400 V with small transient deviation and fast recovery, confirming stable dynamic operation.

4.2. Comparisons with other converters

Table 2 provides a comparative analysis of key parameters, including the number of switches (S), inductors (I), CI, diodes (D), capacitors (C), voltage conversion ratio, and VS of MOSFET. Developing a new topology with high VG and minimized VS is essential for enhancing converter performance. Figure 10 presents a graphical comparison of VG variation with the duty cycle among the proposed and referenced converters, demonstrating that the PC attains the highest VG, surpassing existing designs. It features a single switch, similar to [31]–[33], which simplifies control and reduces switching losses. Additionally, the PC incorporates one inductor and one CI, fewer than [30], [32], and requires fewer diodes than [30], [33]. A key advantage of the PC is its significantly lower switch VS compare to other topologies, allowing low-voltage switch to improve

efficiency. With its superior VG, reduced VS, and practical implementation, the PC stands out as a highly efficient solution for high VG applications, particularly in RES.

Table 2. Comparison of published converters and the PC

Reference	Component count				VG	VS of switch ($/V_O$)
	S	D	C	I/CI		
[30]	2	8	5	0/2	$\frac{2+nD}{1-D}$	$\frac{1}{2+nD}$
[31]	1	6	5	1/1	$\frac{1+n-nD^2}{(1-D)^2}$	$\frac{1}{1+n-nD^2}$
[32]	1	6	4	2/1	$\frac{1+nD}{(1-D)^2}$	$\frac{n^2+(1+n)(1+nD)}{n(1+n)(1+nD)}$
[33]	1	7	5	1/1	$\frac{1+n}{(1-D)^2}$	$\frac{1}{2}$
Proposed converter	1	6	5	1/1	$\frac{n+1+nD}{(1-D)^2}$	$\frac{1}{n+1+nD}$

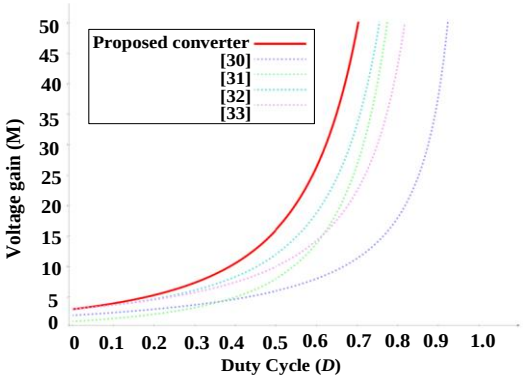


Figure 10. Comparison of VG curves versus duty cycle at n = 2

5. CONCLUSION

This paper presents an ultra-high VG DC–DC converter using a quadratic topology with a CI. The PC features a single active switch, simplifying the control strategy and reducing switching losses. A passive clamp circuit is incorporated to recycle the leakage energy, thereby minimizing the VS on the MOSFET and allowing the use of a low-resistance switch to enhance efficiency. Theoretical analysis, including steady-state operation and component design, validates the feasibility and performance of the PC. Moreover, the influence of magnetizing inductance, duty cycle, and parasitic components on the VG is thoroughly analyzed. The system's transient response to input voltage and load changes has also been investigated to ensure stable operation. SIMPLIS simulation and experimental verification using a 300 W hardware prototype confirm the converter's high efficiency, excellent VG, and reliable performance. The prototype achieves a peak efficiency of 93.6%, demonstrating its potential for renewable energy conversion applications.

FUNDING INFORMATION

This research received no external funding.

AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

Name of Author	C	M	So	Va	Fo	I	R	D	O	E	Vi	Su	P	Fu
Kim-Anh Nguyen	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Thai Anh Au Tran	✓	✓	✓	✓	✓	✓		✓	✓	✓	✓	✓	✓	✓
Xuan Khanh Ho	✓		✓	✓	✓	✓		✓	✓	✓	✓			
Duong Thach Pham			✓	✓		✓	✓	✓	✓		✓			

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

The authors confirm that the data supporting the findings of this study are available within the article.

REFERENCES

[1] Z. Tang, Y. Yang, and F. Blaabjerg, "Power electronics: The enabling technology for renewable energy integration," *CSEE Journal of Power and Energy Systems*, vol. 8, no. 1, pp. 39–52, 2022, doi: 10.17775/CSEEJPES.2021.02850.

[2] M. Kanabar and C. Cosoreanu, "Building the grid of the future to accelerate energy transition: innovations and digital transformation for global utilities," *IEEE Power and Energy Magazine*, vol. 22, no. 2, pp. 90–99, 2024, doi: 10.1109/MPE.2024.3351609.

[3] H. Tiismus, V. Maask, V. Astapov, T. Korotko, and A. Rosin, "State-of-the-art review of emerging trends in renewable energy generation technologies," *IEEE Access*, vol. 13, pp. 10820–10843, 2025, doi: 10.1109/ACCESS.2025.3528640.

[4] J. S. Kim, J. S. Song, C. H. Kim, J. Mahseredjian, and S. H. Kim, "Consideration on present and future of battery energy storage system to unlock battery value," *Journal of Modern Power Systems and Clean Energy*, vol. 13, no. 2, pp. 622–636, 2025, doi: 10.35833/MPCE.2023.000723.

[5] A. Pradhan, S. Mohapatra, K. Ray, S. Mohapatra, R. N. Senapati, and A. K. Giri, "Impact of solar panels on the environment and its analysis at various mounting condition," in *Proceedings of International Conference on Computational Intelligence and Sustainable Engineering Solution, CISES 2023*, 2023, pp. 371–375, doi: 10.1109/CISES58720.2023.10183542.

[6] G. Velasco-Quesada, F. Guinjoan-Gispert, R. Piqué-López, M. Román-Lumbreras, and A. Conesa-Roca, "Electrical PV array reconfiguration strategy for energy extraction improvement in grid-connected PV systems," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 11, pp. 4319–4331, 2009, doi: 10.1109/TIE.2009.2024664.

[7] Z. H. Shi, K. W. E. Cheng, and S. L. Ho, "Static performance and parasitic analysis of tapped-inductor converters," *IET Power Electronics*, vol. 7, no. 2, pp. 366–375, 2014, doi: 10.1049/iet-pel.2012.0760.

[8] F. Lin Luo and H. Ye, "Ultra-lift Luo-converter," *2004 International Conference on Power System Technology, POWERCON 2004*, vol. 1, pp. 81–86, 2004, doi: 10.1201/9781420037104.ch7.

[9] S. Khan *et al*., "A high step-up dc-dc converter based on the voltage lift technique for renewable energy applications," *Sustainability (Switzerland)*, vol. 13, no. 19, 2021, doi: 10.3390/su131911059.

[10] M. Samiullah, A. Iqbal, I. Ashraf, and P. K. Maroti, "Voltage lift switched inductor double leg converter with extended duty ratio for DC microgrid application," *IEEE Access*, vol. 9, pp. 85310–85325, 2021, doi: 10.1109/ACCESS.2021.3088957.

[11] H. Gholizadeh, M. Dehghan, R. S. Shahrivar, M. H. Samimi, and M. Ghassemi, "A non-isolated quadratic DC-DC converter improved by voltage-lift technique suitable for high-voltage applications," *IEEE Access*, vol. 12, pp. 158292–158310, 2024, doi: 10.1109/ACCESS.2024.3484667.

[12] S. M. Alilou, M. Maalandish, A. Samadian, P. Abolhassani, S. H. Hosseini, and M. H. Khooban, "High step-up DC-DC converter using voltage lift techniques for renewable applications," *CSEE Journal of Power and Energy Systems*, vol. 11, no. 2, pp. 739–749, 2025, doi: 10.17775/CSEEJPES.2022.02910.

[13] H. Gholizadeh, R. S. Shahrivar, S. Amini, and T. Rahimi, "An improved cascaded boost converter with an ultra-high voltage gain suitable for dielectric quality tests," *Energies*, vol. 17, no. 15, 2024, doi: 10.3390/en17153861.

[14] A. A. Emon, M. Tabassum, N. Subhani, and K. Bingi, "A non-isolated modified ultra high step-up quadratic boost converter with classical voltage doubler circuit," *The Journal of Engineering*, vol. 2024, no. 11, Nov. 2024, doi: 10.1049/tje2.70029.

[15] W. Qian, D. Cao, J. G. Cintron-Rivera, M. Gebben, D. Wey, and F. Z. Peng, "A switched-capacitor DC-DC converter with high voltage gain and reduced component rating and count," *IEEE Transactions on Industry Applications*, vol. 48, no. 4, pp. 1397–1406, 2012, doi: 10.1109/TIA.2012.2199731.

[16] A. F. de Souza, F. L. Tofoli, and E. R. Ribeiro, "Switched capacitor DC-DC Converters: A survey on the main topologies, design characteristics, and applications," *Energies*, vol. 14, no. 8, p. 2231, Apr. 2021, doi: 10.3390/en14082231.

[17] T. Sabetfar, M. Hosseinpour, A. Seifi, and H. Heydari-doostabad, "Switched capacitor nonisolated step-up DC–DC converter with low voltage stress of devices and high efficiency," *IEEE Transactions on Power Electronics*, vol. 40, no. 10, pp. 15130–15148, Oct. 2025, doi: 10.1109/TPEL.2025.3578205.

[18] H. Alnuman, M. R. Hussan, S. Islam, A. Sarwar, E. M. Ahmed, and A. Armghan, "A single-source switched-capacitor 13-level high gain inverter with lower switch stress," *IEEE Access*, vol. 11, pp. 38082–38093, 2023, doi: 10.1109/ACCESS.2023.3266050.

[19] M. R. Mohammed, A. Saad Al-Sumaiti, and A. R. Beig, "Hybrid active switched inductor DC-DC converter with common ground and suppressed voltage oscillation for fuel cell vehicles," *IEEE Transactions on Transportation Electrification*, vol. 11, no. 1, pp. 3204–3214, 2025, doi: 10.1109/TTE.2024.3434710.

[20] M. S. Bhaskar *et al.*, "A new hybrid zeta-boost converter with active quad switched inductor for high voltage gain," *IEEE Access*, vol. 9, pp. 20022–20034, 2021, doi: 10.1109/ACCESS.2021.3054393.

[21] Y. Tang, H. Tong, R. Afzal, and Y. Guo, "High step-Up ZVT converter based on active switched coupled inductors," *IEEE Access*, vol. 13, pp. 15178–15187, 2025, doi: 10.1109/ACCESS.2020.3041004.

[22] R. Fani, Z. Akhlaghi, and E. Adib, "High step-up DC-DC converter by integration of active switched inductors, built in transformer, and multipliers," *IEEE Transactions on Power Electronics*, vol. 39, no. 2, pp. 2468–2477, 2024, doi: 10.1109/TPEL.2023.3335391.

[23] H. Li and D. Chen, "A novel high step-up nonisolated quasi-Z-source DC-DC converter with active switched inductor and switched capacitor," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 5, pp. 5062–5077, 2023, doi: 10.1109/JESTPE.2023.3295408.

[24] N. Vazquez, L. Estrada, C. Hernandez, and E. Rodriguez, "The tapped-inductor boost converter," *IEEE International Symposium on Industrial Electronics*, pp. 538–543, 2007, doi: 10.1109/ISIE.2007.4374654.

[25] Y. Tang and T. Wang, "Study of an improved dual-switch converter with passive lossless clamping," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 2, pp. 972–981, 2015, doi: 10.1109/TIE.2014.2341608.

[26] M. Harasimczuk, R. Kopacz, and A. Tomaszuk, "Lossless clamp circuit with turn-off voltage and current reduction in high step-up DC-DC converter with coupled inductor," *IEEE Transactions on Power Electronics*, vol. 39, no. 1, pp. 1074–1086, 2024, doi: 10.1109/TPEL.2023.3327064.

[27] M. K. Nguyen, T. D. Duong, and Y. C. Lim, "Switched-capacitor-based dual-switch high-boost DC-DC converter," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 4181–4189, 2018, doi: 10.1109/TPEL.2017.2719040.

[28] K. A. Nguyen, T. A. A. Tran, X. K. Ho, and D. T. Pham, "A two-switch step-up topology with coupled inductor for high voltage conversion," *IEEE Access*, vol. 13, pp. 154326–154340, 2025, doi: 10.1109/ACCESS.2025.3605292.

[29] M. E. Azizkandi, F. Sedaghati, H. Shayeghi, and F. Blaabjerg, "A high voltage gain DC-DC converter based on three winding coupled inductor and voltage multiplier cell," *IEEE Transactions on Power Electronics*, vol. 35, no. 5, pp. 4558–4567, 2020, doi: 10.1109/TPEL.2019.2944518.

[30] M. B. Meier, D. S. S. Avelino, A. A. Badin, E. F. R. Romaneli, and R. Gules, "Soft-switching high static gain DC-DC converter without auxiliary switches," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 3, pp. 2335–2345, 2018, doi: 10.1109/TIE.2017.2739684.

[31] M. Karimi Hajiabadi, A. Lahooti Eshkevari, A. Mosallanejad, and A. Salemnia, "Non-isolated high step-up DC/DC converter for low-voltage distributed power systems based on the quadratic boost converter," *International Journal of Circuit Theory and Applications*, vol. 50, no. 6, pp. 1946–1964, 2022, doi: 10.1002/cta.3234.
[32] S. W. Lee and H. L. Do, "High step-up coupled-inductor cascade boost DC-DC converter with lossless passive snubber," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 10, pp. 7753–7761, 2018, doi: 10.1109/TIE.2018.2803731.
[33] S. A. Modaberi, B. Allahverdinejad, and M. R. Banaei, "A quadratic high step-up DC-DC boost converter based on coupled inductor with Single Switch and Continuous Input Current," *2021 12th Power Electronics, Drive Systems, and Technologies Conference, PEDSTC 2021*, 2021, doi: 10.1109/PEDSTC52094.2021.9405958.

BIOGRAPHIES OF AUTHORS

Kim-Anh Nguyen is currently a lecturer at the University of Danang - University of Science and Technology, Vietnam. He served as the Head of the Automation Division in the Faculty of Electrical Engineering from 2016 to 2020. He received his Engineer's degree in Electrical Engineering from the University of Science and Technology in 2004, an M.Eng. degree in Control Engineering and Automation from the University of Danang in 2009, and a Ph.D. in Systems Optimization and Dependability from Troyes University of Technology, France, in 2015. His current research interests include stochastic modeling of system deterioration, diagnosis, prognosis, and health management techniques, maintenance decision-making, power electronics, power quality, IoT, embedded systems, and control systems. He can be contacted at email: nkanh@dut.udn.vn.

Thai Anh Au Tran was born in Quang Nam, Vietnam. He received his B.S. and M.S. degrees in Electrical Engineering from Hanoi University of Science and Technology, Hanoi, Vietnam, in 2004 and 2007, respectively. He earned his Ph.D. in Electrical Engineering from National Cheng Kung University, Tainan, Taiwan, in 2023. Since 2007, he has been a Lecturer at the Faculty of Electrical Engineering, the University of Danang - University of Science and Technology, Vietnam. His current research focuses on power electronics and control engineering. He can be contacted at email: ttaau@dut.udn.vn.

Xuan Khanh Ho is currently a student at The University of Danang - University of Science and Technology, Vietnam, where he has been studying Electrical Engineering since 2020. He was born on February 2, 2002, in Hue City, Vietnam. His research interests focus on DC–DC converters. He can be contacted at email: hxkhanh.dut.ud@gmail.com.

Duong Thach Pham is currently a student at The University of Danang - University of Science and Technology, Vietnam, where he has been studying Electrical Engineering since 2020. He was born on May 10, 2002, in Quang Ngai Province, Vietnam. His research interests include renewable energy and DC–DC converters. He can be contacted at email: pdthach.dut.ud@gmail.com.